19-3412; Rev 3; 5/07

Quad Network Power Controller for Power-Over-LAN

General Description

The MAX5935 quad network power controller is designed for use in IEEE 802.3af-compliant power sourcing equipment (PSE). The device provides power devices (PD) discovery, classification, current limit, and both DC and AC load disconnect detections. The MAX5935 can be used in either endpoint PSE (LAN switches/routers) or midspan PSE (power injector) applications.

The MAX5935 can operate autonomously or be controlled by software through an I²C-compatible interface. Separate input and output data lines (SDAIN and SDAOUT) allow usage with optocouplers. The MAX5935 is a slave device. Its four address inputs allow 16 unique MAX5935 addresses. A separate $\overline{INT}$ output and four independent shutdown inputs ($\overline{SHD\_}$) allow fast response from a fault to port shutdown. A $\overline{RESET}$ input allows hardware reset of the device. A special Watchdog feature allows the hardware to gracefully take over control if the software crashes. A cadence timing feature allows the MAX5935 to be used in midspan systems.

The MAX5935 is fully software configurable and programmable. A class-over-current detection function enables system power management to detect if a PD draws more current than the allowable amount for its class. Other features are input under/overvoltage lockout, overtemperature protection, output voltage slew-rate limit during startup, power-good, and fault status. The MAX5935's programmability includes gate charging current, current-limit threshold, startup timeout, overcurrent timeout, autorestart duty cycle, PD disconnect AC detection threshold, and PD disconnect detection timeout.

The MAX5935 is available in a 36-pin SSOP package and is rated for both extended (-40°C to +85°C) and commercial (0°C to +70°C) temperature ranges.

Applications

Power-Sourcing Equipment (PSE)

Power-Over-LAN/Power-Over-Ethernet

Switches/Routers

Midspan Power Injectors

Typical Operating Circuits appear at end of data sheet.

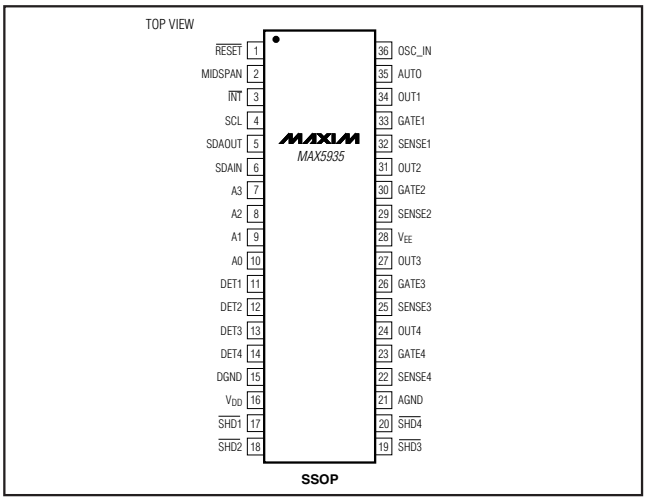
Features

- **IEEE 802.3af Compliant**
- **Controls Four Independent, -48V-Powered Ethernet Ports in Either Endpoint or Midspan PSE Applications**
- **Wide Digital Power Input, V_{DIG}, Common-Mode Range: V_{EE} to (AGND + 7.7V)**
- **PD Violation of Class Current Protection**
- **PD Detection and Classification**
- **Provides Both DC and AC Load Removal Detections**
- **I²C-Compatible, 3-Wire Serial Interface**
- **Fully Programmable and Configurable Operation Through I²C Interface**
- **Current Foldback and Duty-Cycle-Controlled/Programmable Current Limit**
- **Short-Circuit Protection with Fast Gate Pulldown**
- **Direct Fast Shutdown Control Capability**
- **Programmable Direct Interrupt Output**
- **Watchdog Mode Enable Hardware Graceful Takeover**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5935CAX	0°C to +70°C	36 SSOP	A36-2
MAX5935CAX+	0°C to +70°C	36 SSOP	A36-2
MAX5935EAX	-40°C to +85°C	36 SSOP	A36-2
MAX5935EAX+	-40°C to +85°C	36 SSOP	A36-2

Pin Configuration



Quad Network Power Controller for Power-Over-LAN

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)
AGND, DGND, DET_, V_{DD}, $\overline{RESET}$, A3, A2, A1, A0, $\overline{SHD\_}$, OSC_IN, SCL, SDAIN, OUT_ and AUTO .....-0.3V to +80V
GATE_ (Internally Clamped, Note 1) .....-0.3V to +11.4V
SENSE_ .....-0.3V to +24V
V_{DD}, $\overline{RESET}$, A3, A2, A1, A0, $\overline{SHD\_}$, OSC_IN, SCL, SDAIN and AUTO to DGND .....-0.3V to +7V
$\overline{INT}$ and SDAOUT to DGND.....-0.3V to +12V
Maximum Current into $\overline{INT}$, SDAOUT, DET_ 80mA

Maximum Power Dissipation
36-Pin SSOP (derate 11.4mW/°C above +70°C) 941mW
Operating Temperature Ranges:
MAX5935EAX .....-40°C to +85°C
MAX5935CAX .....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AGND = +48V. V_{EE} = 0V, V_{DD} to DGND = +3.3V. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at AGND = +48V, DGND = +48V, V_{DD} = (DGND + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}		32		60	V
	V_{DGND}			0		60	
	V_{DD}	V_{DD} to V_{DGND}, V_{DGND} = V_{AGND}		1.71		5.50	
		V_{DD} to V_{DGND}, V_{DGND} = V_{EE}		3.0		5.5	
Supply Currents	I_{EE}	OUT_= V_{EE}, SENSE_ = V_{EE}, DET_ = AGND, all logic inputs open, SCL = SDAIN = V_{DD}, $\overline{INT}$ and SDAOUT open; measured at AGND in power mode after GATE_ pullup			4.2	6.8	mA
	I_{DIG}	All logic inputs high, measured at V_{DD}			2.7	5.6	
GATE DRIVER AND CLAMPING							
GATE_ Pullup Current	I_{PU}	Power mode, gate drive-on, V_{GATE} = V_{EE} (Note 2)		-35	-50	-65	µA
Weak GATE_ Pulldown Current	I_{PDW}	$\overline{SHD\_}$ = DGND, $V_{GATE\_}$ = V_{EE} + 5V		25	40	55	µA
Maximum Pulldown Current	I_{PDS}	V_{SENSE} = 1V, $V_{GATE\_}$ = V_{EE} + 2V			100		mA
External Gate Drive	V_{GS}	V_{GATE} - V_{EE} , power mode, gate drive-on		9	10	11	V
CURRENT LIMIT							
Current-Limit Clamp Voltage	V_{SU_LIM}	Maximum $V_{SENSE\_}$ allowed during current limit, $V_{OUT\_}$ = V_{EE} (Note 3)		202	212	222	mV
Overcurrent Threshold After Startup	V_{FLT_LIM}	Overcurrent $V_{SENSE\_}$ threshold allowed for t ≤ t_{FAULT} after startup; $V_{OUT\_}$ = V_{EE}	Default, Class 0, Class 3, Class 4	177		196	mV
			Class 1	48		61	
			Class 2	89		105	
Foldback Initial OUT_ Voltage	V_{FLBK_ST}	$V_{OUT\_}$ - V_{EE}, above which the current-limit trip voltage starts folding back			30		V
Foldback Final OUT_ Voltage	V_{FLBK_END}	$V_{OUT\_}$ - V_{EE}, above which the current-limit trip voltage reaches V_{TH_FB}			50		V

ELECTRICAL CHARACTERISTICS (continued)

(AGND = +48V. V_{EE} = 0V, V_{DD} to DGND = +3.3V. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at AGND = +48V, DGND = +48V, V_{DD} = (DGND + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Foldback Current-Limit Threshold	V_{TH_FB}	$V_{OUT\_}$ = V_{AGND}		64		mV
SENSE_ Input Bias Current		$V_{SENSE\_}$ = V_{EE}			-2	µA
SUPPLY MONITORS						
V_{EE} Undervoltage Lockout	V_{EEUVLO}	V_{AGND} - V_{EE}, (V_{AGND} – V_{EE}) increasing		28.5		V
V_{EE} Undervoltage-Lockout Hysteresis	$V_{EEUVLOH}$			3		V
V_{EE} Overvoltage	V_{EE_OV}	(V_{AGND} - V_{EE}) > V_{EE_OV}, V_{AGND} increasing		62.5		V
V_{EE} Overvoltage Hysteresis	V_{OVH}			1		V
V_{EE} Undervoltage	V_{EE_UV}	(V_{AGND} - V_{EE}) < V_{EE_UV}, V_{AGND} decreasing		40		V
V_{DD} Overvoltage	V_{DD_OV}	(V_{DD} - V_{DGND}) > V_{DD_OV}, V_{DD} increasing		3.71		V
V_{DD} Undervoltage	V_{DD_UV}	(V_{DD} - V_{DGND}) < V_{DD_UV}, V_{DD} decreasing		2.82		V
V_{DD} Undervoltage Lockout	V_{DDUVLO}	Device operates when (V_{DD} - V_{DGND}) > V_{DDUVLO}, V_{DD} increasing		1.3		V
V_{DD} Undervoltage-Lockout Hysteresis	V_{DDHYS}			120		mV
Thermal-Shutdown Threshold	T_{SHD}	Ports shut down and device resets if its junction temperature exceeds this limit, temperature increasing		+150		°C
Thermal-Shutdown Hysteresis	T_{SHDH}			20		°C
OUTPUT MONITOR						
OUT_ Input Current	I_{BOUT}	V_{OUT} = V_{AGND}, all modes			2	µA
Idle Pullup Current at OUT_	I_{DIS}	OUT_ discharge current, detection and classification off, port shutdown, $V_{OUT\_}$ = V_{AGND} - 2.8V	200		260	µA
PGOOD High Threshold	PG_{TH}	$V_{OUT\_}$ - V_{EE}, OUT_ decreasing	1.5	2.0	2.5	V
PGOOD Hysteresis	PG_{HYS}			220		mV
PGOOD Low-to-High Glitch Filter	t_{PGOOD}	Minimum time PGOOD has to be high to set bit in register 10h		3		ms
LOAD DISCONNECT						
DC Load Disconnect Threshold	V_{DCTH}	Minimum V_{SENSE} allowed before disconnect (DC disconnect active), $V_{OUT\_}$ = V_{EE}	2.5	4	5	mV

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ELECTRICAL CHARACTERISTICS (continued)

(AGND = +48V. V_{EE} = 0V, V_{DD} to DGND = +3.3V. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at AGND = +48V, DGND = +48V, V_{DD} = (DGND + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC Load Disconnect Threshold (Note 4)	I_{ACTH}	Current into DET_, ACD_EN_ bit = high, OSC_IN = 2.2V		300	325	350	µA
Oscillator Buffer Gain	A_{OSC}	$V_{DET\_}/V_{OSC\_IN}$, ACD_EN_ bit = high, C_{DET} = 400nF		2.90	2.93	3.1	V/ V
OSC_IN Fail Threshold (Note 5)	V_{OSC_FAIL}	Port will not power on if $V_{OSC\_IN} < V_{OSC\_FAIL}$ and ACD_EN_ bit = high		1.8	1.9	2.2	V
OSC_IN Input Resistance	Z_{OSC}	OSC_IN input impedance when all the ACD_EN_ are active		100			kΩ
OSC_IN Input Capacitance	C_{OSC_IN}				5		pF
Load Disconnect Timer	t_{DISC}	Time from $V_{SENSE} < V_{DCTH}$ or current into DET_ < I_{ACTH} to gate shutdown (Note 6)		300		400	ms
DETECTION							
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - $V_{DET\_}$ during the first detection phase		3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - $V_{DET\_}$ during the second detection phase		9.0	9.3	9.6	V
Current-Limit Protection	I_{DLIM}	$V_{DET\_}$ = V_{AGND}, during detection, measure current through DET_		1.5	1.75	2.0	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - $V_{OUT} < V_{DCP}$ after the first detection phase a short circuit to AGND is detected			1.62		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition			12.5		µA
Resistor Detection Window	R_{DOK}	(Note 7)		19.0		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values				15.2	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
Classification Probe Voltage	V_{CL}	V_{AGND} - $V_{DET\_}$ during classification		16		20	V
Current-Limit Protection	I_{CILIM}	$V_{DET\_}$ = V_{AGND}, during classification, measure current through DET_		50		75	mA
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes	Class 0, Class 1	5.5	6.5	7.5	mA
			Class 1, Class 2	13.0	14.5	16.0	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			>Class 4	45	48	51	
DIGITAL INPUTS/OUTPUTS (REFERRED to DGND)							
Digital Input Low	V_{IL}					0.9	V
Digital Input High	V_{IH}			2.4			V

ELECTRICAL CHARACTERISTICS (continued)

(AGND = +48V. V_{EE} = 0V, V_{DD} to DGND = +3.3V. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at AGND = +48V, DGND = +48V, V_{DD} = (DGND + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Input Pullup/Pulldown Resistor	R_{DIN}	Pullup (pulldown) resistor to V_{DD} (DGND) to set default level		25	50	75	kΩ
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 15mA				0.4	V
Open-Drain Leakage	I_{OL}	Open-drain high impedance, V_O = 3.3V				2	µA
TIMING							
Startup Time	t_{START}	Time during which a current limit set by V_{SU_LIM} is allowed, starts when the GATE_ is turned on (Note 8)		50	60	70	ms
Fault Time	t_{FAULT}	Maximum allowed time for an overcurrent condition set by V_{FLT_LIM} after startup (Note 8)		50	60	70	ms
Port Turn-Off Time	t_{OFF}	Minimum delay between any port turning off, does not apply in the case of a reset		0.5	0.75	1	ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed				320	ms
Midspan Mode Detection Delay	t_{DMID}			2.0		2.4	s
Classification Time	t_{CLASS}	Time allowed for classification				40	ms
V_{EEUVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EEUVLO} thresholds before the device operates		2		4	ms
Restart Timer	$t_{RESTART}$	Time a port has to wait before turning on after an overcurrent fault, RSTR_EN bit = high	RSTR bits = 00		16 x t_{FAULT}		ms
			RSTR bits = 01		32 x t_{FAULT}		
			RSTR bits = 10		64 x t_{FAULT}		
			RSTR bits = 11		0		
Watchdog Clock Period	t_{WD}	Rate of decrement of the watchdog timer			164		ms
TIMING CHARACTERISTICS for 2-WIRE FAST MODE (Figures 5 and 6)							
Serial Clock Frequency	f_{SCL}	(Note 9)				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}	(Note 9)		1.2			µs
Hold Time for Start Condition	$t_{HD, STA}$	(Note 9)		0.6			µs
Low Period of the SCL Clock	t_{LOW}	(Note 9)		1.2			µs
High Period of the SCL Clock	t_{HIGH}	(Note 9)		0.6			µs

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ELECTRICAL CHARACTERISTICS (continued)

(AGND = +48V. V_{EE} = 0V, V_{DD} to DGND = +3.3V. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at AGND = +48V, DGND = +48V, V_{DD} = (DGND + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$	(Note 9)	0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 9)	0		150	ns
Data Setup Time	$t_{SU, DAT}$	(Note 9)	100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 9)	$20+0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F	(Note 9)	$20+0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU, STO}$	(Note 9)	0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Note 9)			50	ns

Note 1: GATE_ is internally clamped to 11.4V above V_{EE}. Driving GATE_ higher than 11.4V above V_{EE} may damage the device.

Note 2: Default values. The charge/discharge currents are programmable through the serial interface (see the *Register Map and Description* section).

Note 3: Default values. The current-limit thresholds are programmed through the I²C-compatible serial interface (see the *Register Map and Description* section).

Note 4: This is the default value. Threshold can be programmed through serial interface R23h[2:0].

Note 5: AC disconnect works only if $V_{DD} - V_{DGND} \geq 3V$.

Note 6: t_{DISC} can also be programmed through the serial interface (R29h) (see the *Register Map and Description* section).

Note 7: $R_D = (V_{OUT\_2} - V_{OUT\_1}) / (I_{DET\_2} - I_{DET\_1})$. V_{OUT_1}, V_{OUT_2}, I_{DET_2} and I_{DET_1} represent the voltage at OUT_ and the current at DET_ during phase 1 and 2 of the detection.

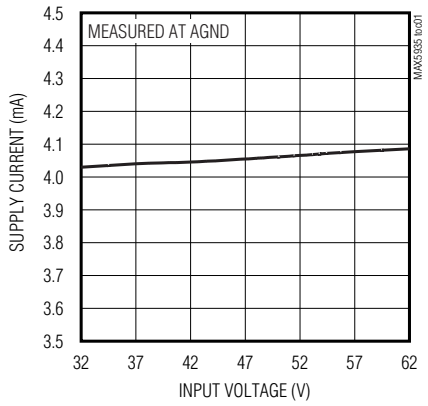
Note 8: Default values. The startup and fault times can be also programmed through the I²C serial interface (see the *Register Map and Description* section).

Note 9: Guaranteed by design. Not subject to production testing.

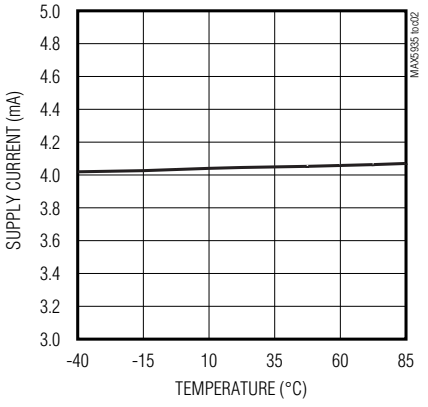
Typical Operating Characteristics

(V_{EE} = -48V, V_{DD} = +3.3V, AUTO = AGND = DGND = 0, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, T_A = +25°C, all registers = default setting, unless otherwise noted.)

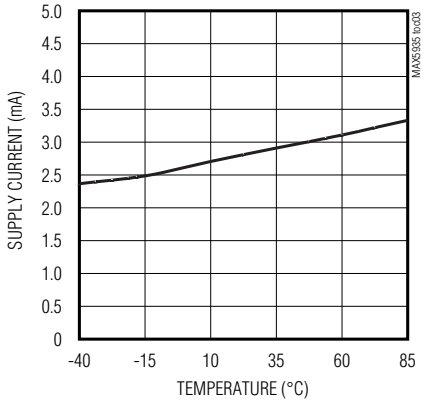
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



ANALOG SUPPLY CURRENT vs. TEMPERATURE



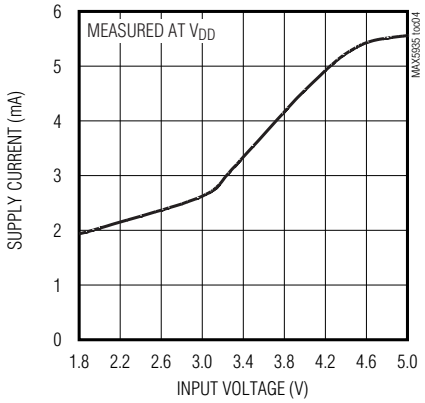
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



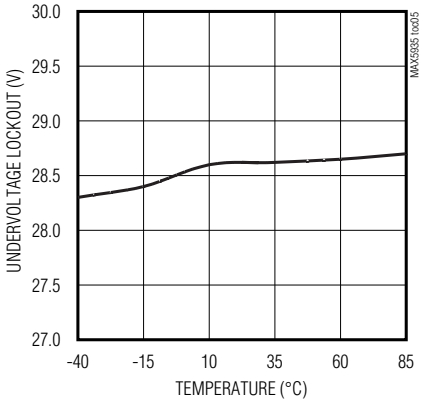
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, AUTO = AGND = DGND = 0, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, T_A = +25°C, all registers = default setting, unless otherwise noted.)

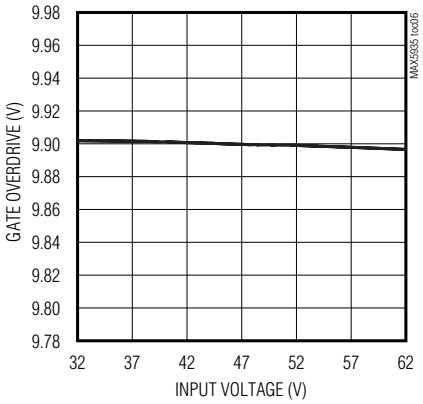
DIGITAL SUPPLY CURRENT vs. INPUT VOLTAGE



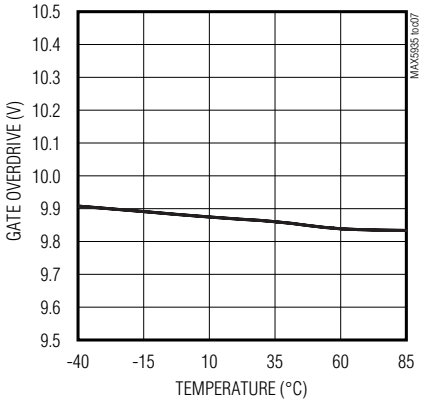
VEE UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



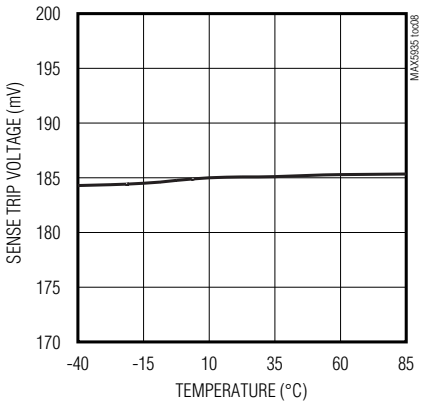
GATE OVERDRIVE vs. INPUT VOLTAGE



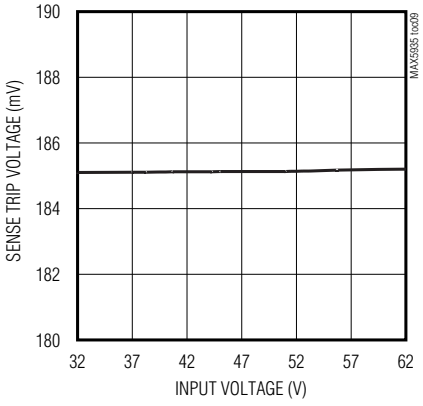
GATE OVERDRIVE vs. TEMPERATURE



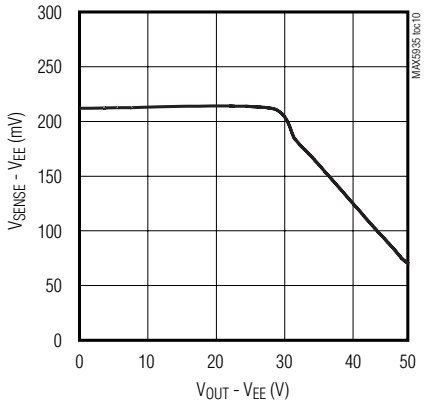
SENSE TRIP VOLTAGE vs. TEMPERATURE



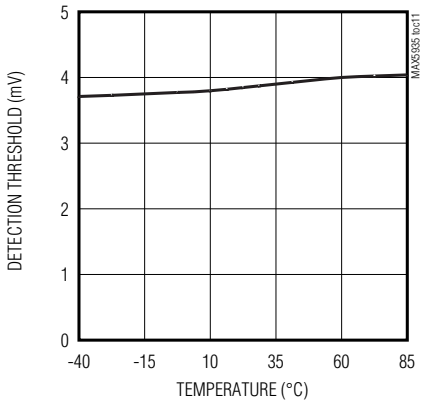
SENSE TRIP VOLTAGE vs. INPUT VOLTAGE



FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



ZERO-CURRENT DETECTION THRESHOLD vs. TEMPERATURE

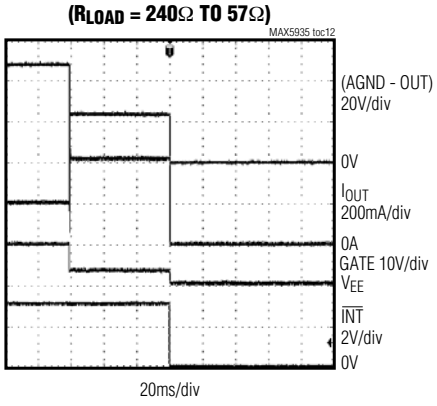


Quad Network Power Controller for Power-Over-LAN

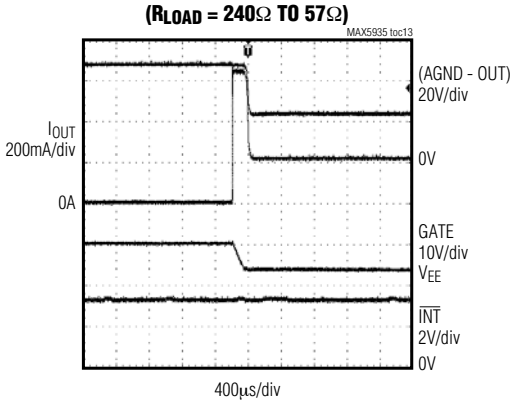
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, AUTO = AGND = DGND = 0, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, T_A = +25°C, all registers = default setting, unless otherwise noted.)

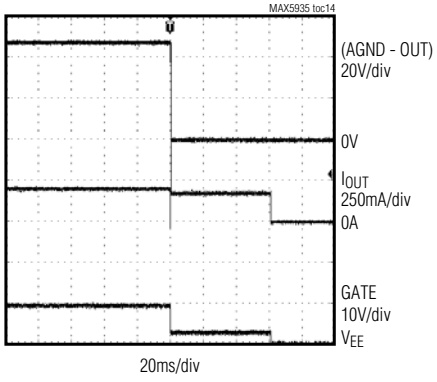
OVERCURRENT TIMEOUT (R_{LOAD} = 240Ω TO 57Ω)



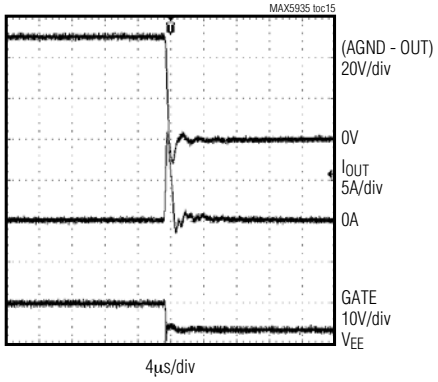
OVERCURRENT RESPONSE WAVEFORM (R_{LOAD} = 240Ω TO 57Ω)



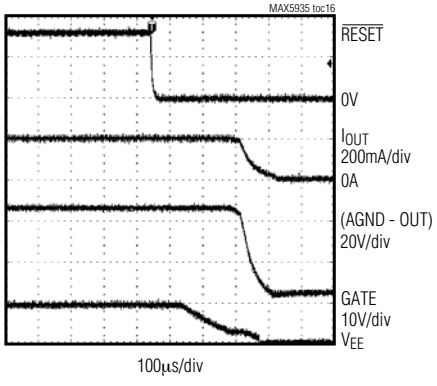
SHORT-CIRCUIT RESPONSE TIME



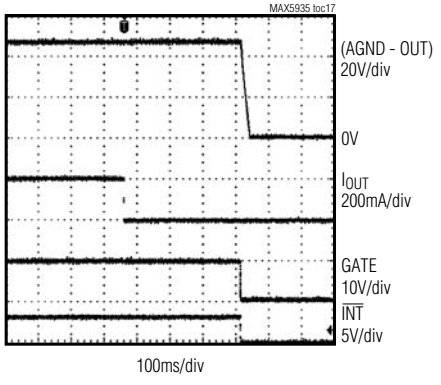
SHORT-CIRCUIT RESPONSE TIME



$\overline{RESET}$ TO OUTPUT TURN-OFF DELAY



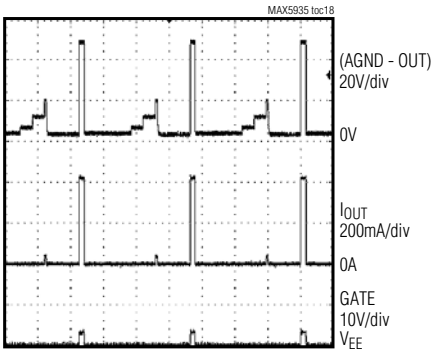
ZERO-CURRENT DETECTION WAVEFORM



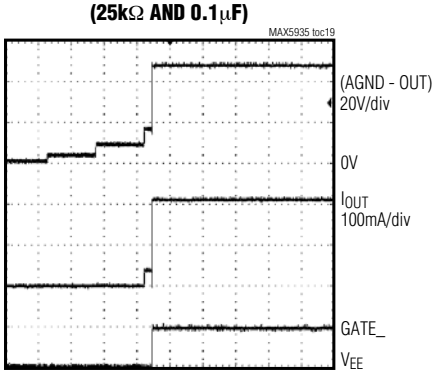
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, AUTO = AGND = DGND = 0, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, T_A = +25°C, all registers = default setting, unless otherwise noted.)

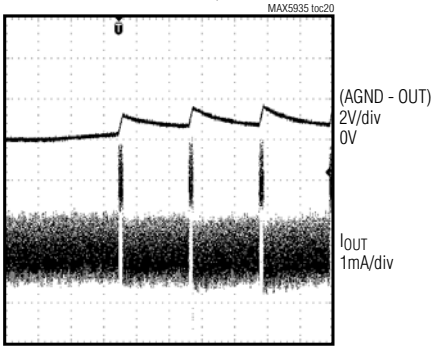
OVERCURRENT RESTART DELAY



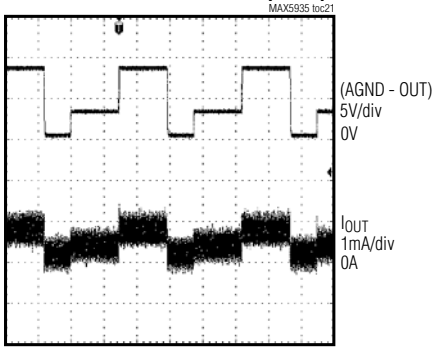
STARTUP WITH VALID PD (25kΩ AND 0.1μF)



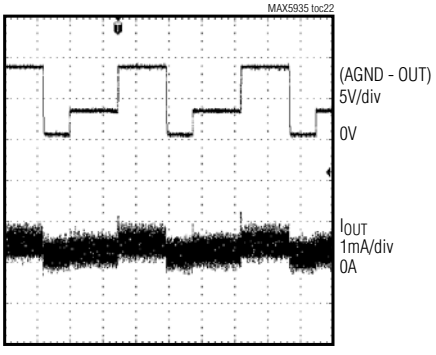
DETECTION WITH INVALID PD (25kΩ AND 10μF)



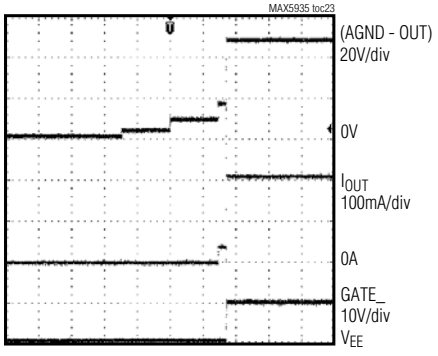
DETECTION WITH INVALID PD (15kΩ)



DETECTION WITH INVALID PD (33kΩ)



STARTUP IN MIDSPAN MODE WITH VALID PD (25kΩ AND 0.1μF)

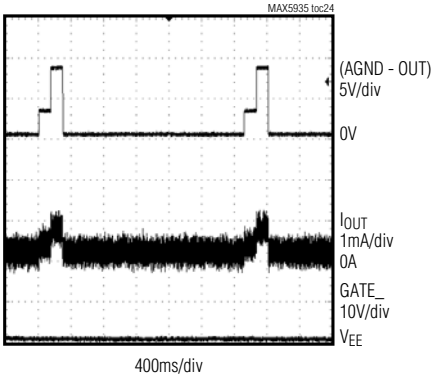


Quad Network Power Controller for Power-Over-LAN

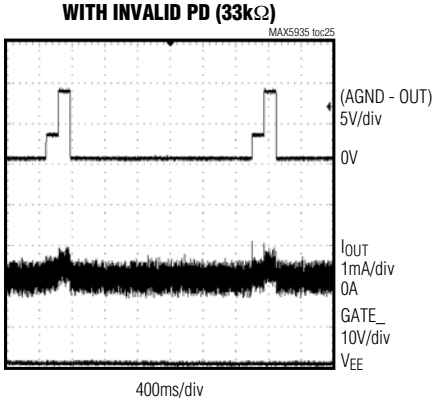
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, AUTO = AGND = DGND = 0, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, T_A = +25°C, all registers = default setting, unless otherwise noted.)

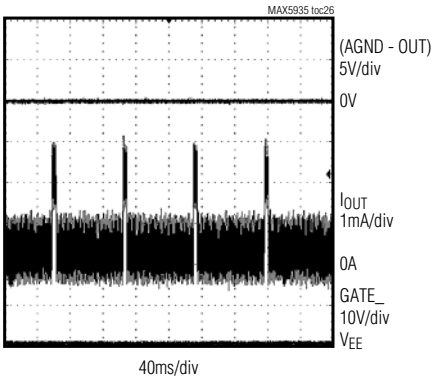
DETECTION WITH MIDSPAN MODE WITH INVALID PD (15kΩ)



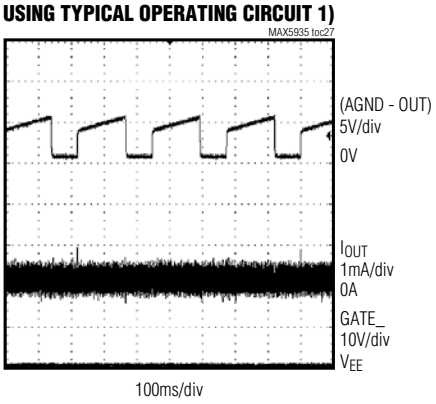
DETECTION WITH MIDSPAN MODE WITH INVALID PD (33kΩ)



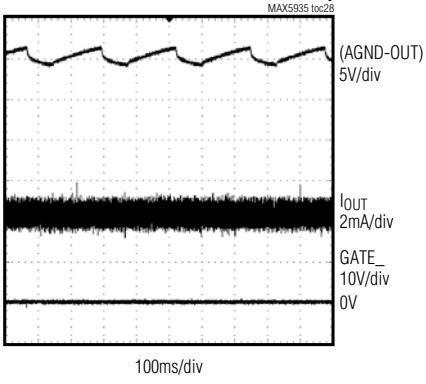
DETECTION WITH OUTPUT SHORTED



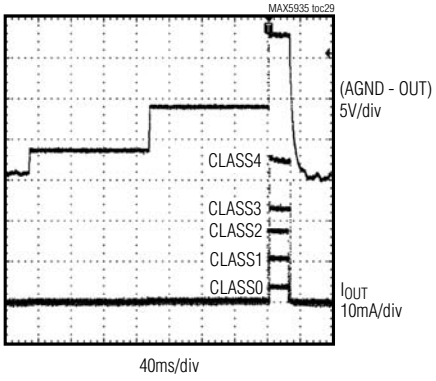
DETECTION WITH INVALID PD (OPEN CIRCUIT, USING TYPICAL OPERATING CIRCUIT 1)



DETECTION WITH INVALID PD (OPEN CIRCUIT, USING TYPICAL OPERATING CIRCUIT 2)



STARTUP WITH DIFFERENT PD CLASSES



Pin Description

PIN	NAME	FUNCTION
1	$\overline{RESET}$	Hardware Reset. Pull $\overline{RESET}$ low for at least 300µs to reset the device. All internal registers reset to their default value. The address (A0–A3), and AUTO and MIDSPAN input logic levels latch on during low-to-high transition of $\overline{RESET}$. Internally pulled up to V_{DD} with a 50kΩ resistor.
2	MIDSPAN	MIDSPAN Mode Input. An internal 50kΩ pulldown resistor to DGND sets the default mode to endpoint PSE operation (power-over-signal pairs). Pull MIDSPAN TO VDIG to set MIDSPAN operation. The MIDSPAN value latches after the IC is powered up or reset (see the *PD Detection* section).
3	$\overline{INT}$	Open-Drain Interrupt Output. $\overline{INT}$ goes low whenever a fault condition exists. Reset the fault condition using software or by pulling $\overline{RESET}$ low (see the *Interrupt* section of the *Detailed Description* for more information about interrupt management).
4	SCL	Serial Interface Clock Line
5	SDAOUT	Serial Output Data Line. Connect the data line optocoupler input to SDAOUT (see the *Typical Application Circuit*). Connect SDAOUT to SDAIN if using a 2-wire I^2C-compatible system.
6	SDAIN	Serial Interface Input Data Line. Connect the data line optocoupler output SDAIN (see the *Typical Application Circuit*). Connect SDAIN to SDAOUT if using a 2-wire wire I^2C-compatible system.
7–10	A3, A2, A1, A0	Address Bit. A3, A2, A1, and A0 form the lower part of the device's address. Address inputs default high with an internal 50kΩ pullup resistor to V_{DD}. The address values latch when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or after a reset. The 3 MSB bits of the address are set to 010.
11–14	DET1, DET2, DET3, DET4	Detection and Classification Voltage Output. Use DET1 to set the detection and classification probe voltages on port 1. Use DET1 for the AC voltage sensing of port 1 when using the AC disconnect scheme (see the *Typical Application Circuit*).
15	DGND	Connect to Digital Ground
16	V_{DD}	Positive Digital Supply. Connect to digital supply (referenced to DGND).
17–20	$\overline{SHD1}$, $\overline{SHD2}$, $\overline{SHD3}$, $\overline{SHD4}$	Port Shutdown Input. Pull $\overline{SHD\_}$ low to turn-off the external FET on port_. Internally pulled up to V_{DD} with a 50kΩ resistor.
21	AGND	Analog Ground. Connect to the high-side analog supply.
22, 25, 29, 32	SENSE4, SENSE3, SENSE2, SENSE1	MOSFET Source Current-Sense Negative Input. Connect to the source of the power MOSFET and connect a current-sense resistor between SENSE_ and V_{EE} (see the *Typical Application Circuit*).
23, 26, 30, 33	GATE4, GATE3, GATE2, GATE1	Port_ MOSFET Gate Driver. Connect GATE_ to the gate of the external FET (see the *Typical Application Circuit*).
24, 27, 31, 34	OUT4, OUT3, OUT2, OUT1	MOSFET Drain-Output Voltage Sense. Connect OUT_ to the power MOSFET drain through a resistor (100Ω to 100kΩ). The low leakage at OUT_ limits the drop across the resistor to less than 100mV (see the *Typical Application Circuit*).
28	V_{EE}	Low-Side Analog Supply Input. Connect the low-side analog supply to V_{EE} (-48V). Bypass with a 1µF capacitor between AGND and V_{EE}.
35	AUTO	AUTO or SHUTDOWN Mode Input. Force high to enter AUTO mode after a reset or power-up. Drive low to put the MAX5935 into SHUTDOWN mode. In SHUTDOWN mode, software controls the operational modes of the MAX5935. A 50kΩ internal pulldown resistor defaults AUTO low. AUTO latches when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or when the device resets. Software commands can take the MAX5935 out of AUTO while AUTO is high.
36	OSC_IN	Oscillator Input. AC-disconnect detection function uses OSC_IN. Connect a 100Hz ±10%, $2V_{P-P}$ ±5%, +1.2V offset sine wave to OSC_IN. If the oscillator positive peak falls below OSC_FAIL threshold of 2V, the ports that have the AC function enabled shut down and are not allowed to power up. When not using the AC-disconnect detection function, leave OSC_IN unconnected.

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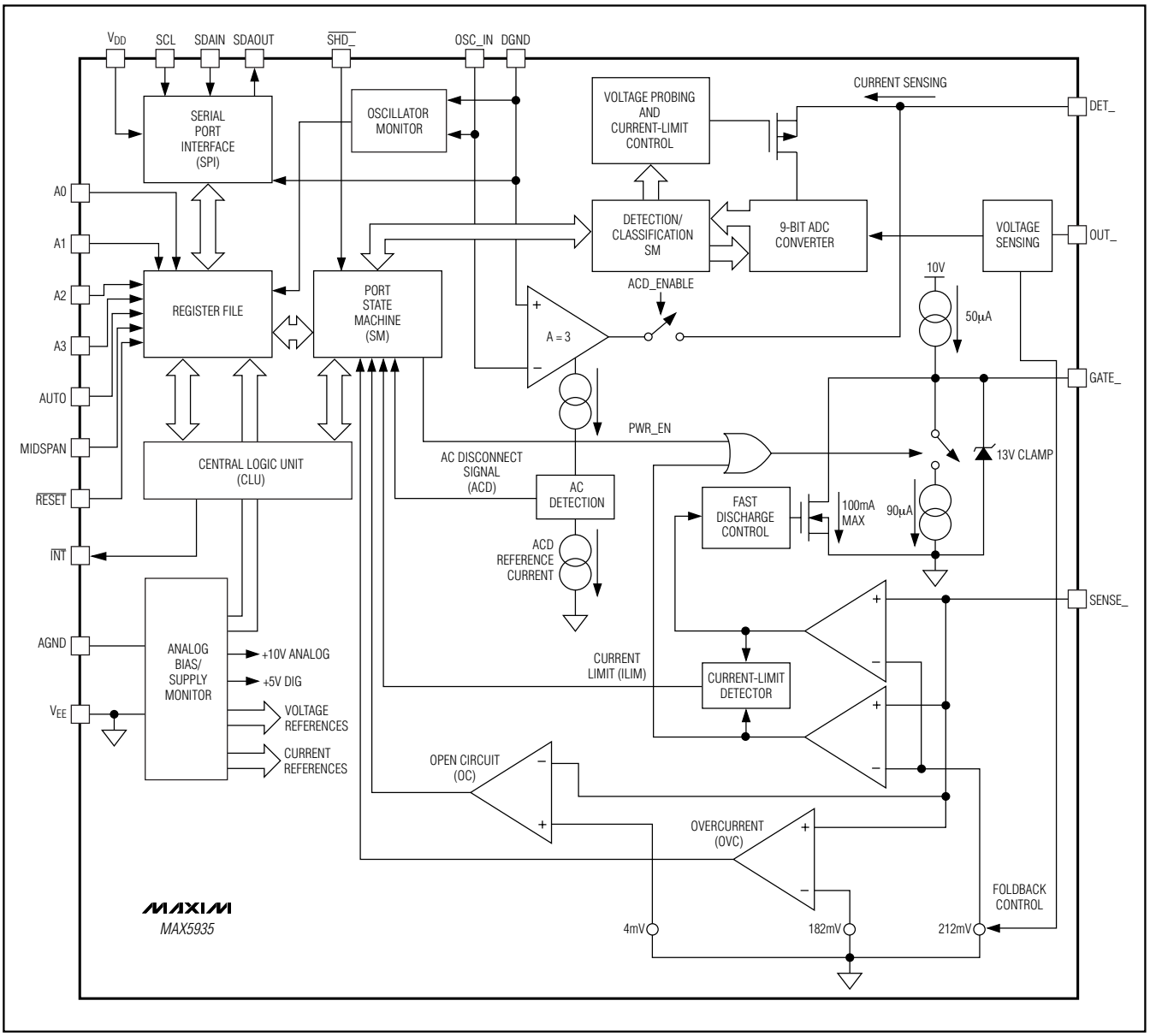

Figure 1. MAX5935 Functional Diagram

Detailed Description

The MAX5935 four-port network power controller controls -32V to -60V negative supply rail systems. Use the MAX5935, which is compliant with the IEEE 802.3af standard for power-sourcing equipment (PSE) in power-over-LAN applications. The MAX5935 provides Power Device (PD) discovery, classification, current limit, both DC and AC load disconnect detections, and other necessary functions for an IEEE 802.3af-compliant PSE. The MAX5935 can be used in either endpoint PSE (LAN Switch/Router) or midspan PSE (Power Injector) applications.

The MAX5935 is fully software-configurable and programmable with more than 25 internal registers. The device features an I²C-compatible, 3-wire serial interface and a class-over-current detection. The class-

over-current detection function enables system power management where it detects a PD that draws more current than the allowable amount for its class. The MAX5935's extensive programmability enhances system flexibility and allows for uses in other applications.

The MAX5935 has four different operating modes: auto mode, semi-auto mode, manual mode, and shutdown mode (see the *Operation Modes* section). A special Watchdog feature allows the hardware to gracefully take over control if the software/firmware crashes. A cadence timing feature allows the MAX5935 to be used in midspan systems.

The MAX5935 provides input undervoltage lockout, input undervoltage detection, input overvoltage lockout, overtemperature protection, output voltage slew-rate limit during startup, power-good status, and fault status. The MAX5935's programmability includes gate-charging current, current-limit threshold, startup timeout, overcurrent timeout, autorestart duty cycle, PD-disconnect AC-detection threshold, and PD-disconnect detection timeout.

The MAX5935 communicates with the system microcontroller through an I^2C-compatible interface. The MAX5935 features separate input and output data lines (SDAIN and SDAOUT) for use with optocoupler isolation. The MAX5935 is a slave device. Its four address inputs allow 16 unique MAX5935 addresses. A separate $\overline{INT}$ output and four independent shutdown inputs ($\overline{SHD\_}$) allow fast interrupt signals between the MAX5935 and the microcontroller. A $\overline{RESET}$ input allows hardware reset of the device.

Reset

Reset is a condition the MAX5935 enters following any of the following conditions:

- After power-up (V_{EE} and V_{DD} rise above their UVLO thresholds)
- Hardware reset. The $\overline{RESET}$ input is driven low and up high again any time after power-up.
- Software reset. Writing a 1 into R1Ah[4] any time after power-up.
- Thermal shutdown

During a reset, the MAX5935 resets its register map to the Reset state as shown in Table 30 and latches in the state of AUTO (pin 35) and MIDSPAN (pin 2). During normal operation, changes at the AUTO and MIDSPAN inputs are ignored. While the condition that caused the reset persists (i.e., high temperature, $\overline{RESET}$ input low or UVLO conditions), the MAX5935 will not acknowledge any addressing from the serial interface.

Port Reset (R1Ah[3:0])

Set high anytime during normal operation to turn off power and clear the events and status registers of the corresponding port. Port reset only resets the events and status registers.

Operation Modes

The MAX5935 contains four independent but identical state machines to provide reliable and real-time control of the four network ports. Each state machine has four different operating modes: auto, semi-auto, manual, and shutdown. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode, upon request, continuously detects and classifies a device connected to a port but does not power up that port until instructed by software. Manual mode allows total software control of the device and is useful in system diagnostic. Shutdown mode terminates all activities and securely turns off power to the ports. Switching between AUTO, SEMI, or MANUAL mode does not take effect until the part finishes its current task. When the port is set into SHUTDOWN mode, all the port operations are immediately stopped and the port remains idle until SHUTDOWN is exited.

Automatic (AUTO) Mode

Enter automatic (AUTO) mode by forcing the AUTO input high prior to a reset, or by setting R12h[P_M1,P_M0] to [1,1] during normal operation (see Tables 15 and 15a). In AUTO mode, the MAX5935 performs detection and classification, and powers up the port automatically once a valid power device (PD) is detected at the port. If a valid PD is not connected at the port, the MAX5935 repeats the detection routine continuously until a valid PD is connected.

Going into AUTO mode, the DET_EN and CLASS_EN bits are set to high and stay high unless changed by software. Using software to set DET_EN and/or CLASS_EN low causes the MAX5935 to skip detection and/or classification. As a protection, disabling the Detection routine in AUTO mode will not allow the corresponding port to power up, unless the DET_BYP (R23H[4]) is set to 1.

The AUTO status is latched into the register only during a reset. Any changes to the AUTO input after reset is ignored.

Semi-Automatic (SEMI) Mode

Enter semi-automatic (SEMI) mode by setting R12h[P_M1,P_M0] to [1,0] during normal operation (see Tables 15 and 15a). In SEMI mode, the MAX5935, upon request, performs detection and/or classification repeatedly but does not power up the port(s), regardless of the status of the port connection.

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Setting R19h[PWR_ON_] (Table 21) high immediately terminates detection/classification routines and turns on power to the port(s).

R14h[DET_EN_, CLASS_EN_] default to low in SEMI mode. Use software to set R14h[DET_EN_, CLASS_EN_] to high to start the detection and/or classification routines. R14h[DET_EN_, CLASS_EN_] are reset every time the software commands a power-off of the port (either through reset or PWR_OFF). In any other cases, the status of the bits is left unchanged (including when the state machine turns off the power because a load disconnect or a fault condition is encountered).

MANUAL Mode

Enter MANUAL mode by setting R12h[P_M1,P_M0] to [0,1] during normal operation (see Tables 15 and 15a). MANUAL mode allows the software to dictate any sequence of operation. Write a 1 to both R14h[DET_EN_] and R14h[CLASS_EN_] start detection and classification operations, respectively and in that priority order. After execution, the command is cleared from the register(s). PWR_ON_ has highest priority. Setting PWR_ON_ high at any time causes the device to enter the powered mode immediately. Setting DET_EN and CLASS_EN high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ or CLASS_EN_ commands.

When switching to MANUAL mode from another mode, DET_EN_, CLASS_EN_ default to low. These bits become “pushbutton” rather than configuration bits (i.e., writing ones to these bits while in MANUAL mode commands the device to execute one cycle of detection and/or classification. The bits are reset back to zeros at the end of the execution). Putting the MAX5935 into shutdown mode immediately turns off power and halts all operations to the corresponding port. The event and status bits of the affected port(s) are also cleared. In SHUTDOWN mode, the DET_EN, CLASS_EN, and PWR_ON commands are ignored.

In SHUTDOWN mode, the serial interface operates normally.

Watchdog

R1Dh, R1Eh, and R1Fh registers control Watchdog operation. The Watchdog function, when enabled, allows the MAX5935 to gracefully take over control or securely shut down the power to the ports in case of software/firmware crashes. Contact the factory for more details.

PD Detection

When PD detection is activated, the MAX5935 probes the output for a valid PD. After each detection cycle, the device sets the DET_END_ bit R04h/05h[3:0] high and reports the detection results in the status registers R0Ch[2:0], R0Dh[2:0], R0Eh[2:0], and R0Fh[2:0]. The DET_END_ bit is reset to low when read through R05h or after a port reset. Both DET_END_bit status registers are cleared after the port powers down.

A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af standard. Table 1 shows the IEEE 802.3af specification for a PSE detecting a valid PD signature (see the *Typical Application Circuit* and Figure 2). The MAX5935 can probe and categorize different types of devices connected to the port such as a valid PD, an open circuit, a low resistive load, a high resistive load, a high capacitive load, a positive DC supply, or a negative DC supply.

During detection, the MAX5935 turns off the external MOSFET and forces two probe voltages through the DET_ input. The current through the DET_ input is measured as well as the voltage at OUT_. A two-point slope measurement is used as specified by the IEEE 802.3af standard to verify the device connected to the port. The MAX5935 implements appropriate settling times and a 100ms digital integration to reject 50Hz/60Hz powerline noise coupling.

An external diode, in series with the DET_ input, restricts PD detection to the 1st quadrant as specified by the IEEE 802.3af standard. To prevent damage to non-PD devices and to protect itself from an output short circuit, the MAX5935 limits the current into DET_ to less than 2mA maximum during PD detection.

In midspan mode, the MAX5935 waits 2.2s before attempting another detection cycle after every failed detection. The first detection, however, happens immediately after issuing the detection command.

Power Device Classification (PD Classification)

During the PD classification mode, the MAX5935 forces a probe voltage (-18V) at DET_ and measures the current into DET_. The measured current determines the class of the PD.

After each classification cycle, the device sets the CL_END_ bit (R04h/05h[7:4]) high and reports the classification results in the status registers R0Ch[6:4], R0Dh[6:4], R0Eh[6:4], and R0Fh[6:4]. The CL_END_ bit is reset to low when read through register R05h or after a port reset. Both Class_END_bit status registers are cleared after the port powers down.

Table 1. PSE PI Detection Modes Electrical Requirement (Table 33-2 of the IEEE 802.3af Standard)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}	—	30	V	In detection mode only.
Short-Circuit Current	I_{SC}	—	5	mA	In detection mode only.
Valid Test Voltage	V_{VALID}	2.8	10	V	
Voltage Difference Between Test Points	ΔV_{TEST}	1	—	V	
Time Between Any Two Test Points	t_{BP}	2	—	ms	This timing implies a 500Hz maximum probing frequency.
Slew Rate	V_{SLEW}	—	0.1	V/µs	
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	
Open-Circuit Resistance	R_{OPEN}	500	—	kΩ	
Accept Signature Capacitance	C_{GOOD}	—	150	nF	
Reject Signature Capacitance	C_{BAD}	10	—	µF	
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	
Signature Offset Current Tolerance	I_{OS}	0	12	µA	

Table 2. PSE Classification of a PD (Table 33.4 of the IEEE 802.3af Standard)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 and 1
8 to 13	Class 1
> 13 and < 16	May be Class 0, 1, or 2
16 to 21	Class 2
> 21 and < 25	May be Class 0, 2, or 3
25 to 31	Class 3
> 31 and <35	May be Class 0, 3, or 4
35 to 45	Class 4
> 45 and < 51	May be Class 0 or 4

Table 2 shows the IEEE 802.3af requirement for a PSE classifying a PD at the Power Interface (PI).

Powered State

When the part enters PWR MODE, the t_{START} and t_{DISC} timers are reset. Before turning on the power, the part checks if any other port is not turning on and if the t_{FAULT} timer is zero. Another check is performed if the ACD_EN bit is set; in this case, the OSC_FAIL bit must be low (oscillator is okay) for the port to be powered.

If these conditions are met, then the part enters startup where it turns on power to the port. An internal signal, POK_, is asserted high when V_{OUT} is within 2V from V_{EE}. PGOOD_ status bits are set high if POK_ stays high longer than t_{PGOOD}. PGOOD immediately resets when POK goes low.

The PWR_CHG bit sets when a port powers up or down. PWR_EN sets when a port powers up and resets when a port shuts down. The port shutdown timer lasts 0.5ms and prevents other ports from turning off during that period, except in the case of emergency shutdowns ($\overline{RESET}$ = L, RESET_IC = H, V_{EEUVLO}, V_{DDUVLO}, and TSHD).

The MAX5935 always checks the status of all ports before turning off. A priority logic system determines the order to prevent the simultaneous turn-on or turn-off of the ports. The port with the lesser ordinal number gets priority over the others (i.e., Port 1 turns on first, Port 2 second, Port 3 third and Port 4 fourth). Setting PWR_OFF_ high turns off power to the corresponding port.

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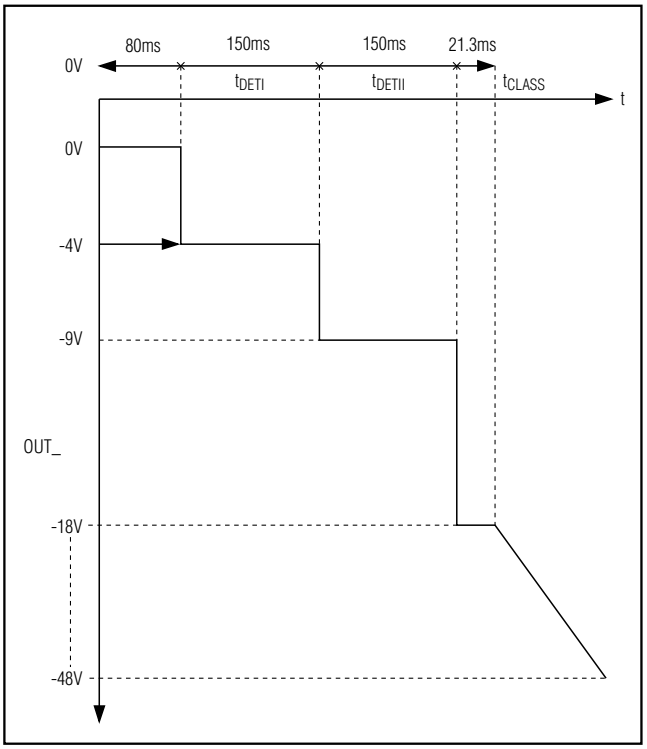

Figure 2. Detection, Classification, and Power-Up Port Sequence

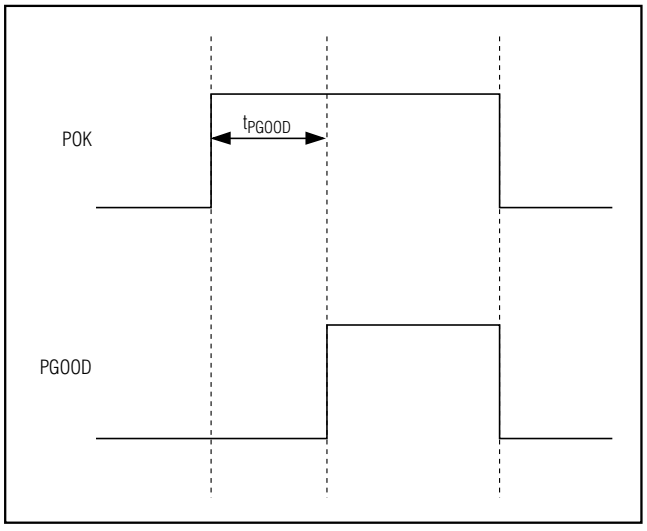

Figure 3. PGOOD Timing

Overcurrent Protection

A sense resistor (R_S), connected between SENSE_ and V_{EE}, monitors the load current. Under all circumstances, the voltage across R_S never exceeds the threshold V_{SU_LIM}. If SENSE_ exceeds V_{SU_LIM}, an internal current-limiting circuit regulates the GATE voltage, limiting the current to $I_{LIM} = V_{SU\_LIM} / R_S$. During transient conditions, if the SENSE_ voltage exceeds V_{SU_LIM}, a fast pulldown circuit activates in order to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, t_{START}, times out, the port shuts off and the STRT_FLT_ bit is set. In the normal powered state, the MAX5935 checks for overcurrent conditions as determined by V_{FLT_LIM} = ~88% of V_{SU_LIM}. The t_{FAULT} counter sets the maximum-allowed continuous overcurrent period. The t_{FAULT} counter increases when V_{SENSE} exceeds V_{FLT_LIM} and decreases at a slower pace when V_{SENSE} drops below V_{FLT_LIM}. A slower decrement for the t_{FAULT} counter allows for detecting repeated short-duration overcurrents. When the counter reaches the t_{FAULT} limit, the MAX5935 powers off the port and asserts the IMAX_FLT_ bit. For a continuous overstress, a fault latches exactly after a period of t_{FAULT}. V_{SU_LIM}, is programmable using R27h[4-7]. t_{FAULT} is programmable using R16h[2-3] and R28[4-7].

After power-off due to an overcurrent fault, and if the RSTR_EN bit is set, the t_{FAULT} timer is not immediately reset but starts decrementing at the same slower pace. The MAX5935 allows the port to be powered on only when the t_{FAULT} counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET to avoid overheating. The duty cycle is programmable using R16h[6-7].

The MAX5935 continuously flags when the current exceeds the maximum current allowed for the class as indicated in the CLASS status register. When class overcurrent occurs, the MAX5935 sets the IVC bit in register R09h.

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUT_ and reduces the current-limit value when ($V_{OUT\_}$ - V_{EE}) > 30V. The foldback function helps to reduce the power dissipation on the FET. The current limit eventually reduces to 1/3 of I_{LIM} when ($V_{OUT\_}$ - V_{EE}) > 50V (see Figure 4).

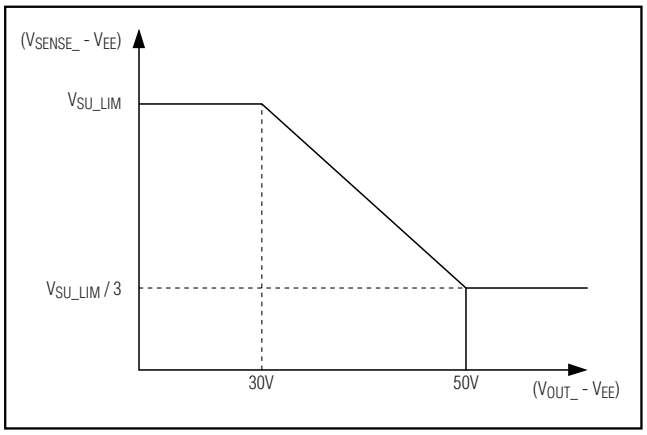

Figure 4. Foldback Current Characteristics

MOSFET Gate Driver

Connect the gate of the external n-channel MOSFET to GATE_. An internal 50µA current source pulls GATE_ to (V_{EE} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE_ to V_{EE} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. The pullup current (gate-charging current) is programmable using R23h[5-7]. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GD}}$$

where C_{GD} is the total capacitance between GATE and DRAIN of the external FET. Current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the MAX5935 manipulates the GATE_ voltage to control the voltage at SENSE_. A fast pulldown activates if SENSE_ overshoots the limit threshold. The fast pulldown current increases with the amount of overshoot. The maximum fast pulldown current is 100mA.

During turn-off when the GATE voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the FET securely off.

Digital Logic

V_{DD} supplies power for the internal logic circuitry. V_{DD} ranges from +1.71V to +3.7V and determines the logic thresholds for the CMOS connections (SDAIN, SDAOUT, SCL, AUTO, $\overline{SHD}$_, A_). This voltage range enables the MAX5935 to interface with a nonisolated low-voltage microcontroller. The MAX5935 checks the digital supply for compatibility with the internal logic. The MAX5935 also features a V_{DD} undervoltage lockout (V_{DDUVLO}) of +1.35V. A V_{DDUVLO} condition keeps the MAX5935 in reset and the ports shut off. Bit 0 in the supply event register shows the status of V_{DDUVLO} (Table 11) after V_{DD} has recovered. All logic inputs and outputs reference to DGND. DGND and AGND are completely isolated internally to the MAX5935. In a completely isolated system, the digital signal can be referenced indifferently to V_{AGND} or V_{EE} or at voltages even higher than AGND (up to 60V). V_{DD} - V_{DGND} must be greater than 3.0V when $V_{DGND} \le (V_{EE} + 3.0V)$

When using the AC disconnect-detection feature, AGND must be connected directly to DGND and V_{DD} must be greater than +3V. In this configuration, connect DGND to AGND at a single point in the system as close to MAX5935 as possible.

Hardware Shutdown

$\overline{SHD}$_ shuts down the respective ports without using the serial interface. Hardware shutdown offers an emergency turn-off feature that allows a fast disconnect of the power supply from the port. Pull $\overline{SHD}$_ low to remove power.

Interrupt

The MAX5935 contains an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. R00h and R01h (Tables 5 and 6) contain the definitions of the interrupt registers. The mask register R01h determines events that trigger an interrupt. As a response to an interrupt, the controller reads the status of the event register to determine the cause of the interrupt and takes subsequent actions. Each interrupt event register also contains a clear-on-read (CoR) register. Reading through the CoR register address clears the interrupt. $\overline{INT}$ remains low when reading the interrupt through the read-only addresses. For example, to clear a startup fault on port 4 read address 09h (see Table 10). Use the global pushbutton bit on register 1Ah (bit 7, Table 22) to clear interrupts, or use a software or hardware reset.

Undervoltage and Overvoltage Protection

The MAX5935 contains several undervoltage and overvoltage protection features. Table 11 in the *Register Map and Description* section shows a detailed list of the undervoltage and overvoltage protection features. An internal V_{EE} undervoltage-lockout (V_{EEUVLO}) circuit keeps the MOSFET off and the MAX5935 in reset until V_{AGND} - V_{EE} exceeds 29V for more than 3ms. An internal V_{EE} overvoltage (V_{EE_OV}) circuit shuts down the ports when (V_{AGND} - V_{EE}) exceeds 60V. The digital supply also contains an undervoltage lockout (V_{DDUVLO}).

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The MAX5935 also features three other undervoltage and overvoltage interrupts: V_{EE} undervoltage interrupt (V_{EEUV}), V_{DD} undervoltage interrupt (V_{DDUV}), and V_{DD} overvoltage interrupt (V_{DDOV}). A fault latches into the supply events register (Table 11), but the MAX5935 does not shut down the ports with a V_{EEUV}, V_{DDUV}, or V_{DDOV}.

DC Disconnect Monitoring

Setting R13h[DCD_EN_] bits high enables DC load monitoring during normal powered state. If SENSE_ falls below the DC load disconnect threshold, V_{DCTH}, for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port. t_{DISC} is programmable using R16h[0-1] and R27h[0-3].

AC Disconnect Monitoring

The MAX5935 features AC load disconnect monitoring. Connect an external sine wave to OSC_IN. The oscillator requirements are:

- Frequency x V_{P-P} = 200V_{P-P} x Hz ±15%
- Positive peak voltage > +2V
- Frequency > 60Hz
- A 100Hz ±10%, 2V_{P-P} ±5%, with +1.2V offset (V_{PEAK} = +2.2V, typ) is recommended.

The MAX5935 buffers and amplifies 3x the external oscillator signal and sends the signal to DET_, where the sine wave is AC-coupled to the output. The MAX5935 senses the presence of the load by monitoring the amplitude of the AC current returned to DET_ (see the *Functional Diagram*).

Setting R13h[ACD_EN_] bits high enable AC load disconnect monitoring during the normal powered state. If the AC current peak at the DET_ pin falls below I_{ACTH} for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port. I_{ACTH} is programmable using R23h[0-3].

An internal comparator checks for a proper amplitude of the oscillator input. If the positive peak of the input sinusoid falls below a safety value of 2V, OSC_FAIL sets and the port shuts down. Power cannot be applied to the ports when ACD_EN is set high and OSC_FAIL is set high. Leave OSC_IN unconnected or connect it to DGND when not using AC disconnect detection.

When using the AC disconnect detection feature, connect AGND directly to DNGD as close as possible to the IC. The MAX5935 also requires a V_{DD} of greater than +3V for this function. See the *Typical Application Circuit* with AC disconnect for other external component requirements.

Table 3. MAX5935 Address

0	1	0	A3	A2	A1	A0	R/W

Thermal Shutdown

If the MAX5935 die temperature reaches +150°C, an overtemperature fault generates and the MAX5935 shuts down and the MOSFETs turn off. The die temperature of the MAX5935 must cool down below +130°C to remove the overtemperature fault condition. After a thermal shutdown, the part is reset.

Address Inputs

A3, A2, A1, and A0 represent the four LSBs of the chip address, the complete seven bits chip address (see Table 3).

The four LSBs latch on the low-to-high transition of $\overline{RESET}$ or after a power-supply start (either on V_{DD} or V_{EE}). Address inputs default high through an internal 50kΩ pullup resistor to V_{DD}. The MAX5935 also responds to the call through a global address 60h (see the *Global Addressing and Alert Response Protocol* section).

I²C-Compatible Serial Interface

The MAX5935 operates as a slave that sends and receives data through an I²C-compatible, 2-wire or 3-wire interface. The interface uses a serial data input line (SDAIN), a serial data output line (SDAOUT) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5935, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial data line (SDA).

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The MAX5935 SDAIN line operates as input. The MAX5935 SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDAOUT. The MAX5935 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

Serial Addressing

Each transmission consists of a START condition (Figure 7) sent by a master, followed by the MAX5935 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

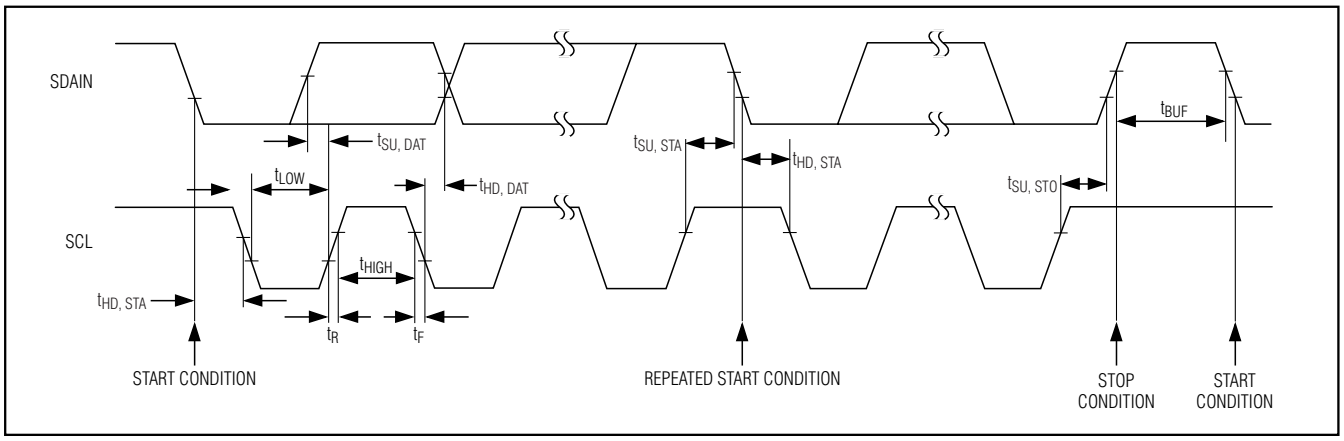

Figure 5. 2-Wire Serial Interface Timing Details

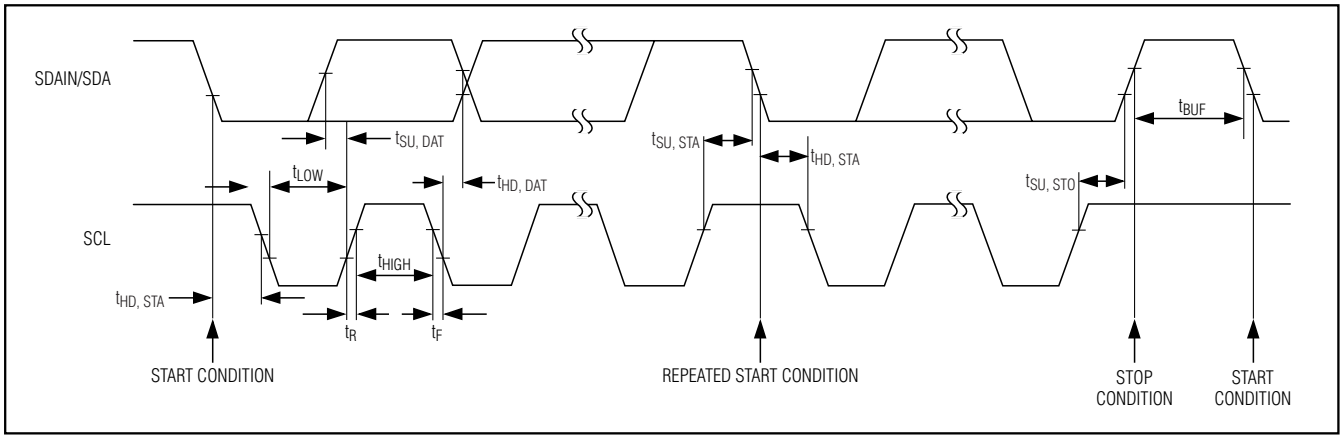

Figure 6. 3-Wire Serial Interface Timing Details

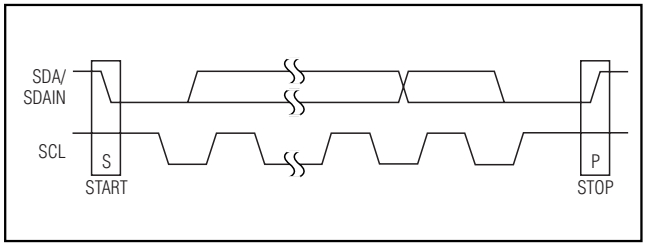

Figure 7. Start and Stop Conditions

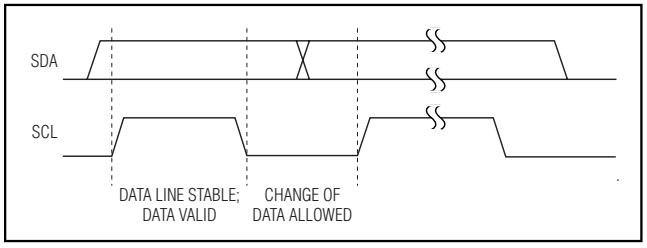

Figure 8. Bit Transfer

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The stop condition frees the bus for another transmission.

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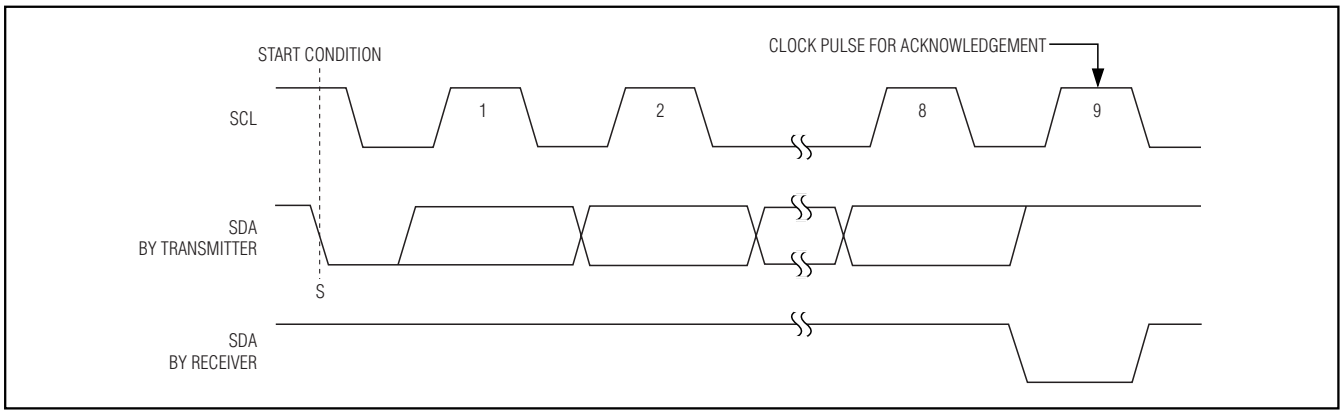

Figure 9. Acknowledge

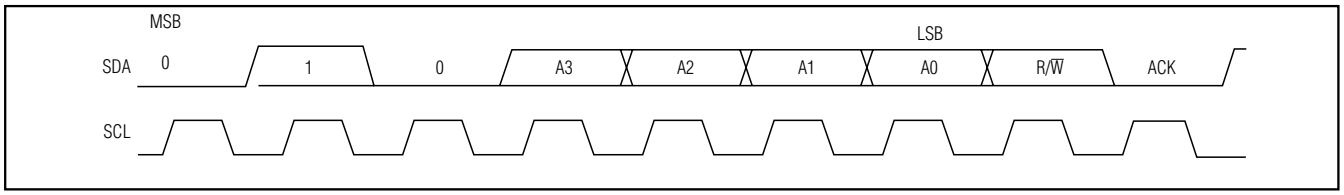

Figure 10. Slave Address

Bit Transfer

Each clock pulse transfers one data bit (Figure 8). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 9), which the recipient uses as a handshake receipt of each byte of data. Thus, each byte effectively transferred requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA (or the SDAOUT in the 3-wire interface) during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5935, the MAX5935 generates the acknowledge bit. When the MAX5935 transmits to the master, the master generates the acknowledge bit.

Slave Address

The MAX5935 has a 7-bit long slave address (Figure 10). The bit following the 7-bit slave address (bit eight) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

010 always represent the first three bits (MSBs) of the MAX5935 slave address. Slave address bits A3, A2, A1, and A0 represent the states of the MAX5935's A3, A2, A1, and A0 inputs, allowing up to sixteen MAX5935 devices to share the bus. The states of the A3, A2, A1, and A0 latch in upon the reset of the MAX5935 into register R11h. The MAX5935 monitors the bus continuously, waiting for a START condition followed by the MAX5935's slave address. When the MAX5935 recognizes its slave address, it acknowledges and is then ready for continued communication.

Global Addressing and Alert Response Protocol

The global address call is used in writing mode to write the same register to multiple devices (address 0x60). In read mode (address 0x61), the global address call is used as the Alert Response address. When responding to a global call, the MAX5935 puts out on the data line its own address whenever its interrupt is active and so does every other device connected to the SDAOUT line that has an active interrupt. After every bit is transmitted, the MAX5935 checks that the data line effectively corresponds to the data it is delivering. If it is not, it then backs off and frees the data line. This litigation protocol always allows the part with the lowest address to complete the transmission. The microcontroller can then respond to the interrupt and take proper actions. The MAX5935 does not reset its own interrupt at the end of the Alert Response protocol. The microcontroller has to do it by clearing the event register through their CoR addresses or activating the CLR_INT pushbutton.

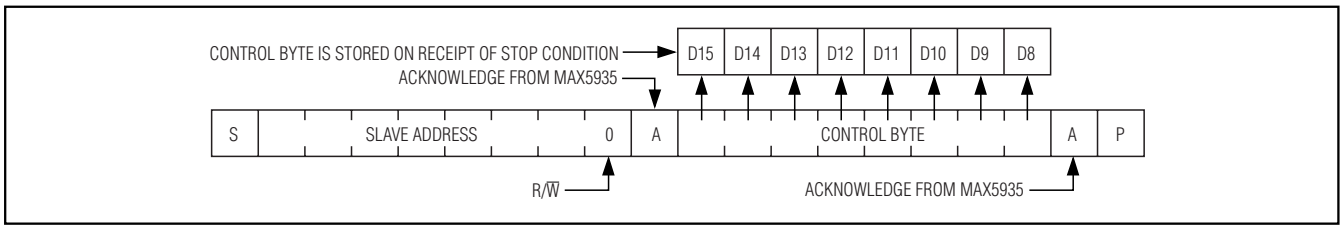

Figure 11. Control Byte Received

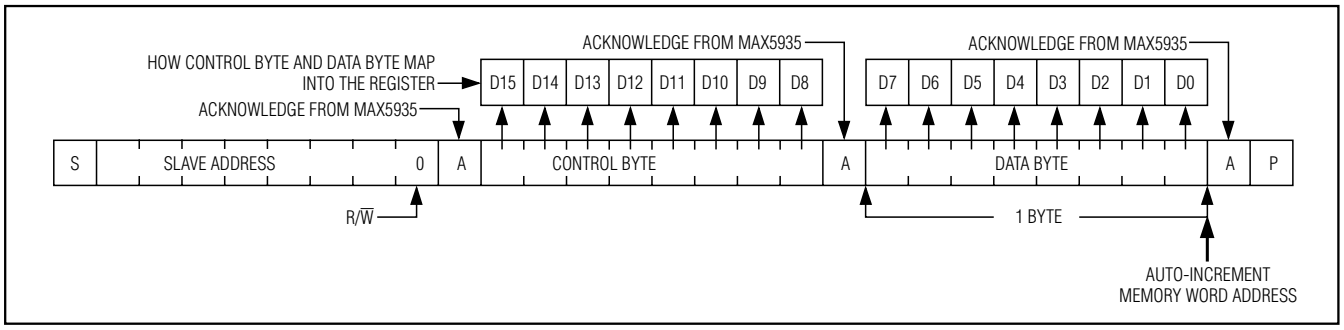

Figure 12. Control and Single Data Byte Received

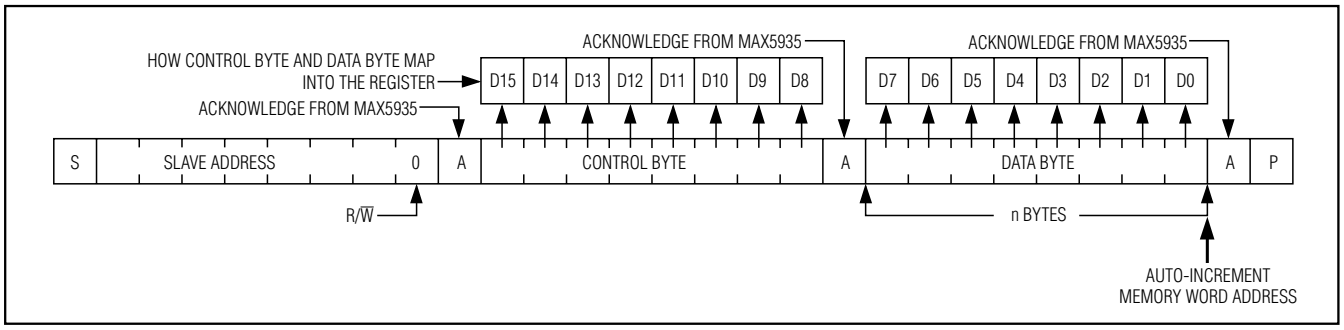

Figure 13. 'n' Data Bytes Received

Message Format for Writing the MAX5935

A write to the MAX5935 comprises of the MAX5935's slave address transmission with the R/W bit set to 0, followed by at least one byte of information. The first byte of information is the command byte (Figure 11). The command byte determines which register of the MAX5935 is written to by the next byte, if received. If the MAX5935 detects a STOP condition after receiving the command byte, then the MAX5935 takes no further action beyond storing the command byte. Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX5935 selected by the command byte. If the MAX5935 transmits multiple data bytes before the MAX5935 detects a STOP condition, these bytes store in subsequent MAX5935 internal registers because the control byte address auto-increments.

Any bytes received after the control byte are data bytes. The first data byte goes into the internal register of the MAX5935 selected by the control byte (Figure 8).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are stored in subsequent MAX5935 internal registers because the control byte address auto-increments.

Table 4. Auto-Increment Rules

COMMAND BYTE ADDRESS RANGE	AUTO-INCREMENT BEHAVIOR
0x00 to 0x26	Command address will auto-increment after byte read or written
0x26	Command address remains at 0x26 after byte written or read

Message Format for Reading

The MAX5935 reads using the MAX5935's internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer auto-increments after reading each data byte using the same rules as for a write. Thus, a read is initiated by first configuring the MAX5935's command byte by performing a write (Figure 12). The master now reads "n" consecutive bytes from the MAX5935, with the first data byte read from the register addressed by the initialized command byte (Figure 13). When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address auto-increments after the write.

Operation with Multiple Masters

When the MAX5935 operates on a 2-wire interface with multiple masters, a master reading the MAX5935 should use repeated starts between the write that sets the MAX5935's address pointer, and the read(s) that takes the data from the location(s). It is possible for master 2 to take over the bus after master 1 has set up the MAX5935's address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX5935's address pointer, then master 1's read may be from an unexpected location.

Command Address Auto-Incrementing

Address auto-incrementing allows the MAX5935 to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX5935 generally increments after each data byte is written or read (Table 4). The MAX5935 is designed to prevent overwrites on unavailable register addresses and unintentional wraparound of addresses.

Register Map And Description

The interrupt register (Table 5) summarizes the event register status and is used to send an interrupt signal ($\overline{INT}$ goes low) to the controller. Writing a 1 to R1Ah[7] clears all interrupt and events registers. A Reset sets R00h to 00h.

INT_EN (R17h[7]) is a global interrupt mask (Table 6). The MASK_ bits activate the corresponding interrupt bits in register R00h. Writing a 0 to INT_EN (R17h[7]) disables the $\overline{INT}$ output.

A Reset sets R01h to AAA00A00b, where A is the state of the AUTO input prior to the reset.

The power event register (Table 7) records changes in the power status of the four ports. Any change in PGOOD_ (R10h[7:4]) sets PG_CHG_ to 1. Any change in the PWR_EN_ (R10h[3:0]) sets PWEN_CHG_ to 1. PG_CHG_ and PWEN_CHG_ trigger on the edges of PGOOD_ and PWR_EN_ and do not depend on the actual level of the bits. The power event register has two addresses. When read through the R02h address, the content of the register is left unchanged. When read through the CoR R03h address, the register content will be cleared. A Reset sets R02h/R03h = 00h.

DET_END_/CL_END_ is set high whenever detection/classification is completed on the corresponding port. A 1 in any of the CL_END_ bits forces R00h[4] to 1. A 1 in any of the DET_END_ bits forces R00h[3] to 1. As with any of the other events register, the detect event register (Table 8) has two addresses. When read through the R04h address, the content of the register is left unchanged. When read through the CoR R05h address, the register content will be cleared. A Reset sets R04h/R05h = 00h.

LD_DISC_ is set high whenever the corresponding port shuts down due to detection of load removal. IMAX_FLT_ is set high when the port shuts down due to an extended overcurrent event after a successful start-up. A 1 in any of the LD_DISC_ bits forces R00h[2] to 1. A 1 in any of the IMAX_FLT_ bits forces R00h[5] to 1. As with any of the other events registers, the fault event register (Table 9) has two addresses. When read through the R06h address, the content of the register is left unchanged. When read through the CoR R07h address, the register content will be cleared. A reset sets R06h/R07h = 00h.

If the port remains in current limit or the PGOOD condition is not met at the end of the startup period, the port shuts down and the corresponding STRT_FLT_ is set to 1. A 1 in any of the STRT_FLT_ bits forces R00h[6] to 1. IVC_ is set to 1 whenever the port current exceeds the maximum allowed limit for the class (determined during the classification process). A 1 in any of IVC_ forces R00h[6] to 1. When the CL_DISC (R17h[2]) is set to 1, the port will also limit the load current according to its class as specified in the *Electrical Characteristics* table. As with any of the other events registers, the startup event register (Table 10) has two addresses. When

Table 5. Interrupt Register

ADDRESS = 00h			DESCRIPTION
SYMBOL	BIT	R/W	
SUP_FLT	7	R	Interrupt signal for supply faults. SUP_FLT is the logic OR of all the bits [7:0] in register R0Ah/R0Bh (Table 8).
TSTR_FLT	6	R	Interrupt signal for startup failures. TSRT_FLT is the logic OR of bits [7:0] in register R08h/R09h (Table 7).
IMAX_FLT	5	R	Interrupt signal for current-limit violations. IMAX_FLT is the logic OR of bits [3:0] in register R06h/R07h (Table 6).
CL_END	4	R	Interrupt signal for completion of classification. CL_END is the logic OR of bits [7:4] in register R04h/R05h (Table 5).
DET_END	3	R	Interrupt signal for completion of detection. DET_END is the logic OR of bits [3:0] in register R04h/R05h (Table 5).
LD_DISC	2	R	Interrupt signal for load disconnection. LD_DISC is the logic OR of bits [7:4] in register R06h/R07h (Table 6).
PG_INT	1	R	Interrupt signal for PGOOD status change. PG_INT is the logic OR of bits [7:4] in register R02h/R03h (Table 4).
PE_INT	0	R	Interrupt signal for power-enable status change. PEN_INT is the logic OR of bits [3:0] in register R02h/R03h (Table 4).

Table 6. Interrupt Mask Register

ADDRESS = 01h			DESCRIPTION
SYMBOL	BIT	R/W	
MASK7	7	R/W	Interrupt mask bit 7. A logic high enables the SUP_FLT interrupts. A logic low disables the SUP_FLT interrupts.
MASK6	6	R/W	Interrupt mask bit 6. A logic high enables the TSTR_FLT interrupts. A low disables the TSTR_FLT interrupts.
MASK5	5	R/W	Interrupt mask bit 5. A logic high enables the IMAX_FLT interrupts. A logic low disables the IMAX_FLT interrupts.
MASK4	4	R/W	Interrupt mask bit 4. A logic high enables the CL_END interrupts. A logic low disables the CL_END interrupts.
MASK3	3	R/W	Interrupt mask bit 3. A logic high enables the DET_END interrupts. A logic low disables the DET_END interrupts.
MASK2	2	R/W	Interrupt mask bit 2. A logic high enables the LD_DISC interrupts. A logic low disables the LD_DISC interrupts.
MASK1	1	R/W	Interrupt mask bit 1. A logic high enables the PG_INT interrupts. A logic low disables the PG_INT interrupts.
MASK0	0	R/W	Interrupt mask bit 0. A logic high enables the PEN_INT interrupts. A logic low disables the PEN_INT interrupts.

Table 7. Power Event Register

ADDRESS =		02h	03h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
PG_CHG4	7	R	CoR	PGOOD change event for port 4
PG_CHG3	6	R	CoR	PGOOD change event for port 3
PG_CHG2	5	R	CoR	PGOOD change event for port 2
PG_CHG1	4	R	CoR	PGOOD change event for port 1
PWEN_CHG4	3	R	CoR	Power enable change event for port 4
PWEN_CHG3	2	R	CoR	Power enable change event for port 3
PWEN_CHG2	1	R	CoR	Power enable change event for port 2
PWEN_CHG1	0	R	CoR	Power enable change event for port 1

Table 8. Detect Event Register

ADDRESS =		04h	05h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
CL_END4	7	R	CoR	Classification completed on port 4
CL_END3	6	R	CoR	Classification completed on port 3
CL_END2	5	R	CoR	Classification completed on port 2
CL_END1	4	R	CoR	Classification completed on port 1
DET_END4	3	R	CoR	Detection completed on port 4
DET_END3	2	R	CoR	Detection completed on port 3
DET_END2	1	R	CoR	Detection completed on port 2
DET_END1	0	R	CoR	Detection completed on port 1

Table 9. Fault Event Register

ADDRESS =		06h	07h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
LD_DISC4	7	R	CoR	Disconnect on port 4
LD_DISC3	6	R	CoR	Disconnect on port 3
LD_DISC2	5	R	CoR	Disconnect on port 2
LD_DISC1	4	R	CoR	Disconnect on port 1
IMAX_FLT4	3	R	CoR	Overcurrent on port 4
IMAX_FLT3	2	R	CoR	Overcurrent on port 3
IMAX_FLT2	1	R	CoR	Overcurrent on port 2
IMAX_FLT1	0	R	CoR	Overcurrent on port 1

Table 10. Startup Event Register

ADDRESS =		08h	09h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
IVC4	7	R	CoR	Class overcurrent flag for port 4
IVC3	6	R	CoR	Class overcurrent flag for port 3
IVC2	5	R	CoR	Class overcurrent flag for port 2
IVC1	4	R	CoR	Class overcurrent flag for port 1
STRT_FLT4	3	R	CoR	Startup failed on port 4
STRT_FLT3	2	R	CoR	Startup failed on port 3
STRT_FLT2	1	R	CoR	Startup failed on port 2
STRT_FLT1	0	R	CoR	Startup failed on port 1

Table 11. Supply Event Register

ADDRESS =		0Ah	0Bh	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
TSD	7	R	CoR	Overtemperature shutdown
V_{DD_OV}	6	R	CoR	V_{DD} overvoltage condition
V_{DD_UV}	5	R	CoR	V_{DD} undervoltage condition
V_{EE_UVLO}	4	R	CoR	V_{EE} undervoltage-lockout condition
V_{EE_OV}	3	R	CoR	V_{EE} overvoltage condition
V_{EE_UV}	2	R	CoR	V_{EE} undervoltage condition
OSC_FAIL	1	R	CoR	Oscillator amplitude is below limit
V_{DD_UVLO}	0	R	CoR	V_{DD} undervoltage-lockout condition

Table 12. Port Status Registers

ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	R	Reserved
CLASS_	6	R	CLASS_[2]
	5	R	CLASS_[1]
	4	R	CLASS_[0]
Reserved	3	R	Reserved
DET_ST_	2	R	DET_[2]
	1	R	DET_[1]
	0	R	DET_[0]

read through the R08h address, the content of the register is left unchanged. When read through the CoR R09h address, the register content will be cleared. A reset sets R08h/R09h = 00h.

The MAX5935 continuously monitors the power supplies and sets the appropriate bits in the supply event register (Table 11). V_{DD_OV}/V_{EE_OV} is set to 1 whenever V_{DD}/V_{EE} exceeds its overvoltage threshold. V_{DD_UV}/V_{EE_UV} is set to 1 whenever V_{DD}/V_{EE} falls below its undervoltage threshold.

OSC_FAIL is set to 1 whenever the amplitude of the oscillator signal at the OSC_input falls below a level that might compromise the AC disconnect detection function. OSC_FAIL generates an interrupt only if at least one of the ACD_EN (R13h[7:4]) bit is set high.

A thermal shutdown circuit monitors the temperature of the die and resets the MAX5935 if the temperature exceeds +150°C. TSD is set to 1 after the MAX5935 returns to normal operation. TSD is also set to 1 after every UVLO reset.

When V_{DD} and/or $|V_{EE}|$ is below its undervoltage-lockout (UVLO) threshold, the MAX5935 is in Reset mode and securely holds all ports off. When V_{DD} and $|V_{EE}|$ rise to above their respective UVLO thresholds, the device comes out of reset as soon as the last supply

Table 12a. Detection Result Decoding Chart

DET_ST_[2:0]	DETECTED	DESCRIPTION
000	None	Detection status unknown.
001	DCP	Positive DC supply connected at the port (AGND - $V_{OUT\_}$ < 1.65V).
010	HIGH CAP	High capacitance at the port (>5µF).
011	RLOW	Low resistance at the port. R_{PD} < 17kΩ.
100	DET_OK	Detection pass. 17kΩ > R_{PD} > 28kΩ.
101	RHIGH	High resistance at the port. R_{PD} > 28kΩ.
110	OPEN0	Open port (I < 12.5µA).
111	DCN	Negative DC supply connected to the port (V_{OUT} - V_{EE} < 2V).

Table 12b. Classification Result Decoding Chart

CLASS_[2:0]	CLASS RESULT
000	Unknown
001	1
010	2
011	3
100	4
101	Undefined (treated as CLASS 0)
110	0
111	Current limit (>I_{CILIM})

crosses the UVLO threshold. The last supply corresponding UV and UVLO bits in the supply event register will be set to 1.

A 1 in any supply event register's bits forces R00h[7] to 1. As with any of the other events register, the supply event register has two addresses. When read through the R0Ah address, the content of the register is left unchanged. When read through the CoR R0Bh address, the register content will be cleared. A reset sets R0Ah/R0Bh to 00100001 if V_{DD} comes up after V_{EE} or to 00010100 if V_{EE} comes up after V_{DD}.

The port status register (Table 12) records the results of the detection and classification at the end of each phase in three encoding bits each. R0Ch contains detection and classification status of port 1. R0Dh corresponds to port 2, R0Eh corresponds to port 3, and R0Fh corresponds to port 4. Tables 12a and 12b show the detection/classification result decoding charts, respectively.

As a protection, when POFF_CL (R17h[3], Table 20) is set to 1, the MAX5935 prohibits turning on power to the port that returns a status 111 after classification. A reset sets 0Ch, 0Dh, 0Eh, and 0Fh = 00h.

PGOOD_ is set to 1 (Table 13) at the end of the power-up startup period if the power-good condition is met (0 < (V_{OUT} - V_{EE}) < PG_{TH}). The power-good condition must remain valid for more than t_{PGOOD} to assert PGOOD_. PGOOD_ is reset to 0 whenever the output falls out of the power-good condition. A fault condition immediately forces PGOOD_ low.

PWR_EN_ is set to 1 when the port power is turned on. PWR_EN resets to 0 as soon as the port turns off. Any transition of PGOOD_ and PWR_EN_ bits set the corresponding bit in the power event registers R02h/R03h (Table 7). A reset sets R10h = 00h.

A3, A2, A1, and A0 (Table 14) represent the four LSBs of the MAX5935 address (Table 3). During a reset, the devices latch into R11h. These four bits address from the corresponding inputs as well as the state of the MIDSPAN and AUTO inputs. Changes to those inputs during normal operation are ignored.

The MAX5935 uses two bits for each port to set the mode of operation (Table 15). Set the modes according to Table 15a.

A reset sets R12h = AAAAAAAA where A represents the latched-in state of the AUTO input prior to the reset. Use software to change the mode of operation. Software resets of ports (RESET_P_ bit, Table 22) do not affect the mode register.

Setting DCD_EN_ to 1 enables the DC load disconnect detection feature (Table 16). Setting ACD_EN_ to 1 enables the AC load disconnect feature. If enabled, the load disconnect detection starts during power mode and after startup when the corresponding PGOOD_ bit in register R10h (Table 13) goes high. A reset sets R13h = 0000AAAA, where A represents the latched-in state of the AUTO input prior to the reset.

Table 13. Power Status Register

ADDRESS = 10h			DESCRIPTION
SYMBOL	BIT	R/W	
PGOOD4	7	R	Power-good condition on Port 4
PGOOD3	6	R	Power-good condition on Port 3
PGOOD2	5	R	Power-good condition on Port 2
PGOOD1	4	R	Power-good condition on Port 1
PWR_EN4	3	R	Power is enabled on Port 4
PWR_EN3	2	R	Power is enabled on Port 3
PWR_EN2	1	R	Power is enabled on Port 2
PWR_EN1	0	R	Power is enabled on Port 1

Table 14. Address Input Status Register

ADDRESS = 11h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	R	Reserved
Reserved	6	R	Reserved
A3	5	R	Device address, A3 pin latched in status
A2	4	R	Device address, A2 pin latched in status
A1	3	R	Device address, A1 pin latched in status
A0	2	R	Device address, A0 pin latched in status
MIDSPAN	1	R	MIDSPAN inputs latched in status
AUTO	0	R	AUTO input's latched-in status

Table 15. Mode Register

ADDRESS = 12h			DESCRIPTION
SYMBOL	BIT	R/W	
P4_M1	7	R/W	M0DE[1] for port 4
P4_M0	6	R/W	M0DE[0] for port 4
P3_M1	5	R/W	M0DE[1] for port 3
P3_M0	4	R/W	M0DE[0] for port 3
P2_M1	3	R/W	M0DE[1] for port 2
P2_M0	2	R/W	M0DE[0] for port 2
P1_M1	1	R/W	M0DE[1] for port 1
P1_M0	0	R/W	M0DE[0] for port 1

Setting DET_EN_/CLASS_EN_ to 1 (Table 17) enables load detection/classification, respectively. Detection always has priority over classification. To perform classification without detection, set the DET_EN_ bit low and CLASS_EN_ bit high.

In MANUAL mode, R14h works like a pushbutton. Set the bits high to begin the corresponding routine. The bit clears after the routine finishes.

When entering AUTO mode, R14h defaults to FFh. When entering MANUAL mode, R14h defaults to 00h. When entering SEMI mode, R1h is left unchanged but is reset every time the software commands power off the port. A reset or power-up sets R14h = AAAAAAAAb, where A represents the latched-in state of the AUTO input prior to the reset.

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Setting BCKOFF_ to 1 (Table 18) enables cadence timing on each port, where the port backs off and waits 2.2s after each failed load discovery detection. The IEEE 802.3af standard requires a PSE that delivers power through the spare pairs (midspan PSE) to have cadence timing. A reset sets R14h = 0000XXXX, where X is the logic AND of the MIDSPAN and AUTO input state prior to a reset. BCKOFF_ can be changed by software at any time while changes to the MIDSPAN and AUTO input state during normal operation are ignored.

Table 15a. Mode Status

MODE	DESCRIPTION
00	Shutdown
01	MANUAL
10	Semi AUTO
11	AUTO

TSTART[1,0] (Table 19) programs the startup timers. Startup time is the time the port is allowed to be in current limit during startup. TFAULT_[1,0] programs the fault time. Fault time is the time allowable for the port to be in current limit during normal operation. RSTR[1,0] programs the discharge rate of the TFAULT_ counter and effectively sets the time the port remains off after an overcurrent fault. TDISC[1,0] programs the load disconnect detection time. The device turns off power to the port if it fails to provide a minimum power maintenance signal for longer than the load disconnect detection time (TDISC).

Set the bits in R16h to scale the TSTART, TFAULT, and TDISC to a multiple of their nominal value specified in the *Electrical Characteristics* table. R27h and R28h further extend the programming range of these timers and also increase the programming resolution.

When the MAX5935 shuts down a port due to an extended overcurrent condition (either during startup or normal operation), if RSRT_EN is set high, then the part does not allow the port to power back on before the restart timer (Table 19a) returns to zero. This effectively

Table 16. Load Disconnect Detection Enable Register

ADDRESS = 13h			DESCRIPTION
SYMBOL	BIT	R/W	
ACD_EN4	7	R/W	Enable AC disconnect detection on port 4
ACD_EN3	6	R/W	Enable AC disconnect detection on port 3
ACD_EN2	5	R/W	Enable AC disconnect detection on port 2
ACD_EN1	4	R/W	Enable AC disconnect detection on port 1
DCD_EN4	3	R/W	Enable DC disconnect detection on port 4
DCD_EN3	2	R/W	Enable DC disconnect detection on port 3
DCD_EN2	1	R/W	Enable DC disconnect detection on port 2
DCD_EN1	0	R/W	Enable DC disconnect detection on port 1

Table 17. Detection and Classification Enable Register

ADDRESS = 14h			DESCRIPTION
SYMBOL	BIT	R/W	
CLASS_EN4	7	R/W	Enable classification on port 4
CLASS_EN3	6	R/W	Enable classification on port 3
CLASS_EN4	5	R/W	Enable classification on port 2
CLASS_EN3	4	R/W	Enable classification on port 1
DET_EN4	3	R/W	Enable detection on port 4
DET_EN3	2	R/W	Enable detection on port 3
DET_EN2	1	R/W	Enable detection on port 2
DET_EN1	0	R/W	Enable detection on port 1

Table 18. Backoff Enable Register

ADDRESS = 15h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	R	Reserved
Reserved	6	R	Reserved
Reserved	5	R	Reserved
Reserved	4	R	Reserved
BCKOFF4	3	R/W	Enable Cadence timing on Port 4
BCKOFF3	2	R/W	Enable Cadence timing on Port 3
BCKOFF2	1	R/W	Enable Cadence timing on Port 2
BCKOFF1	0	R/W	Enable Cadence timing on Port 1

Table 19. Timing Register

ADDRESS = 16h			DESCRIPTION
SYMBOL	BIT	R/W	
RSTR[1]	7	R/W	Restart timer programming bit 1
RSTR[0]	6	R/W	Restart timer programming bit 0
TSTART[1]	5	R/W	Startup timer programming bit 1
TSTART[0]	4	R/W	Startup timer programming bit 0
TFAULT[1]	3	R/W	Overcurrent timer programming bit 1
TFAULT[0]	2	R/W	Overcurrent timer programming bit 0
TDISC[1]	1	R/W	Load disconnect timer programming bit 1
TDISC[0]	0	R/W	Load disconnect timer programming bit 0

Table 19a. Startup, Fault, and Load Disconnect Timers with Default Values in the Register 27h and 28h

Bit[1:0]	RSTR	t_{DISC}	t_{START}	t_{FAULT}
00	16 x t_{FAULT}	t_{DISC} nominal (350ms, typ)	t_{START} nominal (60ms, typ)	t_{FAULT} nominal (60ms, typ)
01	32 x t_{FAULT}	1/4 x t_{DISC} nominal	1/2 x t_{START} nominal	1/2 x t_{FAULT} nominal
10	64 x t_{FAULT}	1/2 x t_{DISC} nominal	2 x t_{START} nominal	2 x t_{FAULT} nominal
11	0 x t_{FAULT}	2 x t_{DISC} nominal	4 x t_{START} nominal	4 x t_{FAULT} nominal

sets a minimum duty cycle that protects the external MOSFET from overheating during prolonged output overcurrent conditions.

A reset sets R16h = 00h.

Setting CL_DISC to 1 (Table 20) enables port-over-class current protection, where the MAX5935 scales down the overcurrent limit (V_{FLT_LIM}) according to the port classification status. This feature provides protection to the system against PDs that violate their maximum class current allowance.

A reset sets R17h = 0xC0.

Power-enable “pushbutton” (Table 21) for SEMI and MANUAL modes. Setting PWR_ON_ to 1 turns on power to the corresponding port. Setting PWR_OFF_ to 1 turns off power to the port. PWR_ON is ignored when the port is already powered and during shutdown. PWR_OFF is ignored when the port is already off and during shutdown. After execution, the bits reset to 0. During detection or classification if PWR_ON_ goes high, the MAX5935 gracefully terminates the current operation and turn-on power to the port. The MAX5935 ignores the PWR_ON_ in AUTO mode. A reset sets R19h = 00h.

Table 20. Miscellaneous Configurations

ADDRESS = 17h			DESCRIPTION
SYMBOL	BIT	R/W	
INT_EN	7	R/W	A logic high enables $\overline{INT}$ functionality
RSTR_EN	6	R	A logic high enables the auto-restart protection time off (as set by the RSRT[1:0] bits)
Reserved	5	R	Reserved
Reserved	4	R	Reserved
POFF_CL	3	R	A logic high prevents power-up after a classification failure (I > 50mA, valid only in AUTO mode)
CL_DISC	2	R/W	A logic high enables reduced current-limit voltage threshold (V_{FLT_LIM}) according to port classification result
Reserved	1	R/W	Reserved
Reserved	0	R/W	Reserved

Table 21. Power Enable Pushbuttons

ADDRESS = 19h			DESCRIPTION
SYMBOL	BIT	R/W	
PWR_OFF4	7	W	A logic high powers off port 4
PWR_OFF3	6	W	A logic high powers off port 3
PWR_OFF2	5	W	A logic high powers off port 2
PWR_OFF1	4	W	A logic high powers off port 1
PWR_ON4	3	W	A logic high powers on port 4
PWR_ON3	2	W	A logic high powers on port 3
PWR_ON2	1	W	A logic high powers on port 2
PWR_ON1	0	W	A logic high powers on port 1

Table 22. Global Pushbuttons

ADDRESS = 1Ah			DESCRIPTION
SYMBOL	BIT	R/W	
CLR_INT	7	W	A logic high clears all interrupts
Reserved	6		Reserved
Reserved	5		Reserved
RESET_IC	4	W	A logic high resets the MAX5935
RESET_P4	3	W	A logic high softly resets port 4
RESET_P3	2	W	A logic high softly resets port 3
RESET_P2	1	W	A logic high softly resets port 2
RESET_P1	0	W	A logic high softly resets port 1

Writing a 1 to CLR_INT (Table 22) clears all the event registers and the corresponding interrupt bits in register R00h. Writing a 1 to RESET_P_ turns off power to the corresponding port and resets only the status and event registers of that port. After execution, the bits reset to 0. Writing a 1 to RESET_IC causes a global software reset, after which the register map is set back to its reset state. A reset sets R1Ah = 00h.

Table 23. ID Register

ADDRESS = 1Bh			DESCRIPTION
SYMBOL	BIT	R/W	
ID_CODE	7	R	ID_CODE[4]
	6	R	ID_CODE[3]
	5	R	ID_CODE[2]
	4	R	ID_CODE[1]
	3	R	ID_CODE[0]
REV	2	R	REV [2]
	1	R	REV [1]
	0	R	REV [0]

ID register keeps track of the device ID number and revision. The MAX5935's ID_CODE[4:0] = 11000b. Contact the factory for REV[2:0] value.

Table 24. SMODE Register

ADDRESS = 1Ch			DESCRIPTION
SYMBOL	BIT	CoR	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
Reserved	5	—	Reserved
Reserved	4	—	Reserved
SMODE4	3	CoR	Hardware control flag for port 4
SMODE3	2	CoR	Hardware control flag for port 3
SMODE2	1	CoR	Hardware control flag for port 2
SMODE1	0	CoR	Hardware control flag for port 1

Enable SMODE function (Table 24) by setting EN_WHDOG (R1Fh[7]) to 1. SMODE_ bit goes high when the watchdog counter reaches zero and the port(s) switch over to hardware-controlled mode. SMODE_ also goes high each and every time the software tries to power on a port but is denied since the port is in hardware mode. A reset sets R1Ch = 00h.

Set EN_WHDOG (R1Fh[7]) to 1 (Table 25) to enable the watchdog function. When activated, the watchdog timer counter, WDTIME[7:0], continuously decrements toward zero once every 164ms. Once the counter reaches zero (also called watchdog expiry), the MAX5935 enters hardware-controlled mode and each port shifts to a mode set by the HWMODE_ bit in register R1Fh (Table 24). Use software to set WDTIME and continuously set this register to some nonzero value before the register reaches zero to prevent a watchdog expiry. In this way, the software gracefully manages the power to ports upon a system crash or switchover.

While in hardware-controlled mode, the MAX5935 ignores all requests to turn the power on and the flag SMODE_ indicates that the hardware took control of the MAX5935 operation. In addition, the software is not allowed to change the mode of operation in hardware-controlled mode. A reset sets R1Eh = 00h.

Setting EN_WHDOG (Table 26) high activates the watchdog counter. When the counter reaches zero, the port switches to the hardware-controlled mode determined by the corresponding HWMODE_ bit. A low in HWMODE_ switches the port into shutdown by setting the bits in register R12h to 00. A high in HWMODE_ switches the port into auto mode by setting the bits in register R12h to 11. If WD_INT_EN is set, an interrupt is sent if any of the SMODE bits are set.

Table 25. Watchdog Timer Register

ADDRESS = 1Eh			DESCRIPTION
SYMBOL	BIT	R/W	
WDTIME	7	R/W	WDTIME[7]
	6	R/W	WDTIME[6]
	5	R/W	WDTIME[5]
	4	R/W	WDTIME[4]
	3	R/W	WDTIME[3]
	2	R/W	WDTIME[2]
	1	R/W	WDTIME[1]
	0	R/W	WDTIME[0]

Table 26. Switch Mode Register

ADDRESS = 1Fh			DESCRIPTION
SYMBOL	BIT	R/W	
EN_WHDOG	7	R/W	A logic high enables the watchdog function
WD_INT_EN	6	—	Enables interrupt on SMODE_ bits
Reserved	5	—	
ACTESTM	4	R/W	AC test mode
HWMODE4	3	R/W	Port 4 switches to AUTO if logic high and SHUTDOWN if logic low when watchdog timer expires
HWMODE3	2	R/W	Port 3 switches to AUTO if logic high and SHUTDOWN if logic low when watchdog timer expires
HWMODE2	1	R/W	Port 2 switches to AUTO if logic high and SHUTDOWN if logic low when watchdog timer expires
HWMODE1	0	R/W	Port 1 switches to AUTO if logic high and SHUTDOWN if logic low when watchdog timer expires

Writing a 1 to ACTESTM brings the MAX5935 to an AC test mode. In this mode, the MAX5935 forces all GATE_ pins low and all PGOOD_ status bits high, thus allowing AC disconnect detection without powering on the ports. A reset sets R1Fh = 00h.

Use IGATE[2:0] (Table 27) to set the gate pin pullup current, I_{PU}, according to the following formula:

$$I_{PU} = 50\mu A - 6.25 \times N$$

where N is the decimal value of IGATE[2:0].

Use AC_TH[2:0] to program the current threshold of the AC disconnect comparator according to the following formula:

$$IAC\_TH = 213.68\mu A + 28.33\mu A \times N$$

where N is the decimal value of AC_TH[2:0]

Note: The programmed value has the same percentage tolerance as the value specified in the *Electrical Characteristics*.

When set low, DET_BYP inhibits port power-on if the discovery detection was bypassed in AUTO mode. When set high, it allows the part to turn on power to a non-IEEE 802.3af load without doing detection. If OSCF_RS is set high, the OSC_FAIL bit is ignored.

A reset sets R23h = 04h, which sets I_{PU} = 50µA and I_{AC_TH} = 325µA as shown in the *Electrical Characteristics*.

Use R27h (Table 28) to program the current-limit threshold, V_{SU_LIM}, and the nominal load disconnect detection time, t_{DISC} nominal.

Use IMAX[3:0] to program the current-limit trip voltage according to the following formula:

$$V_{SU\_LIM} = 135mV + 19.25mV \times N$$

Where N is the decimal value of IMAX[3:0]. The V_{FAULT_LIM} limit scales proportionally to the V_{SU_LIM} value (I_{FAULT} = 88% of V_{SU_LIM}).

A reset sets R27h = 47h, which sets V_{SU_LIM} = 212mV (typ) as shown in the *Electrical Characteristics*. The default threshold is set to meet the IEEE 802.3af standard when using an R_{SENSE} = 0.5Ω, 1%, 100ppm.

Table 27. Program Register 1

ADDRESS = 23h			DESCRIPTION
SYMBOL	BIT	R/W	
IGATE	7	R/W	IGATE[2]
	6	R/W	IGATE[1]
	5	R/W	IGATE[0]
DET_BYP	4	R/W	Detect bypass protection in AUTO mode
OSCF_RS	3	R/W	OSC_FAIL Reset Bit
AC_TH	2	R/W	AC_TH[2]
	1	R/W	AC_TH[1]
	0	R/W	AC_TH[0]

Table 28. Program Register 2

ADDRESS = 27h			DESCRIPTION
SYMBOL	BIT	R/W	
IMAX	7	R	IMAX[3]. V_{SU_LIM} programming bit 3
	6	R	IMAX[2]. V_{SU_LIM} programming bit 2
	5	R	IMAX[1]. V_{SU_LIM} programming bit 1
	4	R	IMAX[0]. V_{SU_LIM} programming bit 0
TD_PR	3	R	TD_PR[3]. t_{DISC} nominal programming bit 3
	2	R	TD_PR [2]. t_{DISC} nominal programming bit 2
	1	R	TD_PR [1]. t_{DISC} nominal programming bit 1
	0	R	TD_PR [0]. t_{DISC} nominal programming bit 0

Use TF_PR[3:0] to set the nominal value for t_{DISC} according to the following formula:

$$t_{DISC} \text{ nominal} = 238ms + 16ms \times N$$

where N is the decimal value of the binary words TF_PR[3:0].

A reset sets R27h = 47h, which sets t_{DISC} nominal = 350ms as shown in the *Electrical Characteristics*. Use R27h in conjunction with the two TDISC[1:0] bits in register R16h to program the values of t_{DISC} from 60ms to almost 340ms with a 16ms resolution.

Example: Set TD_PR[3:0] = 1111b, TDISC[1:0] = 11b

Then:

$$t_{DISC} = 2 \times t_{DISC} \text{ nominal}$$
$$= 2 \times (238ms + 16ms \times 15)$$
$$= 956ms$$

Note: The programmed value has the same percentage tolerance as the value specified in the *Electrical Characteristics*.

Table 29. Program Register 3

ADDRESS = 28h			DESCRIPTION
SYMBOL	BIT	R/W	
TF_PR	7	R	TF_PR[3]. t_{FAULT} nominal programming bit 3
	6	R	TF_PR[2]. t_{FAULT} nominal programming bit 2
	5	R	TF_PR[1]. t_{FAULT} nominal programming bit 1
	4	R	TF_PR[0]. t_{FAULT} nominal programming bit 0
TS_PR	3	R	TS_PR[3]. t_{START} nominal programming bit 3
	2	R	TS_PR[2]. t_{START} nominal programming bit 2
	1	R	TS_PR[1]. t_{START} nominal programming bit 1
	0	R	TS_PR[0]. t_{START} nominal programming bit 0

Use the program registers (Table 29) to set the nominal value for t_{FAULT} and t_{START} for all ports according to the following formula:

$$t_{FAULT} \text{ nominal} = 40.96ms + 2.72ms \times N$$

$$t_{START} \text{ nominal} = 40.96ms + 2.72ms \times N$$

where N is the decimal value of TF_PR[3:0] or TS_PR[3:0], respectively.

A reset sets R28h = 77h, which sets $t_{FAULT} = t_{START}$ = 60ms as shown in the *Electrical Characteristics*. Use R28h in conjunction with the two TSTART and TFAULT bits in register R16h to program the values of t_{FAULT} and t_{START} from about 20ms to almost 330ms with a 2.72ms resolution.

Example: Set TF_PR[3:0] = 1111b, TFAULT[1:0] = 11b

Then:

$$t_{FAULT} = 4 \times t_{FAULT} \text{ nominal}$$
$$= 4 \times (40.96ms + 2.72ms \times 15)$$
$$= 327ms$$

Note: The programmed value has the same percentage tolerance as the value specified in the *Electrical Characteristics*.

Table 30. Register Map Summary

ADDR	REGISTER NAME	R/W	PORT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
INTERRUPTS												
00h	Interrupt	RO	G	SUP_FLT	TSTR_FLT	IMAX_FLT	CL_END	DET_END	LD_DISC	PG_INT	PE_INT	0000,0000
01h	Int Mask	R/W	G	MASK7	MASK6	MASK5	MASK4	MASK3	MASK2	MASK1	MASK0	AAA0,0A00
EVENTS												
02h	Power Event	RO	4321	PG_CHG4	PG_CHG3	PG_CHG2	PG_CHG1	PWEN_ CHG4	PWEN_ CHG3	PWEN_ CHG2	PWEN_ CHG1	0000,0000
03h	Power Event CoR	CoR										
04h	Detect Event	RO	4321	CL_END4	CL_END3	CL_END2	CL_END1	DET_END4	DET_END3	DET_END2	DET_END1	0000,0000
05h	Detect Event CoR	CoR										
06h	Fault Event	RO	4321	LD_DISC4	LD_DISC3	LD_DISC2	LD_DISC1	IMAX_FLT4	IMAX_FLT3	IMAX_FLT2	IMAX_FLT1	0000,0000
07h	Fault Event CoR	CoR										
08h	Tstart Event	RO	4321	IVC4	IVC3	IVC2	IVC1	STRT_FLT4	STRT_FLT3	STRT_FLT2	STRT_FLT1	0000,0000
09h	Tstart Event CoR	CoR										
0Ah	Supply Event	RO	4321	TSD	VDD_OV	VDD_UV	VEE UVLO	VEE_OV	VEE_UV	OSC_FAIL	VDD_UVLO	0011,0101*
0Bh	Supply Event CoR	CoR										
STATUS												
0Ch	Port 1 Status	RO	1	reserved	CLASS1[2]	CLASS1[1]	CLASS1[0]	Reserved	DET_ST1 [2]	DET_ST1 [1]	DET_ST1 [0]	0000,0000
0Dh	Port 2 Status	RO	2	reserved	CLASS2[2]	CLASS2[1]	CLASS2[0]	Reserved	DET_ST2 [2]	DET_ST2 [1]	DET_ST2 [0]	0000,0000
0Eh	Port 3 Status	RO	3	reserved	CLASS3[2]	CLASS3[1]	CLASS3[0]	Reserved	DET_ST3 [2]	DET_ST3 [1]	DET_ST3 [0]	0000,0000
0Fh	Port 4 Status	RO	4	reserved	CLASS4[2]	CLASS4[1]	CLASS4[0]	Reserved	DET_ST4 [2]	DET_ST4 [1]	DET_ST4 [0]	0000,0000
10h	Power Status	RO	4321	PGOOD4	PGOOD3	PGOOD2	PGOOD1	PWR_EN4	PWR_EN3	PWR_EN2	PWR_EN1	0000,0000
11h	Pin Status	RO	G	reserved	reserved	A3	A2	A1	A0	MIDSPAN	AUTO	00A3A2, A1A0MA

**UV and UVLO bits of V_{EE} and V_{DD} asserted depends on the order of V_{EE} and V_{DD} supplies are brought up.*
A = AUTO pin state, A3..0 = ADDRESS pin states, M = MIDSPAN pin state, R = Contact factory for current revision code Table 15a.

Table 30. Register Map Summary (continued)

ADDR	REGISTER NAME	R/W	PORT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
CONFIGURATION												
12h	Operating Mode	R/W	4321	P4_M1	P4_M0	P3_M1	P3_M0	P2_M1	P2_M0	P1_M1	P1_M0	AAAA,AAAA
13h	Disconnect Enable	R/W	4321	ACD_EN4	ACD_EN3	ACD_EN2	ACD_EN1	DCD_EN4	DCD_EN3	DCD_EN2	DCD_EN1	0000,AAAA
14h	Det/Class Enable	R/W	4321	CLASS_EN4	CLASS_EN 3	CLASS_EN 2	CLASS_EN 1	DET_EN4	DET_EN3	DET_EN2	DET_EN1	AAAA,AAAA
15h	Backoff Enable	R/W	4321	reserved	reserved	reserved	reserved	Bckoff4	Bckoff3	Bckoff2	Bckoff1	0000,MMMM
16h	Timing Config	R/W	G	RSTR[1]	RSTR[0]	TSTART[1]	TSTART[0]	TFAULT[1]	TFAULT[0]	TDISC[1]	TDISC[0]	0000,0000
17h	Misc Config	R/W	G	INT_EN	RSTR_EN	reserved	reserved	POFF_CL	CL_DISC	reserved	reserved	1100,0000
PUSHBUTTONS												
18h	Reserved	R/W	G	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	
19h	Power Enable	WO	4321	PWR_OFF4	PWR_OFF3	PWR_OFF2	PWR_OFF1	PWR_ON4	PWR_ON3	PWR_ON2	PWR_ON1	0000,0000
1Ah	Global	WO	G	CLR_INT	reserved	reserved	RESET_IC	RESET_P4	RESET_P3	RESET_P2	RESET_P1	0000,0000
GENERAL												
1Bh	ID	RO	G	ID_CODE[4]	ID_CODE[3]	ID_CODE[2]	ID_CODE[1]	ID_CODE[0]	REV [2]	REV [1]	REV [0]	1100,0RRR
1Ch	SMODE	CoR	4321	reserved	reserved	reserved	reserved	SMODE4	SMODE3	SMODE2	SMODE1	00000000
1Dh	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
1EH	Watchdog	R/W	G	WDTIME[7]	WDTIME[6]	WDTIME[5]	WDTIME[4]	WDTIME[3]	WDTIME[2]	WDTIME[1]	WDTIME[0]	00000000
1FH	Switch Mode	R/W	4321	EN_WHDOG	WD_INT_EN	reserved	ACTEST	HWMODE4	HWMODE3	HWMODE2	HWMODE1	00000000
MAXIM RESERVED												
20H	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
21H	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
22H	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
23H	Program1	R/W	4321	IGATE[2]	IGATE[1]	IGATE[0]	DET_BYP	OSCF_RS	AC_TH[0]	AC_TH[0]	AC_TH[0]	00000100
24h	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
25h	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
26h	Reserved		G	reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved	00000000
27H	Program2	R/W	G	IMAX[3]	IMAX[2]	IMAX[1]	IMAX[0]	TD[3]	TD[2]	TD[1]	TD[0]	01000111
28H	Program3	R/W	G	TF_PR[3]	TF_PR[2]	TF_PR[1]	TF_PR[0]	TS_PR[3]	TS_PR[2]	TS_PR[1]	TS_PR[0]	01110111

**UV and UVLO bits of V_{EE} and V_{DD} asserted depends on the order of V_{EE} and V_{DD} supplies are brought up.*
A = AUTO pin state, A3..0 = ADDRESS pin states, M = MIDSPAN pin state, R = Contact factory for current revision code Table 15a.

Applications Information

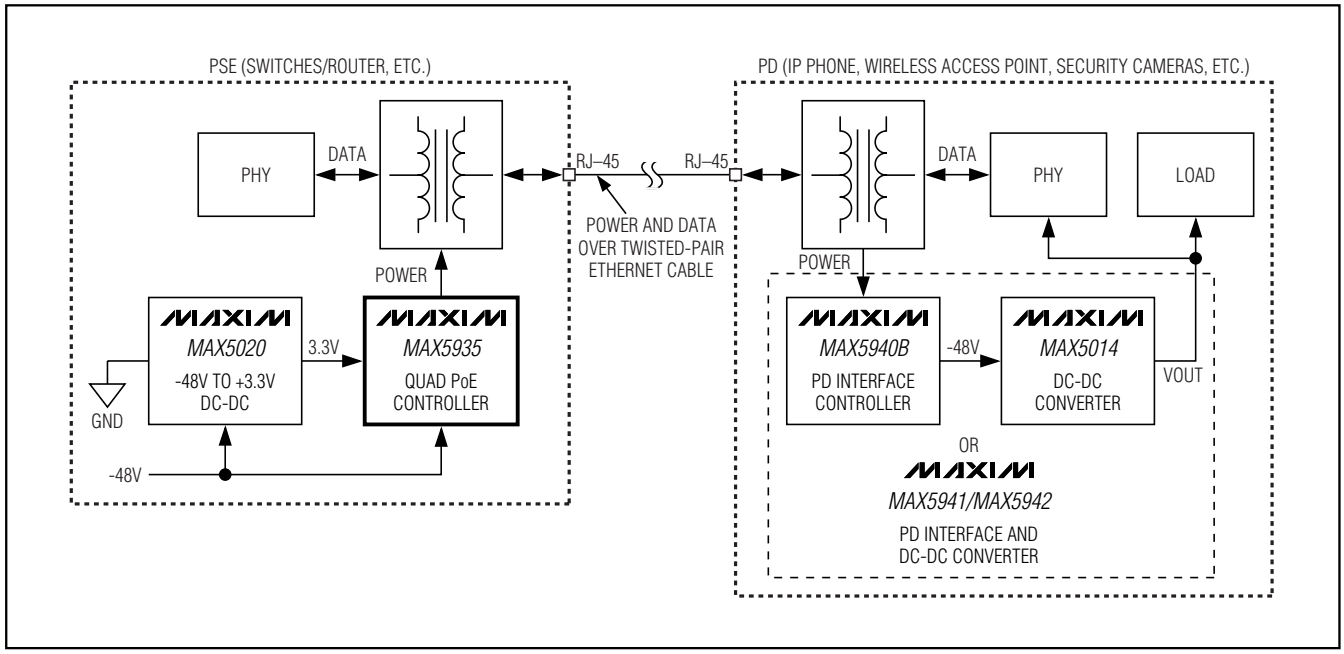


Figure 14. PoE System Block Diagram

Quad Network Power Controller for Power-Over-LAN

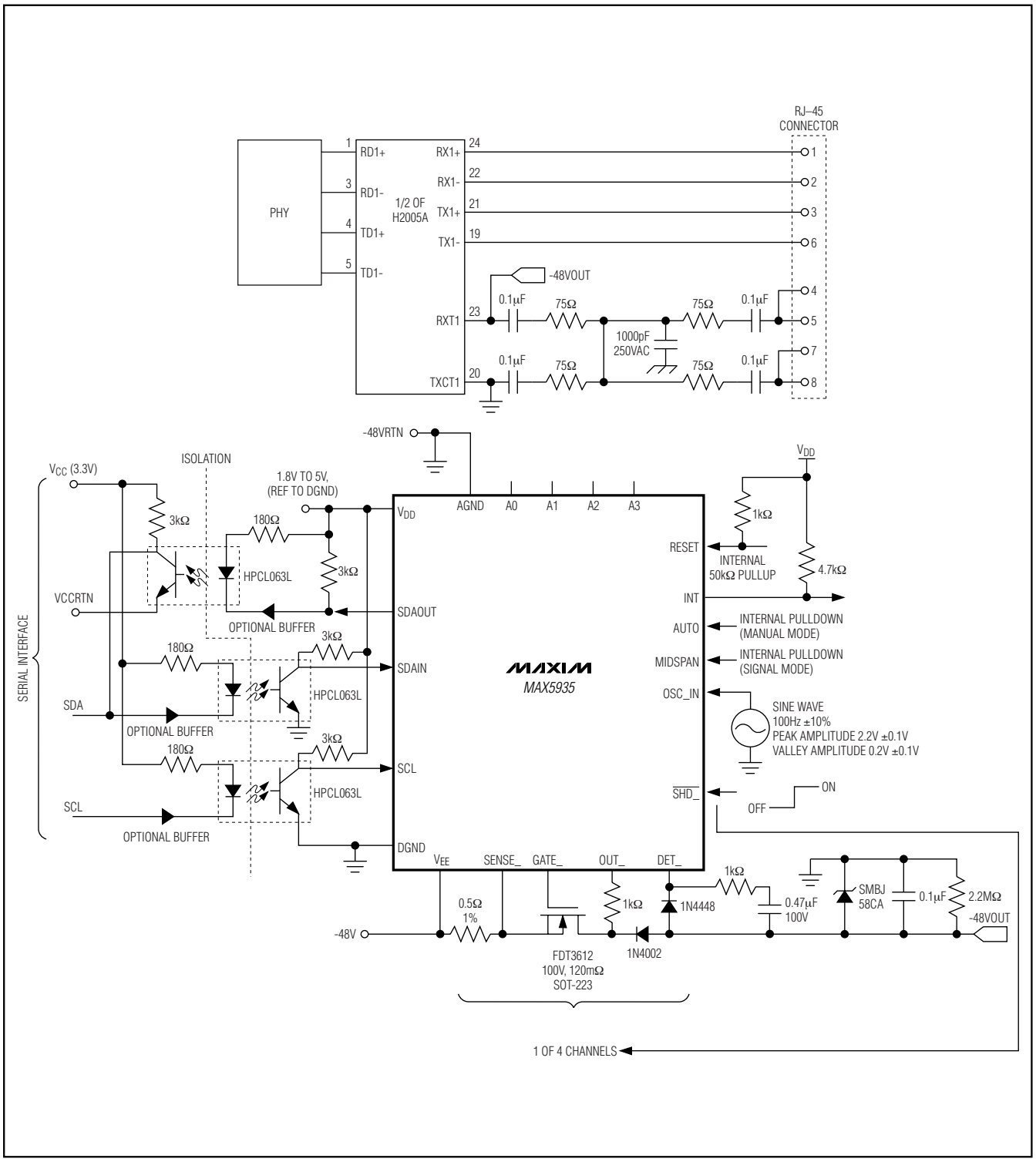


Figure 15. PoE System Diagram of One Complete Port, Endpoint PSE

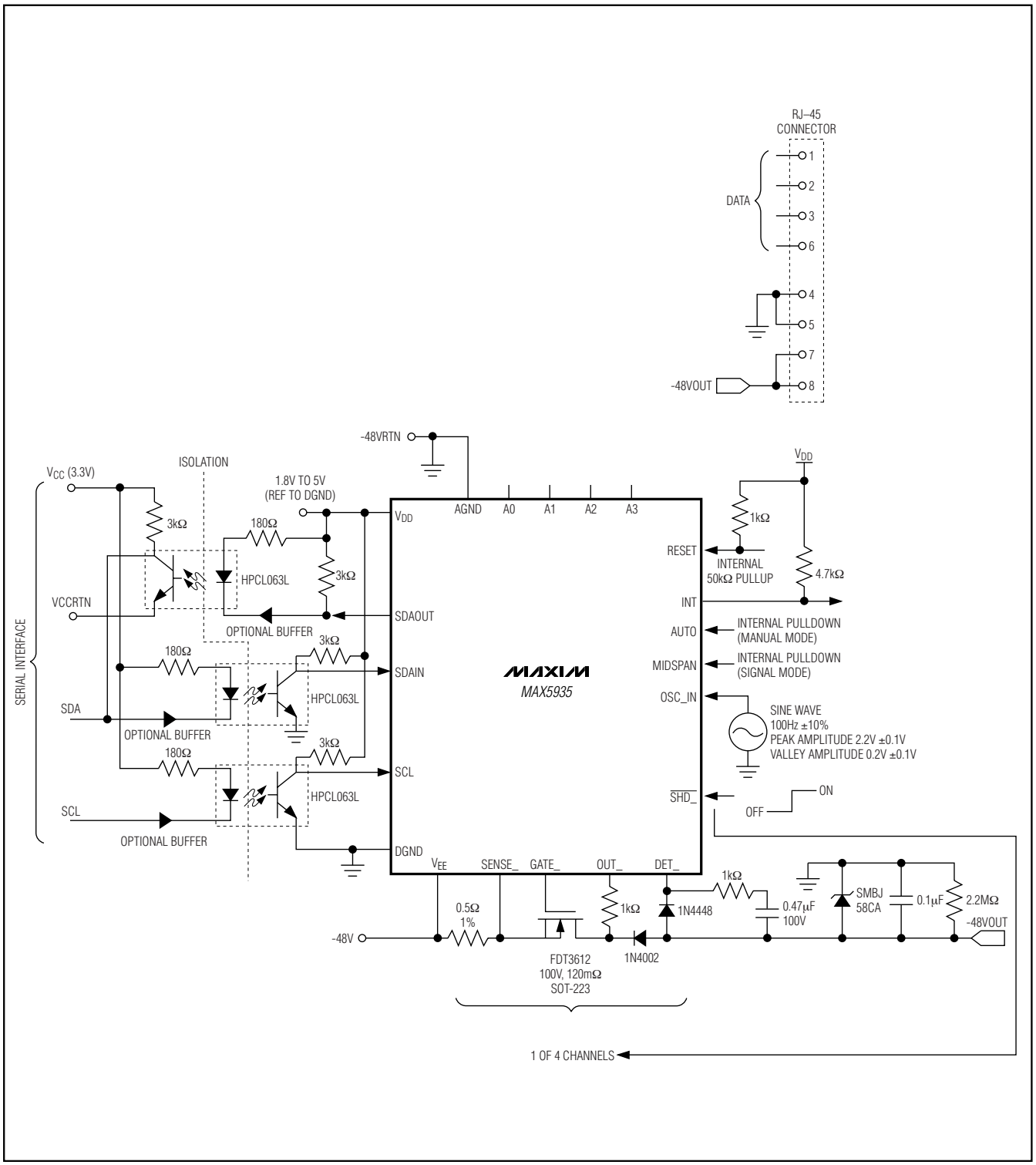


Figure 16. PoE System Diagram of One Complete Port, Midspan PSE

Quad Network Power Controller for Power-Over-LAN

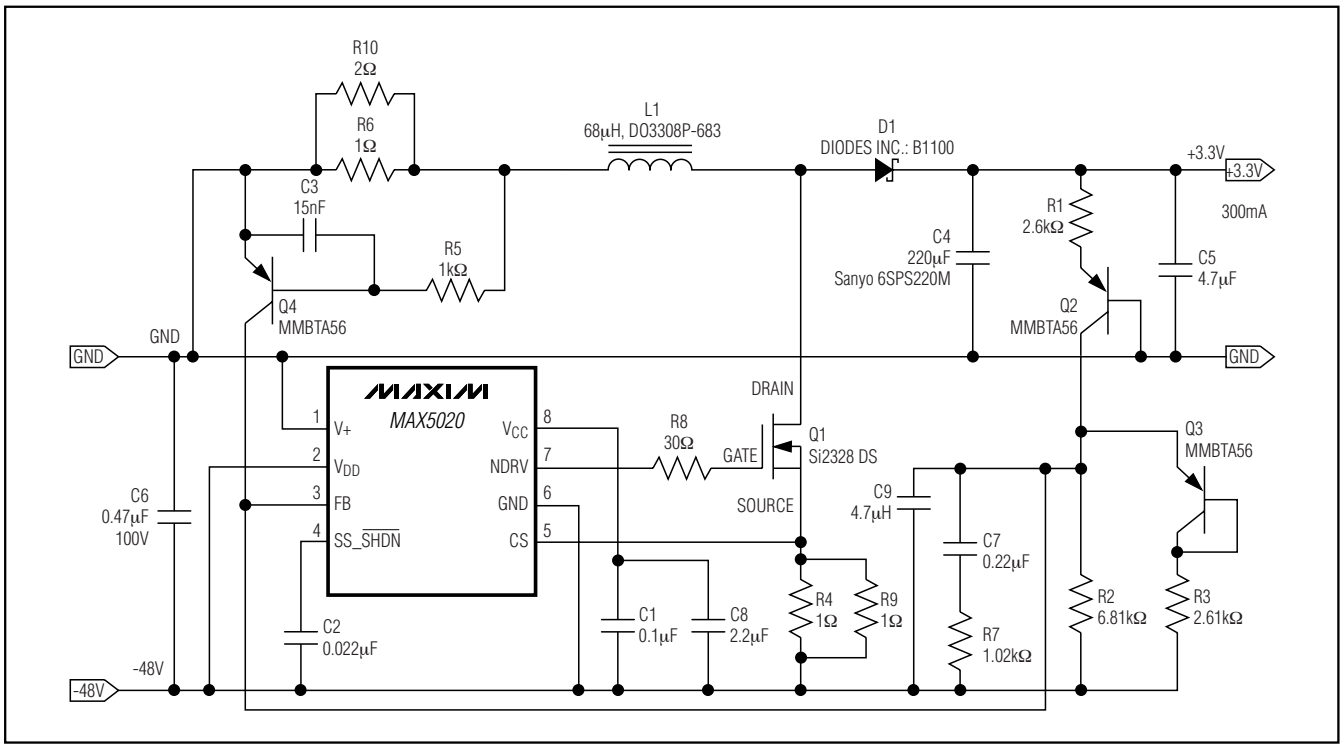


Figure 17. -48V to +3.3V (300mA) Boost Converter Solution for VDIG

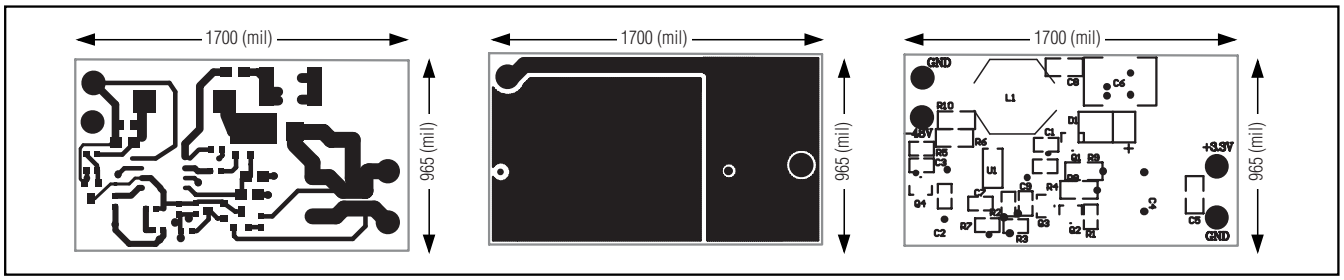


Figure 18. Layout Example for Boost Converter Solution for VDIG

Component List

DESIGNATION	DESCRIPTION
C1	0.1µF, 25V ceramic capacitor
C2	0.022µF, 25V ceramic capacitor
C3	15nF, 25V ceramic capacitor
C4	220µF capacitor Sanyo 6SVPA220MAA
C5	4.7µF, 16V ceramic capacitor
C6	0.1µF, 100V ceramic capacitor
C7	0.22µF, 16V ceramic capacitor
C8	0.22µF, 16V ceramic capacitor
C9	4.7nF, 16V ceramic capacitor
D1	B1100 100V Schottky diode
L1	68µH inductor Coilcraft DO3308P-683 or equivalent
Q1	Si2328DS Vishay n-Channel MOSFET, SOT-23
Q2	MMBTA56 small-signal pnp
Q3	MMBTA56 small-signal pnp
Q4	MMBTA56 small-signal pnp
R1	2.61kΩ ±1% resistor
R2	6.81kΩ ±1% resistor
R3	2.61kΩ ±1% resistor
R4	1Ω ±1% resistor
R5	1kΩ ±1% resistor
R6	1Ω ±1% resistor
R7	1.02kΩ ±1% resistor
R8	30Ω ±1% resistor
R9	1Ω ±1% resistor
R10	2Ω ±1% resistor
U1	High-voltage PWM IC MAX5020ESA (8-pin SO)

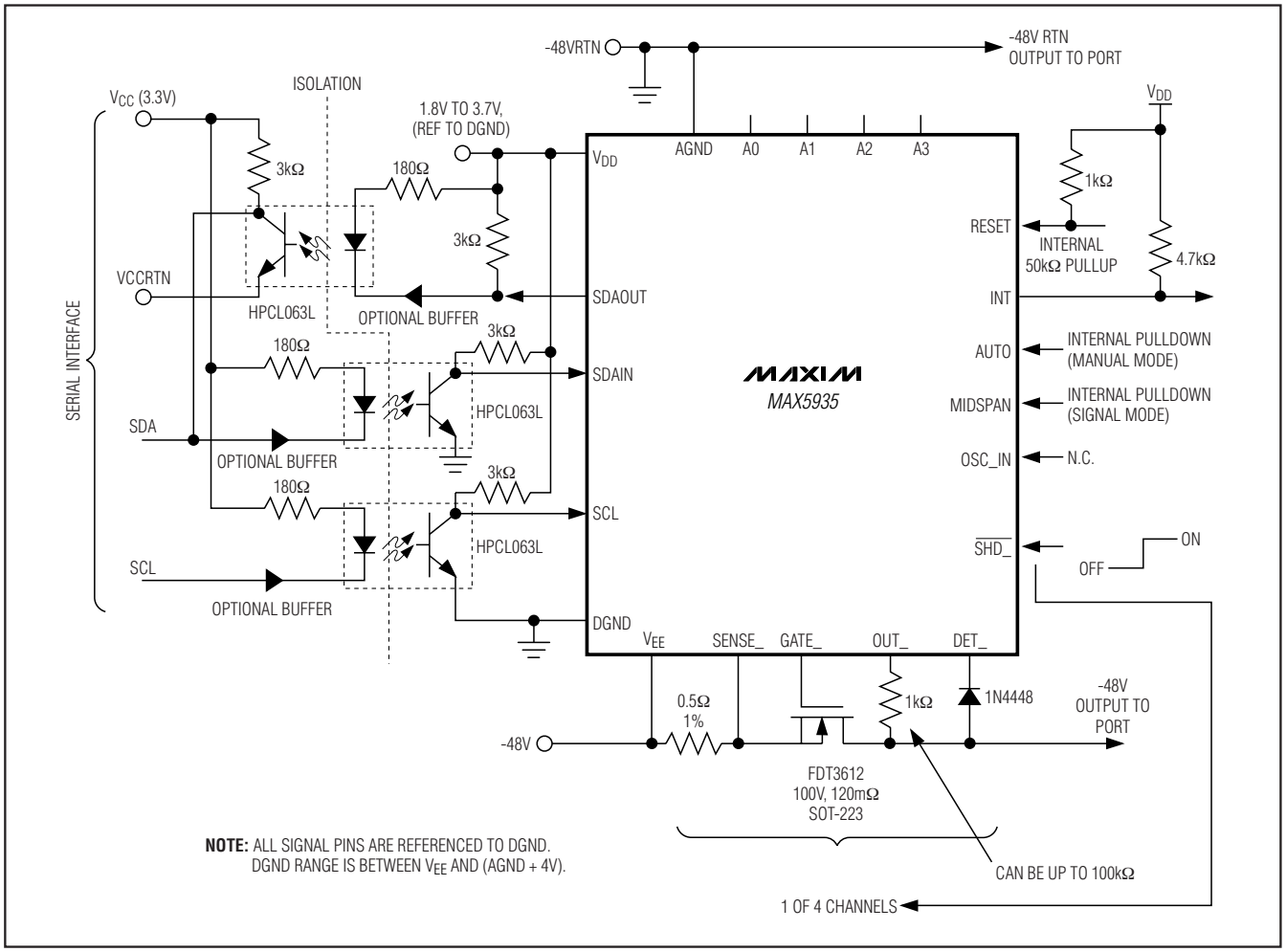
Chip Information

TRANSISTOR COUNT: 148,768

PROCESS: BiCMOS

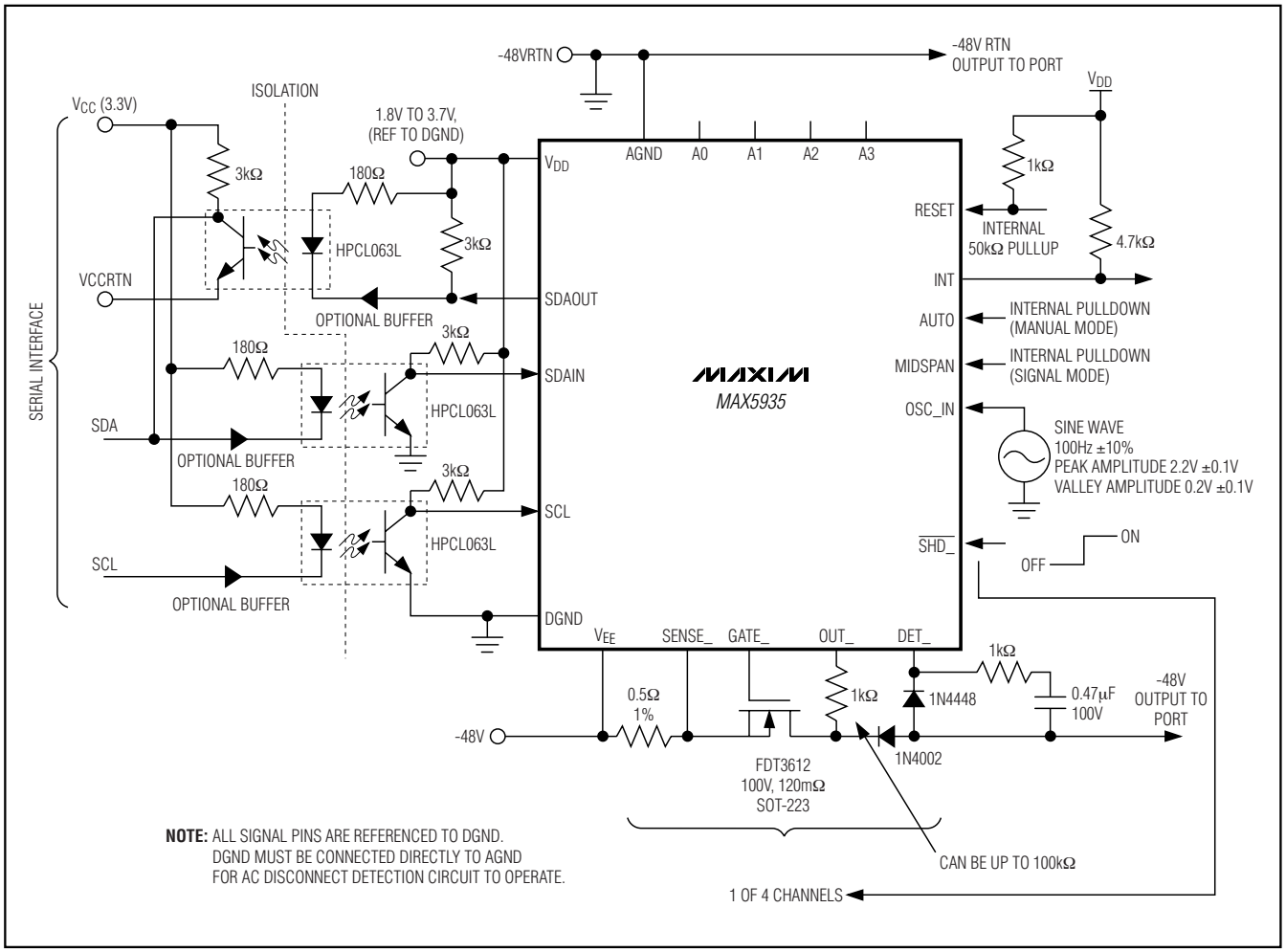
Quad Network Power Controller for Power-Over-LAN

Typical Operating Circuits



Typical Operating Circuit 1 (without AC Load Removal Detection)

Typical Operating Circuits (continued)



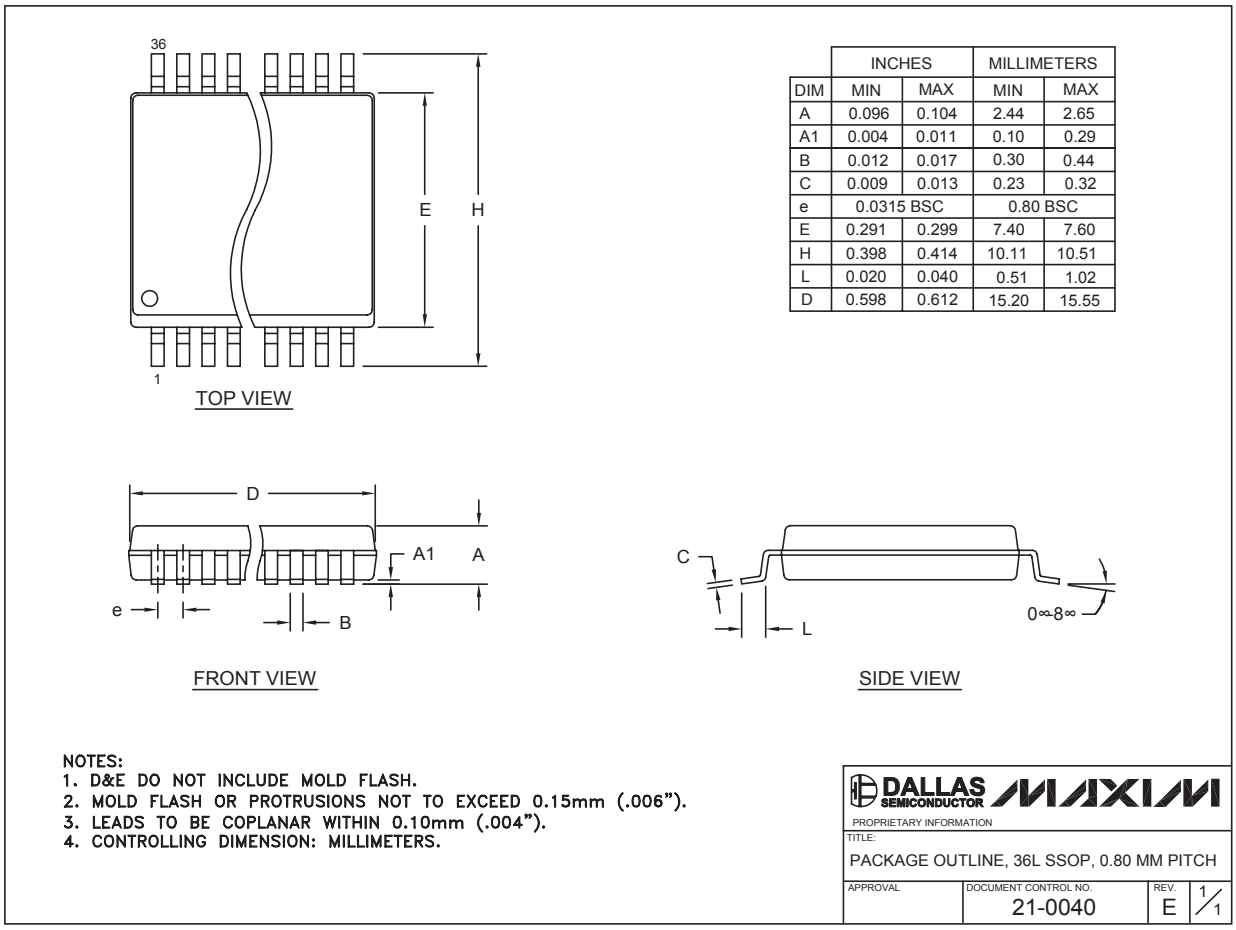
Typical Operating Circuit 2 (with AC Load Removal Detection)

Quad Network Power Controller for Power-Over-LAN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.096	0.104	2.44	2.65
A1	0.004	0.011	0.10	0.29
B	0.012	0.017	0.30	0.44
C	0.009	0.013	0.23	0.32
e	0.0315 BSC		0.80 BSC	
E	0.291	0.299	7.40	7.60
H	0.398	0.414	10.11	10.51
L	0.020	0.040	0.51	1.02
D	0.598	0.612	15.20	15.55

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 36L SSOP, 0.80 MM PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0040	E	1/1

Revision History

Pages changed at Rev 1: 1–6, 44

Pages changed at Rev 2: 1, 44