

**SY89546U**
**2.5V, 3.2Gbps Differential 4:1 LVDS  
Multiplexer with 1:2 Fanout and Internal  
Termination**
**General Description**

The SY89546U is a precision, High-speed 4:1 differential multiplexer that provides two copies of the selected input. The high speed LVDS (350mV) compatible outputs with a guaranteed throughput of up to 3.2Gbps over temperature and voltage.

The SY89546U differential inputs include Micrel's unique 3-pin internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled without external resistor-bias and termination networks. The result is a clean, stub-free, low jitter interface solution.

The SY89546U operates from a single 2.5V supply, and is guaranteed over the full industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ). For applications that require a 3.3V supply, consider the SY89547L. Or, for applications that only require one differential output, consider the SY89544U or SY89545L. The SY89546U is part of Micrel's Precision Edge® product family.

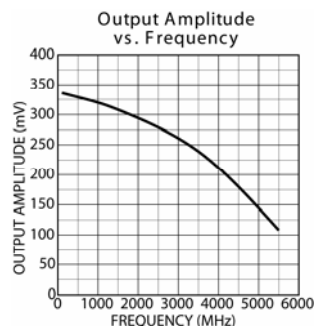
Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

**Features**

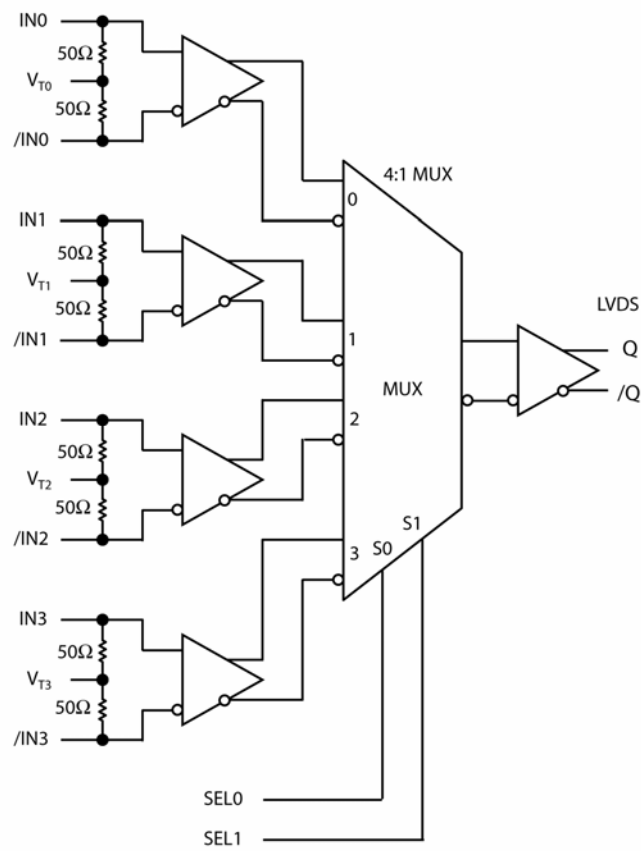
- Selects among four differential inputs
- Provides two copies of the selected input
- Guaranteed AC parameters over temp/voltage:
  - DC-to >3.2Gbps data rate throughput
  - <620ps In-to-Out  $t_{pd}$
  - <150ps  $t_r/t_f$  time
- Unique input isolation design minimize crosstalk
- Ultra-low jitter design:
  - <1ps<sub>RMS</sub> random jitter
  - <10ps<sub>PP</sub> deterministic jitter
  - <10ps<sub>PP</sub> total jitter (clock)
  - <0.7ps<sub>RMS</sub> crosstalk-induced jitter
- Internal input termination
- Unique input termination and VT pin accepts DC-coupled and AC-coupled inputs (LVDS, LVPECL, CML)
- 350mV LVDS output swing
- Power supply 2.5V  $\pm 5\%$
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range
- Available in 32-pin (5mmx5mm) MLF® package

**Applications**

- SONET/SDH multi-channel select applications
- Fibre Channel applications
- GigE application

**Typical Performance**

# Functional Block Diagram



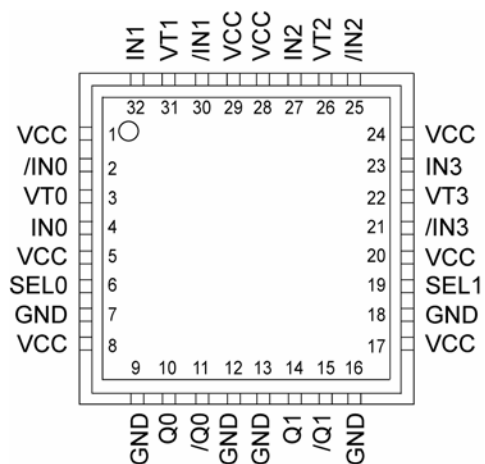
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89546UMI	MLF-32	Industrial	SY89546U	Sn-Pb
SY89546UMITR <sup>(2)</sup>	MLF-32	Industrial	SY89546U	Sn-Pb
SY89546UMG <sup>(3)</sup>	MLF-32	Industrial	SY89546U with Pb-Free bar-line indicator	Pb_Free NiPdAu
SY89546UMGTR <sup>(2,3)</sup>	MLF-32	Industrial	SY89546U with Pb-Free bar-line indicator	Pb_Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.
2. Tape and Reel.
3. Recommended for new designs.

## Pin Configuration



**32-Pin MLF®**

## Pin Description

Pin Number	Pin Name	Pin Function
4, 2, 21, 32, 30, 27, 25, 23, 21	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3	Differential Inputs: These inputs pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a $V_T$ pin through 50 $\Omega$ . Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to $V_{CC}$ and the complementary input to GND through a 1k $\Omega$ resistor. The VT pin is to be left open in this configuration. Please refer to the "input Interface Applications" section for more details.
3, 31, 26, 22	VT0, VT1, VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair, terminates to a $V_T$ pin. The $V_{TA0}$ , $V_{TA1}$ , $V_{TB0}$ , $V_{TB1}$ pins provide a center-tap to a termination network for maximum interface flexibility. See "input Interface Applications" section for more details.
6, 19	SEL0, SEL1	These single-ended TTL/CMOS-compatible inputs select the inputs to the multiplexers. Note that these inputs are internally connected to a 25k $\Omega$ pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is $V_{CC}/2$ .
1, 5, 8, 17, 20, 24, 28, 29	VCC	Positive Power Supply: Bypass with 0.1 $\mu$ F    0.01 $\mu$ F low ESR capacitors.
10, 11, 14, 15	Q0, /Q0 Q1, /Q1	Differential Outputs: These LVDS outputs pairs are the outputs of the device. They are a logic function of the INA0, INA1, INB0, INB1 and SELA and SELB inputs. Please refer to the "Truth Table" for details. If an output is not used, it must be terminated with 100 $\Omega$ across the differential pair.
7, 9, 12, 13, 16, 18	GND, Exposed pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC}$ ).....	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ ).....	-0.5V to $V_{CC}$
Termination Current <sup>(3)</sup>	
Source or sink current on VT .....	$\pm 100$ mA
Input Current	
Source or sink current on VT .....	$\pm 50$ mA
Lead Temperature (soldering, 20sec.).....	+260°C
Storage Temperature ( $T_s$ ).....	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ ).....	2.375V to 2.625V
Ambient Temperature ( $T_A$ ).....	-40°C to +85°C
Package Thermal Resistance <sup>(4)</sup>	
MLF® ( $\theta_{JA}$ )	
Still Air, multi-layer PCB .....	35°C/W
500lfpm, multi-layer PCB.....	28°C/W
MLF® ( $\Psi_{JA}$ )	
Junction-to-Board .....	20°C/W

**DC Electrical Characteristics<sup>(5)</sup>**

-40°C  $\leq T_A \leq$  +85°C, unless stated otherwise.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply		2.375	2.5	2.625	V
$I_{CC}$	Power Supply Current	No Load, Max. $V_{CC}$ <sup>(6)</sup>		75	100	mA
$R_{DIFF\_IN}$	Differential Input Resistance (IN-to-/IN)		80	100	120	$\Omega$
$R_{IN}$	Input Resistance (IN-to- $V_T$ , /IN-to- $V_T$ )		40	50	60	$\Omega$
$V_{IH}$	Input High Voltage (IN, /IN)		1.2		$V_{CC}$	V
$V_{IL}$	Input Low Voltage (IN, /IN)		0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	Note 7	0.1		$V_{CC}$	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing $ IN - /IN $	Note 7	0.2			V
IN-to- $V_T$		<b>Note 7</b>			1.8	V

**Notes:**

- Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Due to the limited drive capability use for input of the same package only.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.  $\Psi_{JA}$  uses 4-layer  $\theta_{JA}$  in still-air unless otherwise stated.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Includes current through internal 50 $\Omega$  pull-ups.
- See "Single-Ended and Differential Swings" section for  $V_{IN}$  and  $V_{DIFF\_IN}$  definition.

## LVDS Outputs DC Electrical Characteristics<sup>(9)</sup>

$V_{CC} = 2.5V \pm 5\%$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ ,  $R_L = 100\Omega$  across Q and /Q, unless stated otherwise.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage (Q, /Q)	See Figure 5a				V
$V_{OL}$	Output LOW Voltage (Q, /Q)	See Figure 5a	0.925			V
$V_{OUT}$	Output Voltage Swing (Q, /Q)	See Figure 1a, 5a	250	350		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing $ Q - /Q $	See Figure 1b	500	700		mV
$V_{OCM}$	Output common Mode Voltage (Q, /Q)	See Figure 5b	1.125		1.275	V
$\Delta V_{OCM}$	Change in Common Mode Voltage (Q, /Q)	See Figure 5b	-50		+50	mV

## LVTTL/CMOS DC Electrical Characteristics<sup>(9)</sup>

$V_{CC} = 2.5V \pm 5\%$ ,  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless stated otherwise.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current				40	$\mu A$
$I_{IL}$	Input LOW Current				-300	$\mu A$

### Notes:

1. The circuit is the designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics <sup>(10)</sup>

$V_{CC} = 2.5V \pm 5\%$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ ,  $R_L = 100\Omega$  across Q and /Q, unless stated otherwise.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	NRZ Data	3.2			Gbps
		$V_{OUT} \geq 200mV$ Clock	3	4		GHz
$t_{PD}$	Differential Propagation Delay	IN-to-Q	330	430	530	ps
		SEL-to-Q	200	400	700	ps
$t_{SKEW}$	Input-to-Input Skew	<b>Note 11</b>		4	20	ps
	Output-to- Output Skew	<b>Note 12</b>		8	20	ps
	Part-to-Part Skew	<b>Note 13</b>			200	ps
$t_{JITTER}$	Data	Random Jitter (RJ)	<b>Note 14</b>		1	ps <sub>RMS</sub>
		Deterministic Jitter (DJ)	<b>Note 15</b>		10	ps <sub>P</sub>
	Clock	Total Jitter (TJ)	<b>Note 16</b>		10	ps <sub>P</sub>
		Cycle-to-Cycle Jitter	<b>Note 17</b>			1
Crosstalk	Crosstalk-Induced Jitter	<b>Note 18</b>			0.7	ps <sub>RMS</sub>
$t_r, t_f$	Output Rise/Fall Time (20% to 80%)	At full output swing	35	80	150	ps

### Notes:

1. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High frequency AC parameters are guaranteed by design and characterization.
2. Input-to-input skew is the difference in time from an input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.
3. Output-to-output skew is measured between two different outputs under identical input transitions.
4. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Total skew is calculated as the RMS (Root Mean Square) of the input skew and output skew.
5. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 3.2Gbps.
6. Deterministic jitter is measured at 1.25Gbps and 3.2Gbps, with both K28.5 and  $2^{23}-1$  PRBS pattern.  
Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
7. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T - T_{n-1}$ , where T is the time between rising edges of the output cycle.
8. Crosstalk is measured at the output while applying two similar clock frequencies to adjacent inputs that are asynchronous with respect to each other at the inputs.

## Single-Ended and Differential Swings

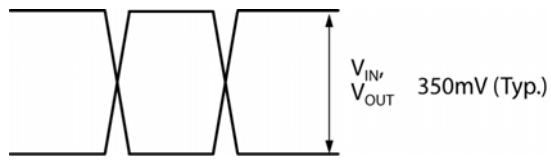


Figure 1a . Single-Ended Voltage Swing

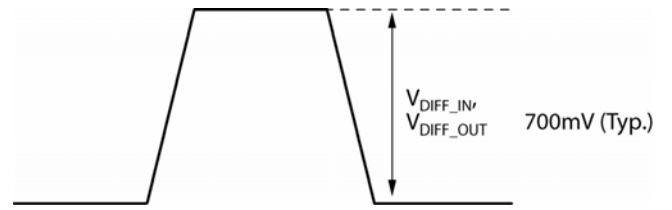


Figure 1b . Differential Voltage Swing

## Timing Diagram

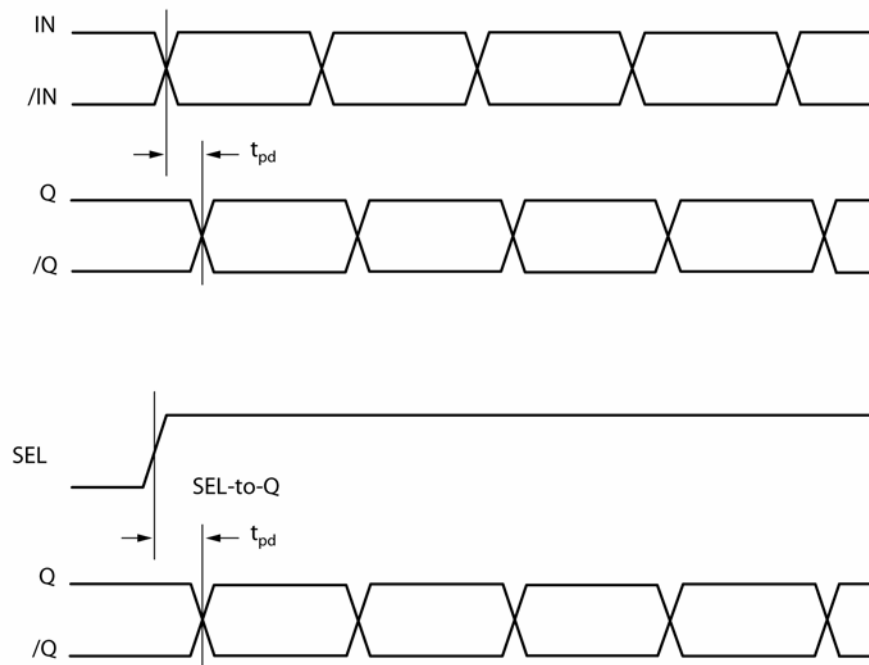


Figure 2. Timing Diagrams

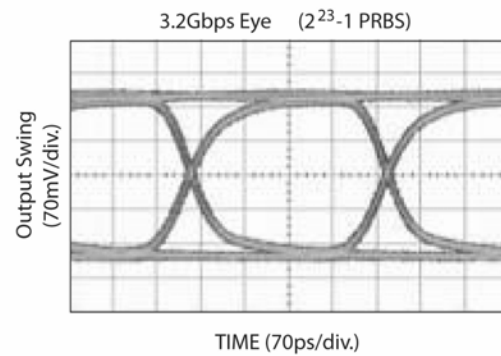
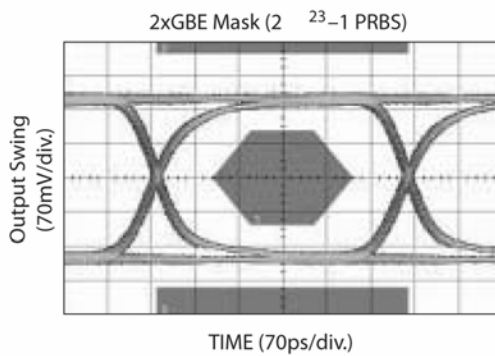
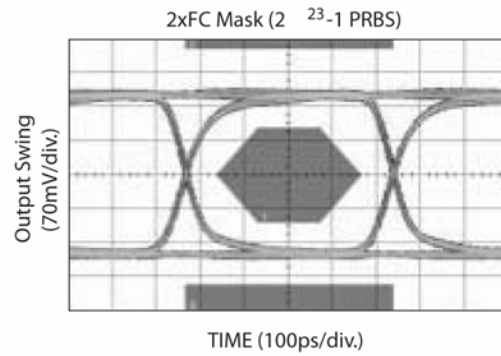
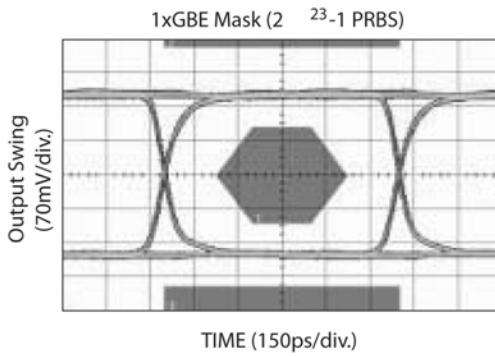
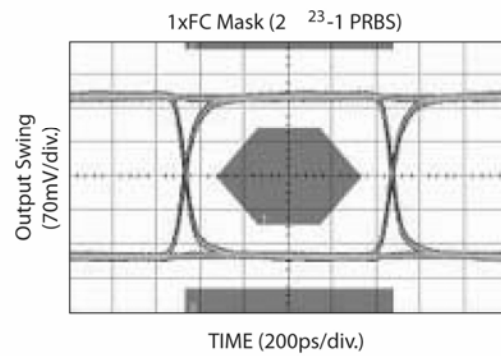
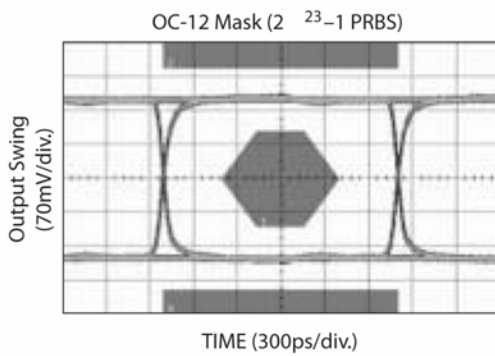
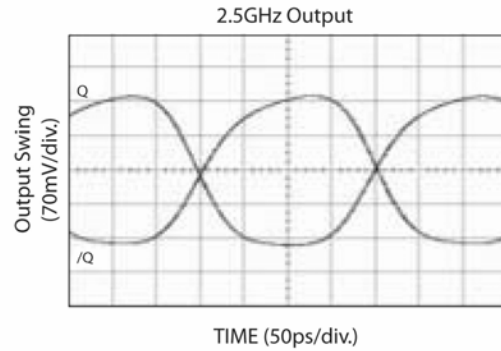
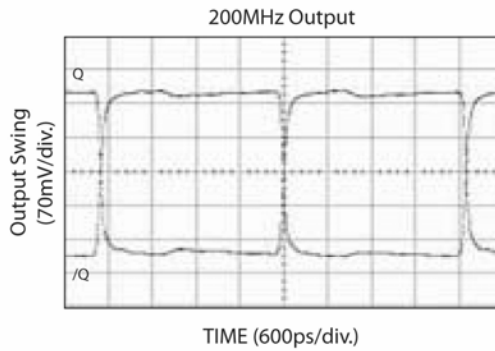


**Truth Table**

IN0	IN1	IN2	IN3	SEL0	SEL1	Q	/Q
0	X	X	X	0	0	0	1
1	X	X	X	0	0	1	0
X	0	X	X	1	0	0	1
X	1	X	X	1	0	1	0
X	X	0	X	0	1	0	1
X	X	1	X	0	1	1	0
X	X	X	0	1	1	0	1
X	X	X	1	1	1	1	0

## Functional Characteristics

$V_{CC} = 2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ .



## Input and Output Stage Internal Termination

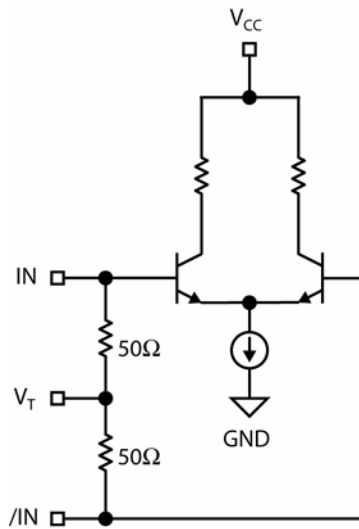
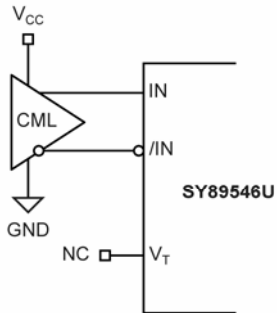
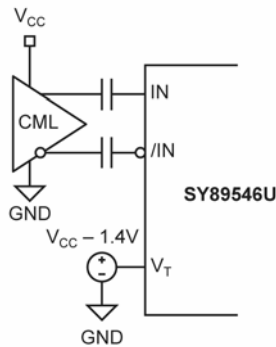


Figure 3 . Simplified Differential Input Stage

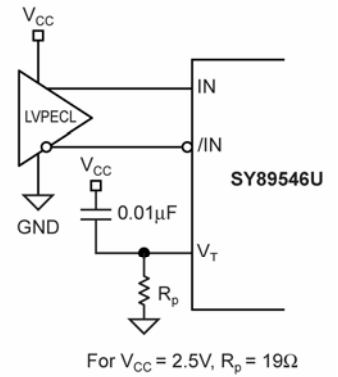
# Input Interface Applications



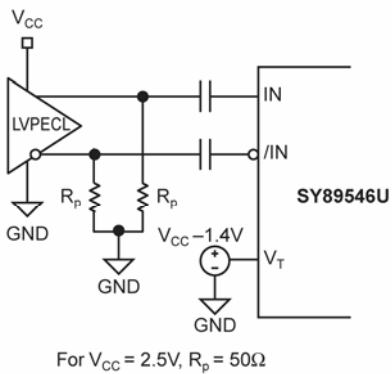
**Figure 4a. CML Interface (DC-Coupled)**



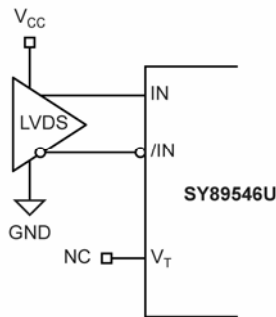
**Figure 4b. CML Interface (AC-Coupled)**



**Figure 4c. LVPECL Interface (DC-Coupled)**



**Figure 4d. LVPECL Interface (AC-Coupled)**



**Figure 4e. LVDS Interface**

## Output Interface Applications

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in

ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

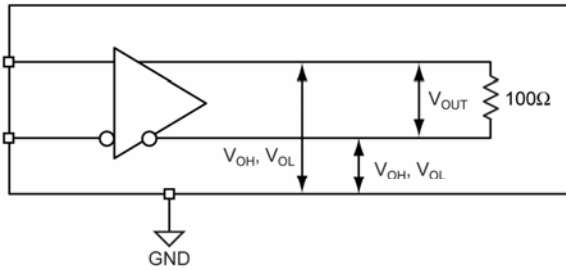


Figure 5a. LVDS Differential Measurement

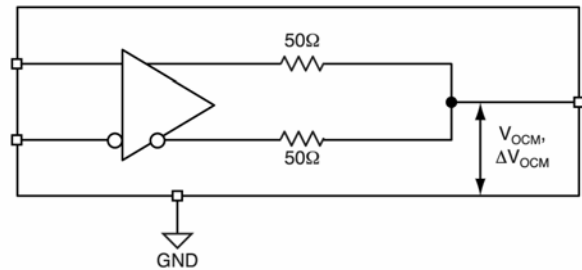
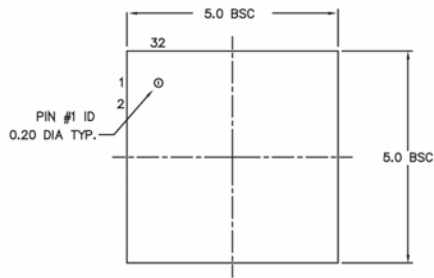


Figure 5b. LVDS Common Mode Measurement

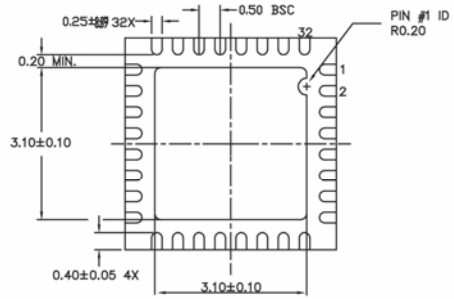
## Related Micrel Products and Support Documentation

Part Number	Function	Data Sheet Link
SY89542U	2.5 V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination	<a href="http://www.micrel.com/_PDF/HBW/sy89542u.pdf">http://www.micrel.com/_PDF/HBW/sy89542u.pdf</a>
SY89543L	3.3V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination	<a href="http://www.micrel.com/_PDF/HBW/sy89543l.pdf">http://www.micrel.com/_PDF/HBW/sy89543l.pdf</a>
SY89544U	2.5V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with Internal Input Termination	<a href="http://www.micrel.com/_PDF/HBW/sy89544u.pdf">http://www.micrel.com/_PDF/HBW/sy89544u.pdf</a>
SY89545L	3.3V, 3.2Gbps 4:1 LVDS Multiplexer with Internal Input Termination	<a href="http://www.micrel.com/_PDF/HBW/sy89545l.pdf">http://www.micrel.com/_PDF/HBW/sy89545l.pdf</a>
SY89547L	3.3V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Input Termination	<a href="http://www.micrel.com/_PDF/HBW/SY89547l.pdf">http://www.micrel.com/_PDF/HBW/SY89547l.pdf</a>
	MLF® Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>

# Package Information



TOP VIEW

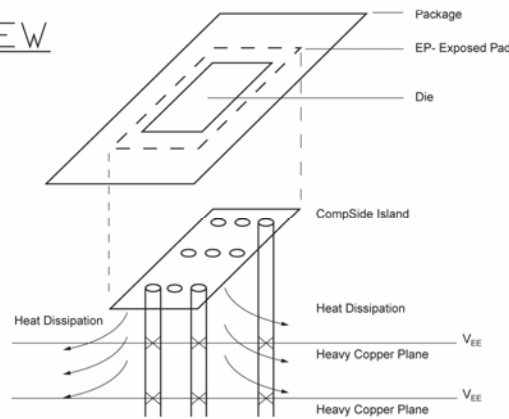


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 32-Pin MFL® Package**  
**(Always solder, or equivalent, the exposed pad to the PCB)**

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