

### FEATURES

- Bandwidth: 195 MHz**
- Low insertion loss and on resistance: 2.6 Ω typical**
- On-resistance flatness 0.3 Ω typical**
- 3.3 V analog signal range (5 V supply, 75 Ω load)**
- Single 3 V/5 V supply operation**
- Low quiescent supply current: 1 nA typical**
- Fast switching times: t<sub>ON</sub> = 185 ns, t<sub>OFF</sub> = 181 ns**
- I<sup>2</sup>C<sup>®</sup>-compatible interface**
- Compact, 24-lead LFCSP**
- Two I<sup>2</sup>C-controllable logic outputs**
- ESD protection**
  - 4 kV human body model (HBM)**
  - 200 V machine model (MM)**
  - 1 kV field-induced charged device model (FICDM)**

### APPLICATIONS

- RGB/YPbPr video switches**
- HDTV**
- Projection TV**
- DVD-R/RW**
- AV receivers**

### GENERAL DESCRIPTION

The ADG793A/ADG793G are monolithic CMOS devices comprising three 3:1 multiplexers/demultiplexers controllable via a standard I<sup>2</sup>C serial interface. The CMOS process provides ultralow power dissipation, yet gives high switching speed and low on resistance.

The on-resistance profile is very flat over the full analog input range, and the wide bandwidth ensures excellent linearity and low distortion. These features, combined with a wide input signal range, make the ADG793A/ADG793G the ideal switching solution for a wide range of TV applications, including RGB and YPbPr video switches.

The switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The ADG793A/ADG793G switches exhibit break-before-make switching action. The ADG793G has two general-purpose logic output pins controllable through the I<sup>2</sup>C interface, which can be used to control other non-I<sup>2</sup>C-compatible devices such as video filters. The integrated I<sup>2</sup>C interface provides a large degree of

### FUNCTIONAL BLOCK DIAGRAMS

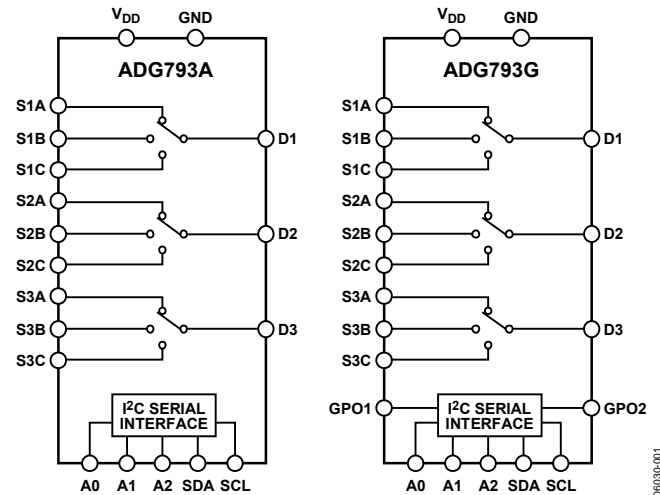


Figure 1.

flexibility in the system design. It has three configurable I<sup>2</sup>C address pins that allow the user to connect up to eight devices to the same bus to build larger switching arrays.

The ADG793A/ADG793G operate from a single 3 V or 5 V supply voltage and are available in a compact, 4 mm × 4 mm body, 24-lead, lead-free chip scale package (LFCSP).

### PRODUCT HIGHLIGHTS

1. Wide bandwidth: 195 MHz.
2. Ultralow power dissipation.
3. Extended input signal range.
4. Integrated I<sup>2</sup>C serial interface.
5. Compact, 4 mm × 4 mm body, 24-lead, lead-free chip scale package (LFCSP).
6. ESD protection tested as per ESD Association standards:
  - 4 kV HBM (ANSI/ESD STM5.1-2001)
  - 200 V MM (ANSI/ESD STM5.2-1999)
  - 1 kV FICDM (ANSI/ESD STM5.3.1-1999)

#### Rev. 0

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## REVISION HISTORY

7/06—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>ANALOG SWITCH</b>					
Analog Signal Range <sup>2</sup>	$V_S = V_{DD}$ , $R_L = 1\text{ M}\Omega$	0		4	V
	$V_S = V_{DD}$ , $R_L = 75\ \Omega$	0		3.3	V
On Resistance, $R_{ON}$	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 22		2.6	3.5	$\Omega$
	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 22			4	$\Omega$
On-Resistance Matching Between Channels, $\Delta R_{ON}$	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$		0.15	0.5	$\Omega$
	$V_D = 1\text{ V}$ , $I_S = -10\text{ mA}$			0.6	$\Omega$
On-Resistance Flatness, $R_{FLAT(ON)}$	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$		0.3	0.55	$\Omega$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_{S(OFF)}$	$V_D = 4\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4\text{ V}$ , see Figure 23		$\pm 0.25$		nA
Drain Off Leakage, $I_{D(OFF)}$	$V_D = 4\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4\text{ V}$ , see Figure 23		$\pm 0.25$		nA
Channel On Leakage, $I_{D(ON)}$ , $I_{S(ON)}$	$V_D = V_S = 4\text{ V}/1\text{ V}$ , see Figure 24		$\pm 0.25$		nA
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>					
$t_{ON}$ , $t_{ENABLE}$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 28		185	240	ns
$t_{OFF}$ , $t_{DISABLE}$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 28		181	235	ns
Break-Before-Make Time Delay, $t_D$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_{S1} = V_{S2} = 2\text{ V}$ , see Figure 29	1	3		ns
I <sup>2</sup> C-to-GPO Propagation Delay, $t_H$ , $t_L$	ADG793G only			130	ns
Off Isolation	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 26		-60		dB
Channel-to-Channel Crosstalk	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 27				
Same Multiplexer			-55		dB
Different Multiplexer			-75		dB
-3 dB Bandwidth	$R_L = 50\ \Omega$ , see Figure 25		195		MHz
THD + N	$R_L = 100\ \Omega$		0.14		%
Charge Injection	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ , see Figure 30		5		pC
$C_{S(OFF)}$			10		pF
$C_{D(OFF)}$			26		pF
$C_{D(ON)}$ , $C_{S(ON)}$			37		pF
Power Supply Rejection Ratio, PSSR	$f = 20\text{ kHz}$		70		dB
Differential Gain Error	CCIR330 test signal		0.59		%
Differential Phase Error	CCIR330 test signal		0.83		Degrees
<b>LOGIC INPUTS<sup>3</sup></b>					
A0, A1, A2		2.0			V
Input High Voltage, $V_{INH}$				0.8	V
Input Low Voltage, $V_{INL}$				$\pm 1$	$\mu\text{A}$
Input Current, $I_{INL}$ or $I_{INH}$	$V_{IN} = 0\text{ V}$ to $V_{DD}$		0.005		$\mu\text{A}$
Input Capacitance, $C_{IN}$			3		pF
SCL, SDA		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
Input High Voltage, $V_{INH}$		$-0.3$		$+0.3 \times V_{DD}$	V
Input Low Voltage, $V_{INL}$			0.005	$\pm 1$	$\mu\text{A}$
Input Leakage Current, $I_{IN}$	$V_{IN} = 0\text{ V}$ to $V_{DD}$		$0.05 \times V_{DD}$		V
Input Hysteresis					V
Input Capacitance, $C_{IN}$			3		pF

# ADG793A/ADG793G

Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>LOGIC OUTPUTS<sup>3</sup></b>					
SDA Pin					
Output Low Voltage, $V_{OL}$	$I_{SINK} = 3 \text{ mA}$			0.4	V
	$I_{SINK} = 6 \text{ mA}$			0.6	V
Floating-State Leakage Current				$\pm 1$	$\mu\text{A}$
Floating-State Output Capacitance				10	pF
<b>GPO1 Pin and GPO2 Pin</b>					
Output Low Voltage, $V_{OL}$	$I_{LOAD} = +2 \text{ mA}$			0.4	V
Output High Voltage, $V_{OH}$	$I_{LOAD} = -2 \text{ mA}$	2.0			V
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	Digital inputs = 0 V or $V_{DD}$ , I <sup>2</sup> C interface inactive		0.001	1	$\mu\text{A}$
	I <sup>2</sup> C interface active, $f_{SCL} = 400 \text{ kHz}$			0.2	mA
	I <sup>2</sup> C interface active, $f_{SCL} = 3.4 \text{ MHz}$			0.7	mA

<sup>1</sup>All typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise stated.

<sup>2</sup>Guaranteed by initial characterization, not subject to production test.

<sup>3</sup>Guaranteed by design, not subject to production test.

$V_{DD} = 3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>ANALOG SWITCH</b>					
Analogue Signal Range <sup>2</sup>	$V_S = V_{DD}$ , $R_L = 1\text{ M}\Omega$	0		2.2	V
	$V_S = V_{DD}$ , $R_L = 75\ \Omega$	0		1.7	V
On Resistance, $R_{ON}$	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 22		3	4	$\Omega$
	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 22			6	$\Omega$
On-Resistance Matching Between Channels, $\Delta R_{ON}$	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$		0.15	0.6	$\Omega$
	$V_D = 1\text{ V}$ , $I_S = -10\text{ mA}$			1.1	$\Omega$
On-Resistance Flatness, $R_{FLAT(ON)}$	$V_D = 0\text{ V}$ to $1\text{ V}$ , $I_S = -10\text{ mA}$		0.3	2.8	$\Omega$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_{S(OFF)}$	$V_D = 3\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/3\text{ V}$ , see Figure 23		$\pm 0.25$		nA
Drain Off Leakage, $I_{D(OFF)}$	$V_D = 3\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/3\text{ V}$ , see Figure 23		$\pm 0.25$		nA
Channel On Leakage, $I_{D(ON)}$ , $I_{S(ON)}$	$V_D = V_S = 3\text{ V}/1\text{ V}$ , see Figure 24		$\pm 0.25$		nA
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>					
$t_{ON}$ , $t_{ENABLE}$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 28		200	260	ns
$t_{OFF}$ , $t_{DISABLE}$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_S = 2\text{ V}$ , see Figure 28		197	255	ns
Break-Before-Make Time Delay, $t_D$	$C_L = 35\text{ pF}$ , $R_L = 50\ \Omega$ , $V_{S1} = V_{S2} = 2\text{ V}$ , see Figure 29	1	3		ns
I <sup>2</sup> C-to-GPO Propagation Delay, $t_H$ , $t_L$	ADG793G only			121	ns
Off Isolation	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 26		-60		dB
Channel-to-Channel Crosstalk	$f = 10\text{ MHz}$ , $R_L = 50\ \Omega$ , see Figure 27				
Same Multiplexer			-55		dB
Different Multiplexer			-75		dB
-3 dB Bandwidth	$R_L = 50\ \Omega$ , see Figure 25		190		MHz
THD + N	$R_L = 100\ \Omega$		0.14		%
Charge Injection	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ , see Figure 30		3.5		pC
$C_{S(OFF)}$			10		pF
$C_{D(OFF)}$			26		pF
$C_{D(ON)}$ , $C_{S(ON)}$			37		pF
Power Supply Rejection Ratio, PSRR	$f = 20\text{ kHz}$		70		dB
Differential Gain Error	CCIR330 test signal		0.51		%
Differential Phase Error	CCIR330 test signal		0.62		Degrees
<b>LOGIC INPUTS<sup>3</sup></b>					
<b>A0, A1, A2</b>					
Input High Voltage, $V_{INH}$		2.0			V
Input Low Voltage, $V_{INL}$				0.8	V
Input Current, $I_{INL}$ or $I_{INH}$	$V_{IN} = 0\text{ V}$ to $V_{DD}$		0.005	$\pm 1$	$\mu\text{A}$
Input Capacitance, $C_{IN}$			3		pF
<b>SCL, SDA</b>					
Input High Voltage, $V_{INH}$		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
Input Low Voltage, $V_{INL}$		-0.3		$+0.3 \times V_{DD}$	V
Input Leakage Current, $I_{IN}$	$V_{IN} = 0\text{ V}$ to $V_{DD}$		0.005	$\pm 1$	$\mu\text{A}$
Input Hysteresis			$0.05 \times V_{DD}$		V
Input Capacitance, $C_{IN}$			3		pF

# ADG793A/ADG793G

Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>LOGIC OUTPUTS<sup>3</sup></b>					
SDA Pin					
Output Low Voltage, $V_{OL}$	$I_{SINK} = 3 \text{ mA}$			0.4	V
	$I_{SINK} = 6 \text{ mA}$			0.6	V
Floating-State Leakage Current				$\pm 1$	$\mu\text{A}$
Floating-State Output Capacitance			3		pF
<b>GPO1 Pin and GPO2 Pin</b>					
Output Low Voltage, $V_{OL}$	$I_{LOAD} = +2 \text{ mA}$			0.4	V
Output High Voltage, $V_{OH}$	$I_{LOAD} = -2 \text{ mA}$	2.0			V
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	Digital inputs = 0 V or $V_{DD}$ , I <sup>2</sup> C interface inactive		0.001	1	$\mu\text{A}$
	I <sup>2</sup> C interface active, $f_{SCL} = 400 \text{ kHz}$			0.1	mA
	I <sup>2</sup> C interface active, $f_{SCL} = 3.4 \text{ MHz}$			0.2	mA

<sup>1</sup>All typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise stated.

<sup>2</sup>Guaranteed by initial characterization, not subject to production test.

<sup>3</sup>Guaranteed by design, not subject to production test.

## I<sup>2</sup>C TIMING SPECIFICATIONS

V<sub>DD</sub> = 2.7 V to 5.5 V; GND = 0 V; T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. See Figure 2 for timing diagram.

Table 3.

Parameter <sup>1</sup>	Conditions	Min	Max	Unit	Description
f <sub>SCL</sub>	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode				
	C <sub>B</sub> = 100 pF max		3.4	MHz	
	C <sub>B</sub> = 400 pF max		1.7	MHz	
t <sub>1</sub>	Standard mode	4		μs	t <sub>HIGH</sub> , SCL high time
	Fast mode	0.6		μs	
	High speed mode				
	C <sub>B</sub> = 100 pF max	60		ns	
	C <sub>B</sub> = 400 pF max	120		ns	
t <sub>2</sub>	Standard mode	4.7		μs	t <sub>LOW</sub> , SCL low time
	Fast mode	1.3		μs	
	High speed mode				
	C <sub>B</sub> = 100 pF max	160		ns	
	C <sub>B</sub> = 400 pF max	320		ns	
t <sub>3</sub>	Standard mode	250		ns	t <sub>SU,DAT</sub> , data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t <sub>4</sub> <sup>2</sup>	Standard mode	0	3.45	μs	t <sub>HD,DAT</sub> , data hold time
	Fast mode	0	0.9	μs	
	High speed mode				
	C <sub>B</sub> = 100 pF max	0	703	ns	
	C <sub>B</sub> = 400 pF max	0	150	ns	
t <sub>5</sub>	Standard mode	4.7		μs	t <sub>SU,STA</sub> , setup time for a repeated start condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t <sub>6</sub>	Standard mode	4		μs	t <sub>HD,STA</sub> , hold time (repeated) start condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t <sub>7</sub>	Standard mode	4.7		μs	t <sub>BUF</sub> , bus free-time between a stop and a start condition
	Fast mode	1.3		μs	
t <sub>8</sub>	Standard mode	4		μs	t <sub>SU,STO</sub> , setup time for stop condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t <sub>9</sub>	Standard mode		1000	ns	t <sub>RDA</sub> , rise time of SDA signal
	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns	
	High speed mode				
	C <sub>B</sub> = 100 pF max	10	80	ns	
	C <sub>B</sub> = 400 pF max	20	160	ns	
t <sub>10</sub>	Standard mode		300	ns	t <sub>FDA</sub> , fall time of SDA signal
	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns	
	High speed mode				
	C <sub>B</sub> = 100 pF max	10	80	ns	
	C <sub>B</sub> = 400 pF max	20	160	ns	

# ADG793A/ADG793G

Parameter <sup>1</sup>	Conditions	Min	Max	Unit	Description
t <sub>11</sub>	Standard mode		1000	ns	t <sub>RCL</sub> , rise time of SCL signal
	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns	
	High speed mode				
	C <sub>B</sub> = 100 pF max C <sub>B</sub> = 400 pF max	10 20	40 80	ns ns	
t <sub>11A</sub>	Standard mode		1000	ns	t <sub>RCL1</sub> , rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns	
	High speed mode				
	C <sub>B</sub> = 100 pF max C <sub>B</sub> = 400 pF max	10 20	80 160	ns ns	
t <sub>12</sub>	Standard mode		300	ns	t <sub>FCL</sub> , fall time of SCL signal
	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns	
	High speed mode				
	C <sub>B</sub> = 100 pF max C <sub>B</sub> = 400 pF max	10 20	40 80	ns ns	
t <sub>SP</sub>	Fast mode	0	50	ns	Pulse width of suppressed spike
	High speed mode	0	10	ns	

<sup>1</sup>Guaranteed by initial characterization. C<sub>B</sub> refers to capacitive load on the bus line, t<sub>r</sub> and t<sub>f</sub> measured between 0.3 V<sub>DD</sub> and 0.7 V<sub>DD</sub>.

<sup>2</sup>A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.

## TIMING DIAGRAM

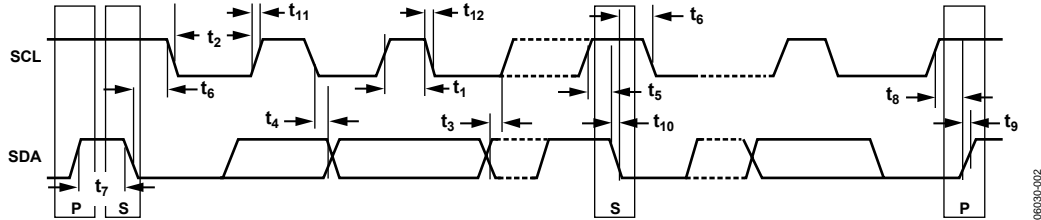


Figure 2. Timing Diagram for 2-Wire Serial Interface



## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +6 V
Analog, Digital Inputs	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D Pins	100 mA
Peak Current, S or D Pins	300 mA (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
$\theta_{JA}$ Thermal Impedance	
24-Lead LFCSP	30°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

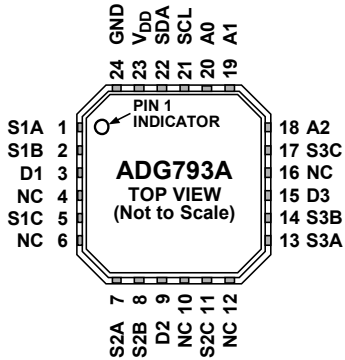
### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADG793A/ADG793G

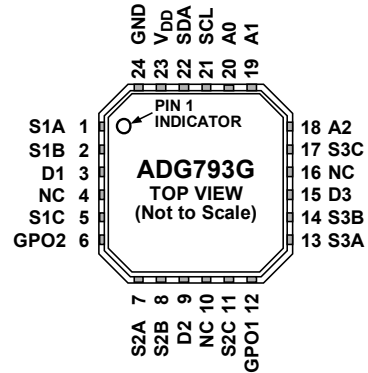
## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**  
 1. NC = NO CONNECT.  
 2. THE EXPOSED PAD MUST BE TIED TO GND.

Figure 3. ADG793A Pin Configuration

06030-029



- NOTES**  
 1. NC = NO CONNECT.  
 2. THE EXPOSED PAD MUST BE TIED TO GND.

Figure 4. ADG793G Pin Configuration

06030-030

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1A	A-Side Source Terminal for Mux 1. Can be an input or output.
2	S1B	B-Side Source Terminal for Mux 1. Can be an input or output.
3	D1	Drain Terminal for Mux 1. Can be an input or output.
4	NC	Not internally connected.
5	S1C	C-Side Source Terminal for Mux 1. Can be an input or output.
6	NC/GPO2	Not internally connected for ADG793A. General-Purpose Logic Output 2 for ADG793G.
7	S2A	A-Side Source Terminal for Mux 2. Can be an input or output.
8	S2B	B-Side Source Terminal for Mux 2. Can be an input or output.
9	D2	Drain Terminal for Mux 2. Can be an input or output.
10	NC	Not internally connected.
11	S2C	C-Side Source Terminal for Mux 2. Can be an input or output.
12	NC/GPO1	Not internally connected for ADG793A. General-Purpose Logic Output 1 for ADG793G.
13	S3A	A-Side Source Terminal for Mux 3. Can be an input or output
14	S3B	B-Side Source Terminal for Mux 3. Can be an input or output.
15	D3	Drain Terminal for Mux 3. Can be an input or output.
16	NC	Not internally connected.
17	S3C	C-Side Source Terminal for Mux 3. Can be an input or output.
18	A2	Logic Input. Sets Bit A2 from the third least significant bit of the 7-bit slave address.
19	A1	Logic Input. Sets Bit A1 from the second least significant bit of the 7-bit slave address.
20	A0	Logic Input. Sets Bit A0 from the first least significant bit of the 7-bit slave address.
21	SCL	Digital Input, Serial Clock Line. Open-drain input that is used in conjunction with SDA to clock data into the device. External pull-up resistor required.
22	SDA	Digital I/O. Bidirectional open-drain data line. External pull-up resistor required.
23	V <sub>DD</sub>	Positive Power Supply Input.
24	GND	Ground (0 V) Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

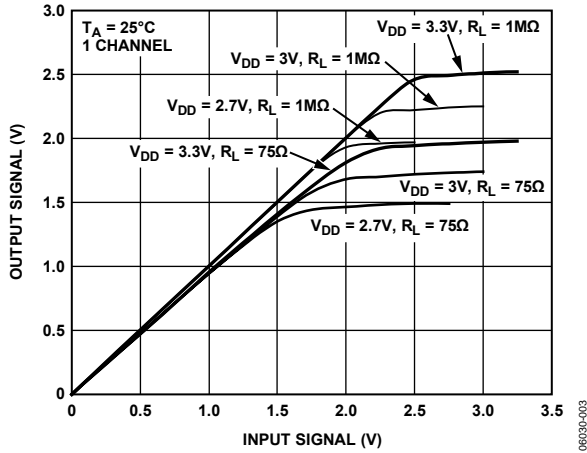


Figure 5. Analog Signal Range (3 V Supply)

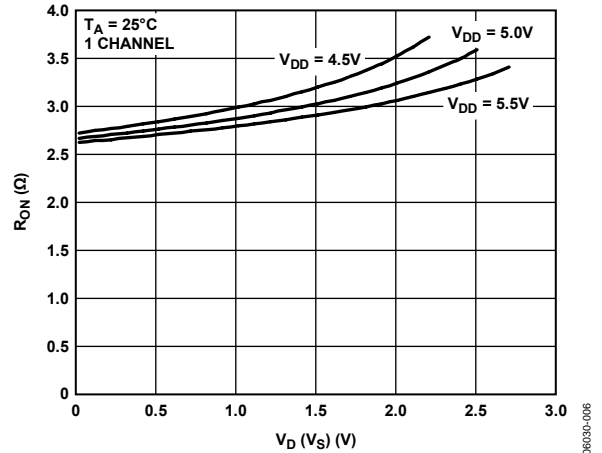


Figure 8. On Resistance vs.  $V_D$  (Vs) with 5 V Supply

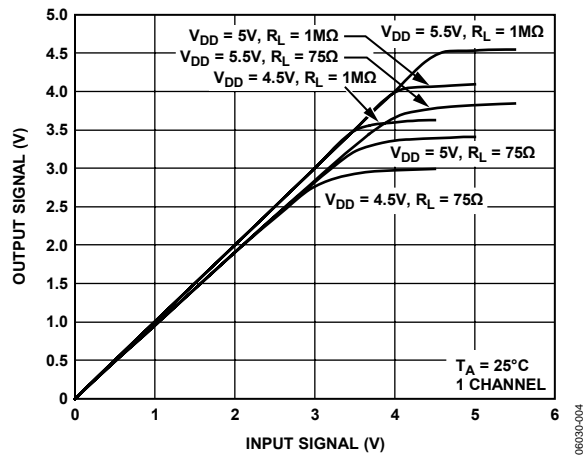


Figure 6. Analog Signal Range (5 V Supply)

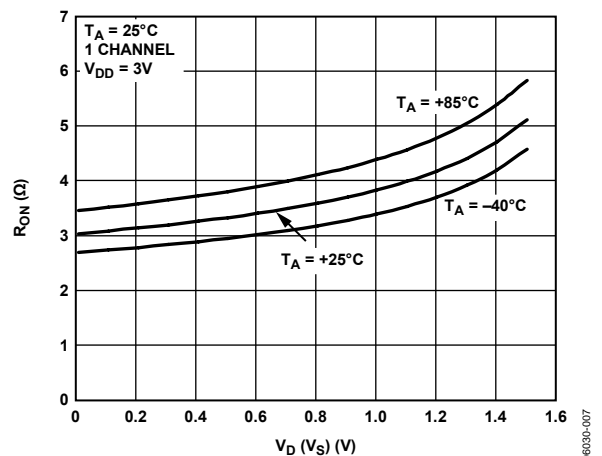


Figure 9. On Resistance vs.  $V_D$  (Vs) for Various Temperatures with 3 V Supply

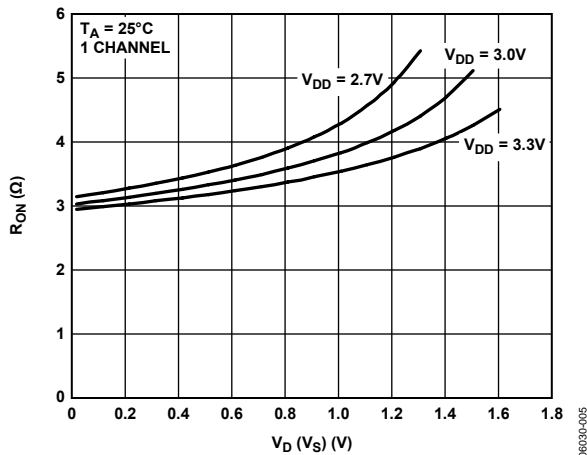


Figure 7. On Resistance vs.  $V_D$  (Vs) with 3 V Supply

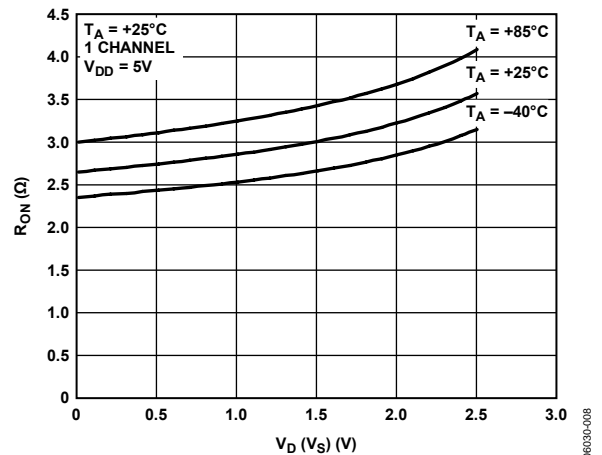


Figure 10. On Resistance vs.  $V_D$  (Vs) for Various Temperatures with 5 V Supply

# ADG793A/ADG793G

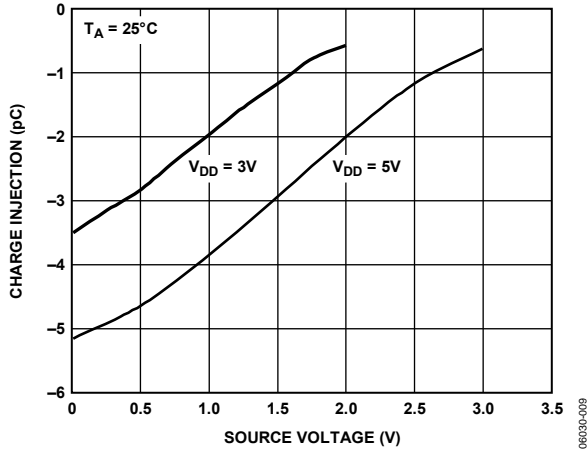


Figure 11. Charge Injection vs. Source Voltage

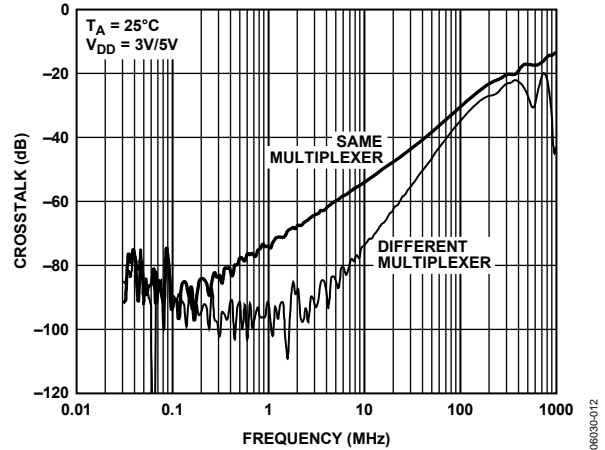


Figure 14. Crosstalk vs. Frequency

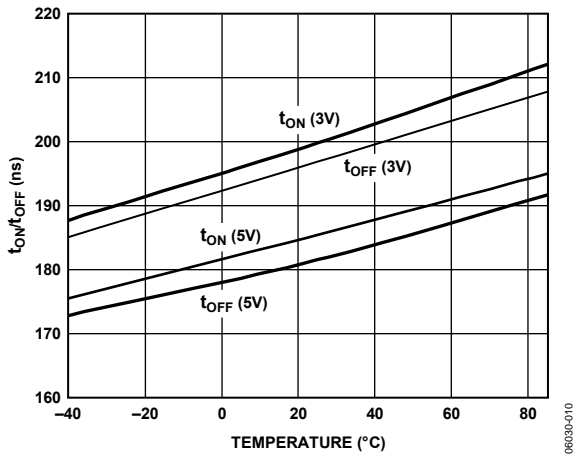


Figure 12.  $t_{ON}/t_{OFF}$  vs. Temperature

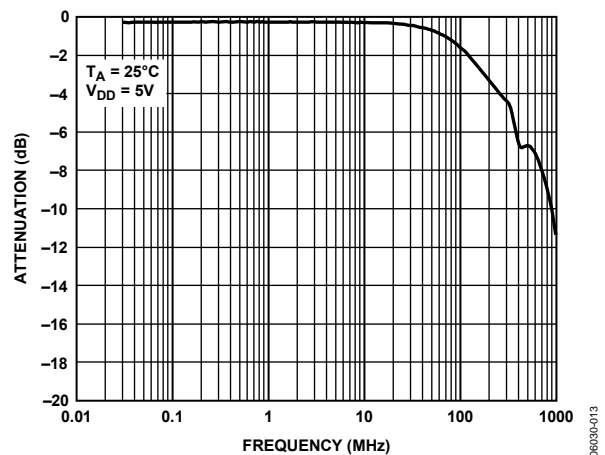


Figure 15. Bandwidth

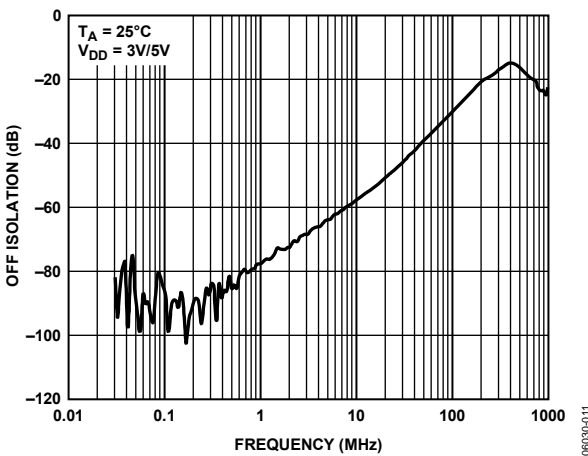


Figure 13. Off Isolation vs. Frequency

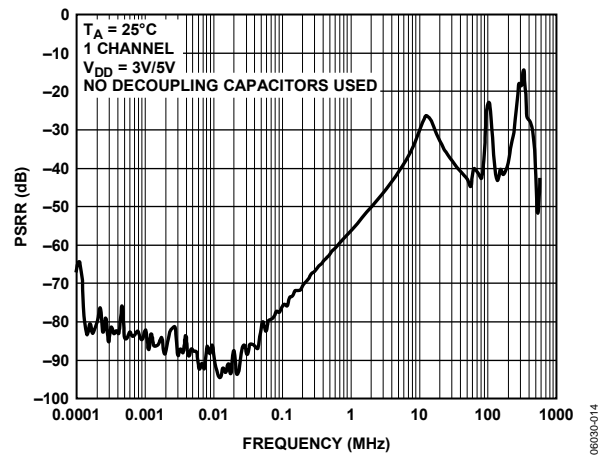


Figure 16. PSRR vs. Frequency

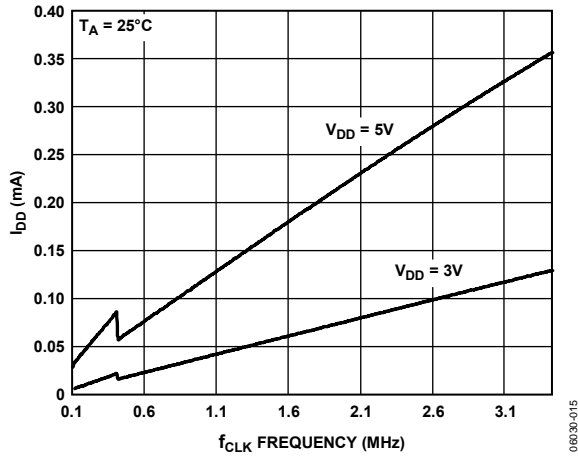


Figure 17.  $I_{DD}$  vs.  $f_{CLK}$  Frequency

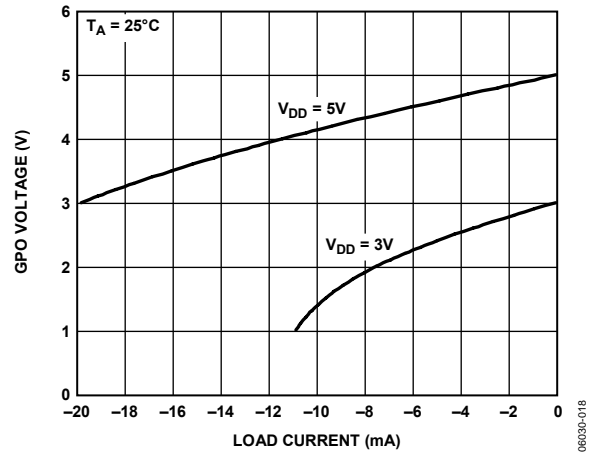


Figure 20. GPO  $V_{OH}$  vs. Load Current

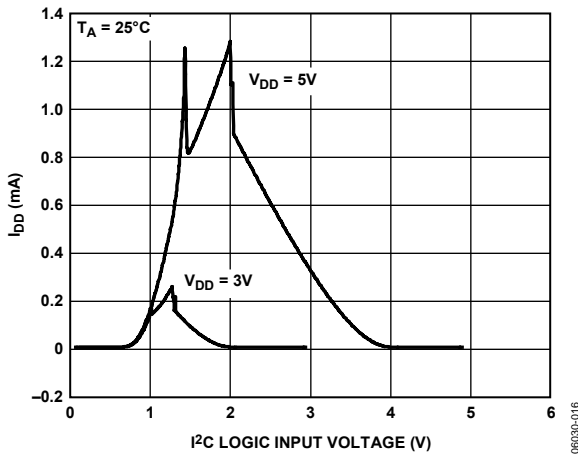


Figure 18.  $I_{DD}$  vs.  $I^2C$  Logic Input Voltage (SDA, SCL)

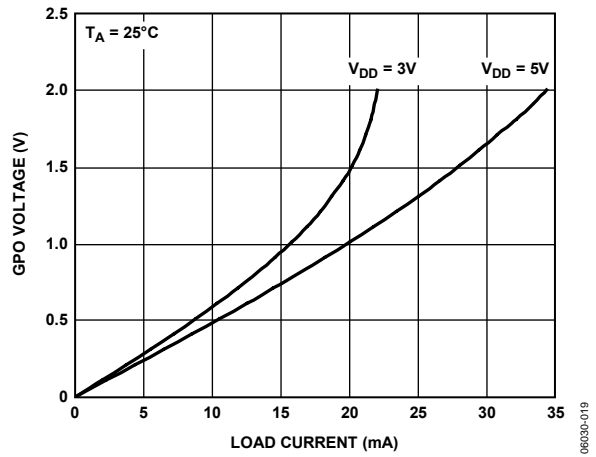


Figure 21. GPO  $V_{OL}$  vs. Load Current

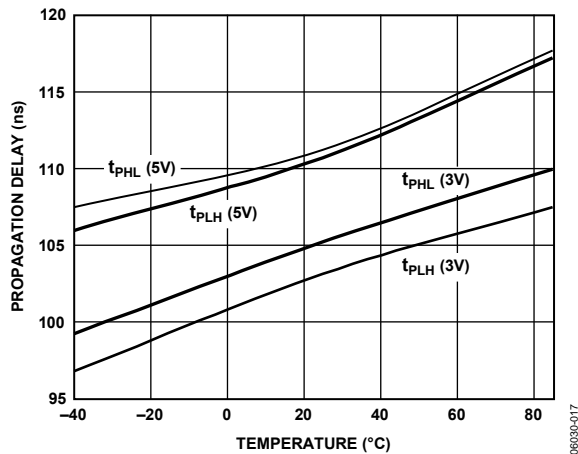


Figure 19.  $I^2C$ -to-GPO Propagation Delay vs. Temperature

## TEST CIRCUITS

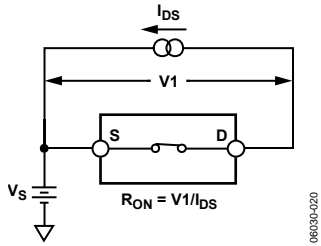


Figure 22. On Resistance

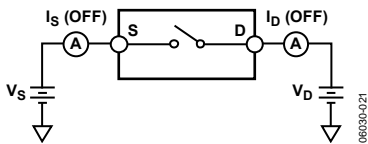


Figure 23. Off Leakage

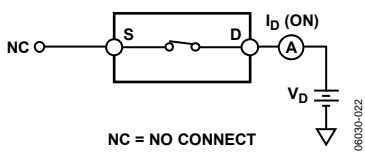


Figure 24. On Leakage

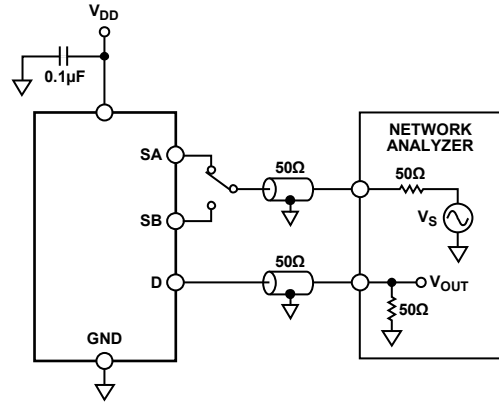


Figure 25. Bandwidth

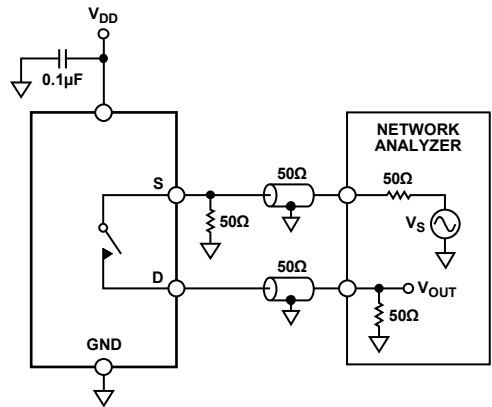


Figure 26. Off Isolation

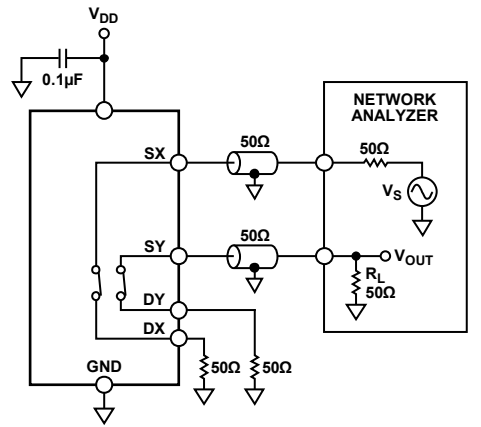


Figure 27. Channel-to-Channel Crosstalk

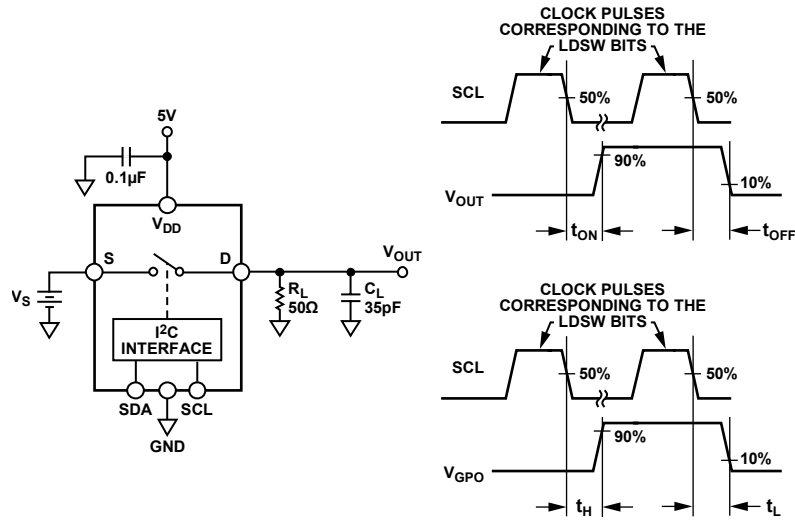


Figure 28. Switching Times

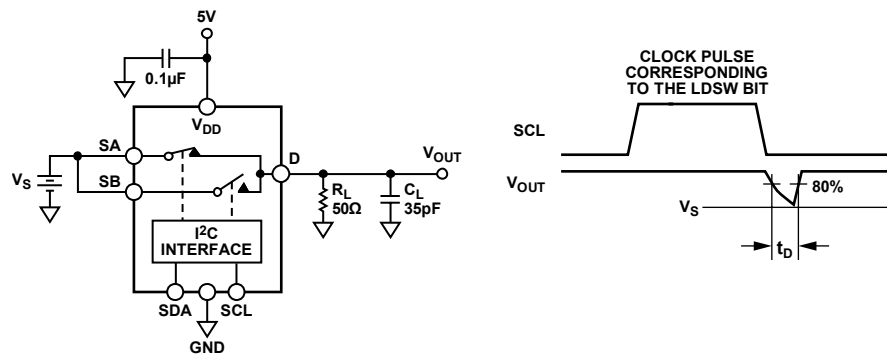


Figure 29. Break-Before-Make Time Delay

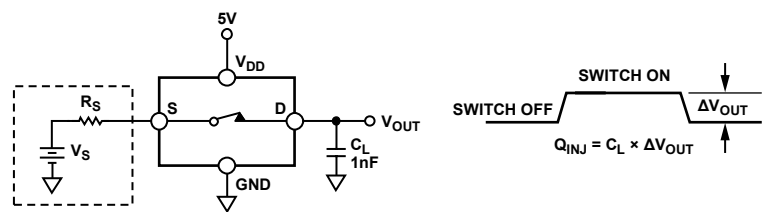


Figure 30. Charge Injection

## TERMINOLOGY

### On Resistance ( $R_{ON}$ )

The series on-channel resistance measured between the S pin and D pin.

### On Resistance Match ( $\Delta R_{ON}$ )

The channel-to-channel matching of on resistance when channels are operated under identical conditions.

### On Resistance Flatness ( $R_{FLAT(ON)}$ )

The variation of on resistance over the specified range produced by the specified analog input voltage change with a constant load current.

### Channel Off Leakage ( $I_{OFF}$ )

The sum of leakage currents into or out of an off channel input.

### Channel On Leakage ( $I_{ON}$ )

The current loss/gain through an on-channel resistance, creating a voltage offset across the device.

### Input Leakage Current ( $I_{IN}$ , $I_{INL}$ , $I_{INH}$ )

The current flowing into a digital input when a specified low level voltage or high level voltage is applied to that input.

### Input/Output Off Capacitance ( $C_{OFF}$ )

The capacitance between an analog input and ground when the switch channel is off.

### Input/Output On Capacitance ( $C_{ON}$ )

The capacitance between the inputs or outputs and ground when the switch channel is on.

### Digital Input Capacitance ( $C_{IN}$ )

The capacitance between a digital input and ground.

### Output On Switching Time ( $t_{ON}$ )

The time required for the switch channel to close. The time is measured from 50% of the falling edge of the LDSW bit to the time the output reaches 90% of the final value.

### Output Off Switching Time ( $t_{OFF}$ )

The time required for the switch to open. The time is measured from 50% of the falling edge of the load switch (LDSW) bit to the time the output reaches 10% of the final value.

### I<sup>2</sup>C-to-GPO Propagation Delay ( $t_H$ , $t_L$ )

The time required for the logic value at the GPO pin to settle after loading a GPO command. The time is measured from 50% of the falling edge of the LDSW bit to the time the output reaches 90% of the final value for high and 10% for low.

### Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

### -3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

### Off Isolation

The measure of unwanted signal coupling through an off switch.

### Crosstalk

The measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Charge Injection

The measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

### Differential Gain Error

The measure of how much color saturation shift occurs when the luminance level changes. Both attenuation and amplification can occur; therefore, the largest amplitude change between any two levels is specified and expressed in percent (%).

### Differential Phase Error

The measure of how much hue shift occurs when the luminance level changes. It can be a negative or positive value and is expressed in degrees of subcarrier phase.

### Input High Voltage ( $V_{INH}$ )

The minimum input voltage for Logic 1.

### Input Low Voltage ( $V_{INL}$ )

The maximum input voltage for Logic 0.

### Output High Voltage ( $V_{OH}$ )

The minimum output voltage for Logic 1.

### Output Low Voltage ( $V_{OL}$ )

The maximum output voltage for Logic 0.

### $I_{DD}$

Positive supply current.



## THEORY OF OPERATION

The ADG793A/ADG793G are monolithic CMOS devices comprising three 3:1 multiplexers/demultiplexers controllable via a standard I<sup>2</sup>C serial interface. The CMOS process provides ultralow power dissipation, yet gives high switching speed and low on resistance.

The on-resistance profile is very flat over the full analog input range, and the wide bandwidth ensures excellent linearity and low distortion. These features, combined with a wide input signal range make the ADG793A/ADG793G the ideal switching solution for a wide range of TV applications.

The switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The integrated serial I<sup>2</sup>C interface controls the operation of the multiplexers and general-purpose logic pins (ADG793G only).

The ADG793A/ADG793G has many attractive features, such as the ability to individually control each multiplexer, the option of reading back the status of any switch, and two general purpose logic output pins controllable through the I<sup>2</sup>C interface. The following sections describe these features in more detail.

### I<sup>2</sup>C SERIAL INTERFACE

The ADG793A/ADG793G are controlled via an I<sup>2</sup>C-compatible serial bus interface (refer to the *I<sup>2</sup>C-Bus Specification* available from Philips Semiconductor) that allows the part to operate as a slave device (no clock is generated by the ADG793A/ADG793G). The communication protocol between the I<sup>2</sup>C master and the device operates as follows.

1. The master initiates data transfer by establishing a start condition defined as a high-to-low transition on the SDA line while SCL is high. This indicates that an address/data stream follows. All slave devices connected to the bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/W bit. This bit determines the direction of the data flow during the communication between the master and the addressed slave device.
2. The slave device whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit).  
At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register. If the R/W bit is set high, the master reads from the slave device. However, if the R/W bit is set low, the master writes to the slave device.

3. Data transmits over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of the clock signal, SCL, and remain stable during the high period of SCL, because a low-to-high transition when the clock signal is high can be interpreted as a stop event which ends the communication between the master and the addressed slave device.
4. After transferring all data bytes, the master establishes a stop condition, defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (the SDA line remains high). The master brings the SDA line low before the tenth clock pulse and then high during the tenth clock pulse to establish a stop condition.

### I<sup>2</sup>C ADDRESS

The ADG793A/ADG793G have a 7-bit I<sup>2</sup>C address. The four most significant bits are internally hardwired and the last three bits A0, A1, and A2 are user-adjustable. This allows the user to connect up to eight ADG793As/ADG793Gs to the same bus. The I<sup>2</sup>C bit map shows the configuration of the 7-bit address.

#### 7-Bit I<sup>2</sup>C Address Bit Configuration

MSB				LSB		
1	0	1	0	A2	A1	A0

### WRITE OPERATION

When writing to the ADG793A/ADG793G, the user must begin with an address byte and R/W bit, after which time the switch acknowledges that it is prepared to receive data by pulling SDA low. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCL. Figure 31 illustrates the entire write sequence for the ADG793A/ADG793G. The first data byte (AX7 to AX0) controls the status of the switches and the LDSW and RESETB bits from the second byte control the operation mode of the device. Table 6 shows a list of all commands supported by the ADG793A/ADG793G with the corresponding byte that needs to be loaded during a write operation.

To achieve the desired configuration, one or more commands can be loaded into the device. Any combination of the commands in Table 6 can be used with these restrictions:

- Only one switch from a given multiplexer can be on at any given time.
- When a sequence of successive commands affect the same element (that is, the switch or GPO pin), only the last command is executed.

# ADG793A/ADG793G

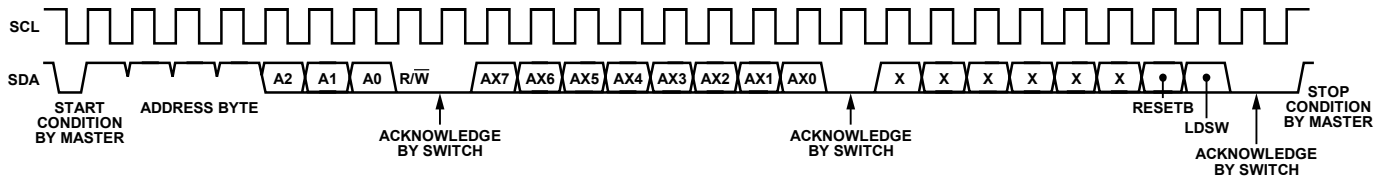


Figure 31. Write Operation

Table 6. ADG793A/ADG793G Command List

AX7	AX6	AX5	AX4	AX3	AX2	AX1	AX0	Addressed Switch/GPO Pin
0	1	0	0	0	0	0	0	S1A/D1, S2A/D2, S3A/D3 off
1	1	0	0	0	0	0	0	S1A/D1, S2A/D2, S3A/D3 on
0	1	0	0	0	0	0	1	S1B/D1, S2B/D2, S3B/D3 off
1	1	0	0	0	0	0	1	S1B/D1, S2B/D2, S3B/D3 on
0	1	0	0	0	0	1	0	S1C/D1, S2C/D2, S3C/D3 off
1	1	0	0	0	0	1	0	S1C/D1, S2C/D2, S3C/D3 on
X <sup>1</sup>	1	0	0	0	0	1	1	Reserved
0	1	0	0	0	1	0	0	S1A/D1 off
1	1	0	0	0	1	0	0	S1A/D1 on
0	1	0	0	0	1	0	1	S1B/D1 off
1	1	0	0	0	1	0	1	S1B/D1 on
0	1	0	0	0	1	1	0	S1C/D1 off
1	1	0	0	0	1	1	0	S1C/D1 on
X <sup>1</sup>	1	0	0	0	1	1	1	Reserved
0	1	0	0	1	0	0	0	S2A/D2 off
1	1	0	0	1	0	0	0	S2A/D2 on
0	1	0	0	1	0	0	1	S2B/D2 off
1	1	0	0	1	0	0	1	S2B/D2 on
0	1	0	0	1	0	1	0	S2C/D2 off
1	1	0	0	1	0	1	0	S2C/D2 on
X <sup>1</sup>	1	0	0	1	0	1	1	Reserved
0	1	0	0	1	1	0	0	S3A/D3 off
1	1	0	0	1	1	0	0	S3A/D3 on
0	1	0	0	1	1	0	1	S3B/D3 off
1	1	0	0	1	1	0	1	S3B/D3 on
0	1	0	0	1	1	1	0	S3/C/D3 off
1	1	0	0	1	1	1	0	S3/C/D3 on
X <sup>1</sup>	1	0	0	1	1	1	1	Reserved
X <sup>1</sup>	1	0	1	0	0	0	0	Mux 1 disabled (all switches connected to D1 are off)
X <sup>1</sup>	1	0	1	0	0	0	1	Mux 2 disabled (all switches connected to D2 are off)
X <sup>1</sup>	1	0	1	0	0	1	0	Mux 3 disabled (all switches connected to D3 are off)
0	1	0	1	0	0	1	1	Reserved for ADG793A/GPO1 low for ADG793G
1	1	0	1	0	0	1	1	Reserved for ADG793A/GPO1 high for ADG793G
0	1	0	1	0	1	0	0	Reserved for ADG793A/GPO2 low for ADG793G
1	1	0	1	0	1	0	0	Reserved for ADG793A/GPO2 high for ADG793G
0	1	0	1	0	1	0	1	Reserved for ADG793A/GPO1, GPO2 low for ADG793G
1	1	0	1	0	1	0	1	Reserved for ADG793A/GPO1, GPO2 high for ADG793G
0	1	0	1	1	1	1	1	All muxes disabled (all switches are off)
1	1	0	1	1	1	1	1	Reserved

<sup>1</sup>X = Logic state does not matter.



# ADG793A/ADG793G

## EVALUATION BOARD

The ADG793G evaluation kit allows designers to evaluate the high performance of the device with a minimum of effort.

The evaluation kit includes a printed circuit board populated with the ADG793G. The evaluation board can be used to evaluate the performance of both the ADG793A and ADG793G. It interfaces to the USB port of a PC, or it can be used as a standalone evaluation board.

Software is available with the evaluation board that allows the user to program the ADG793G easily through the USB port. The software runs on any PC that has Microsoft® Windows® 2000 or Windows XP installed with a minimum screen resolution of 1200 × 768. See Figure 33 and Figure 34 for schematics of the evaluation board.

## USING THE ADG793G EVALUATION BOARD

The ADG793G evaluation kit is a test system designed to simplify the evaluation of the device. Each input/output of the part comes with a socket specifically chosen for easy audio/video evaluation. An evaluation board data sheet is also available and provides full instructions for operating the evaluation board.

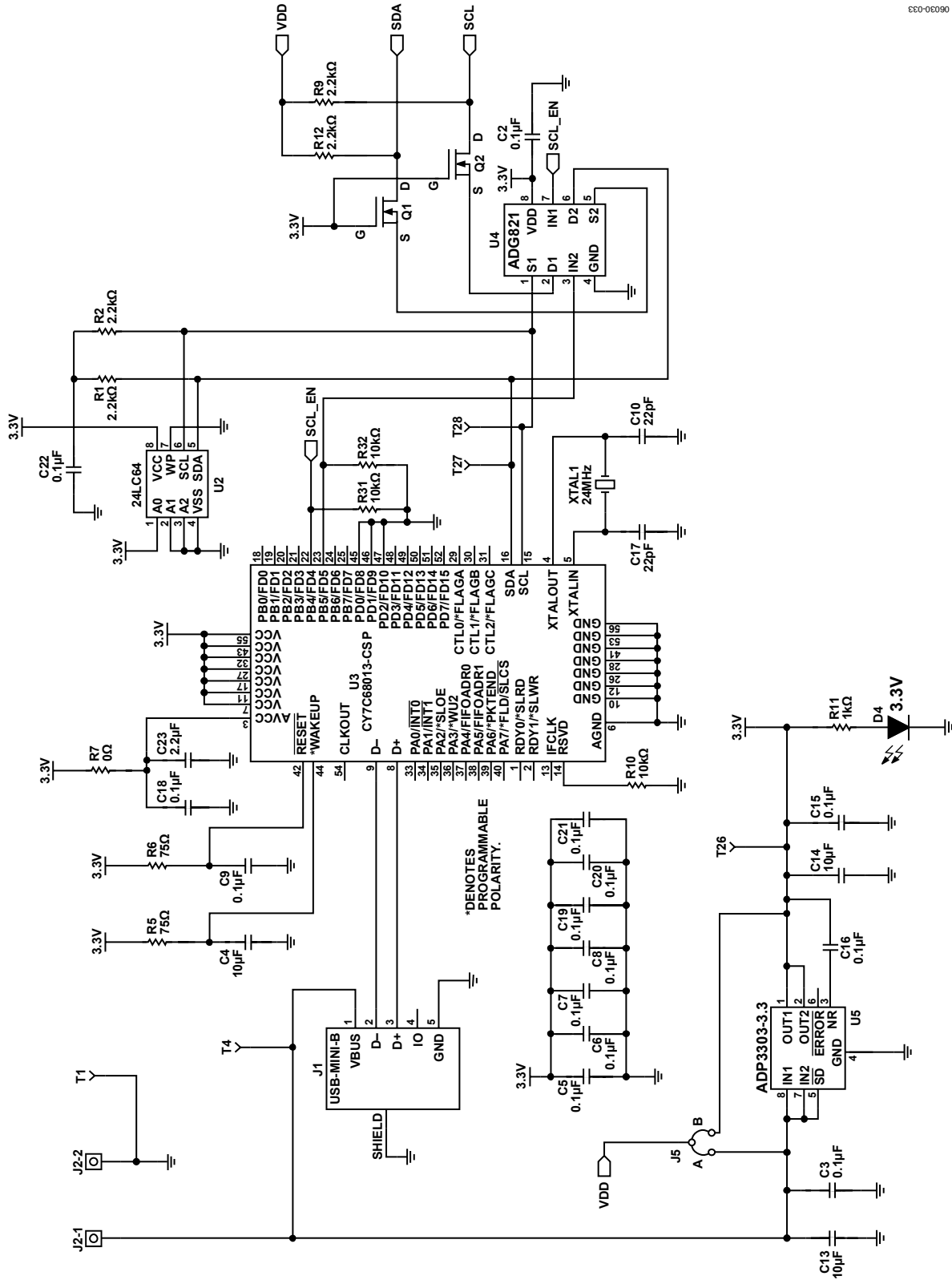


Figure 33. EVAL-ADG793GEB Schematic, USB Controller Section

# ADG793A/ADG793G

06030-034

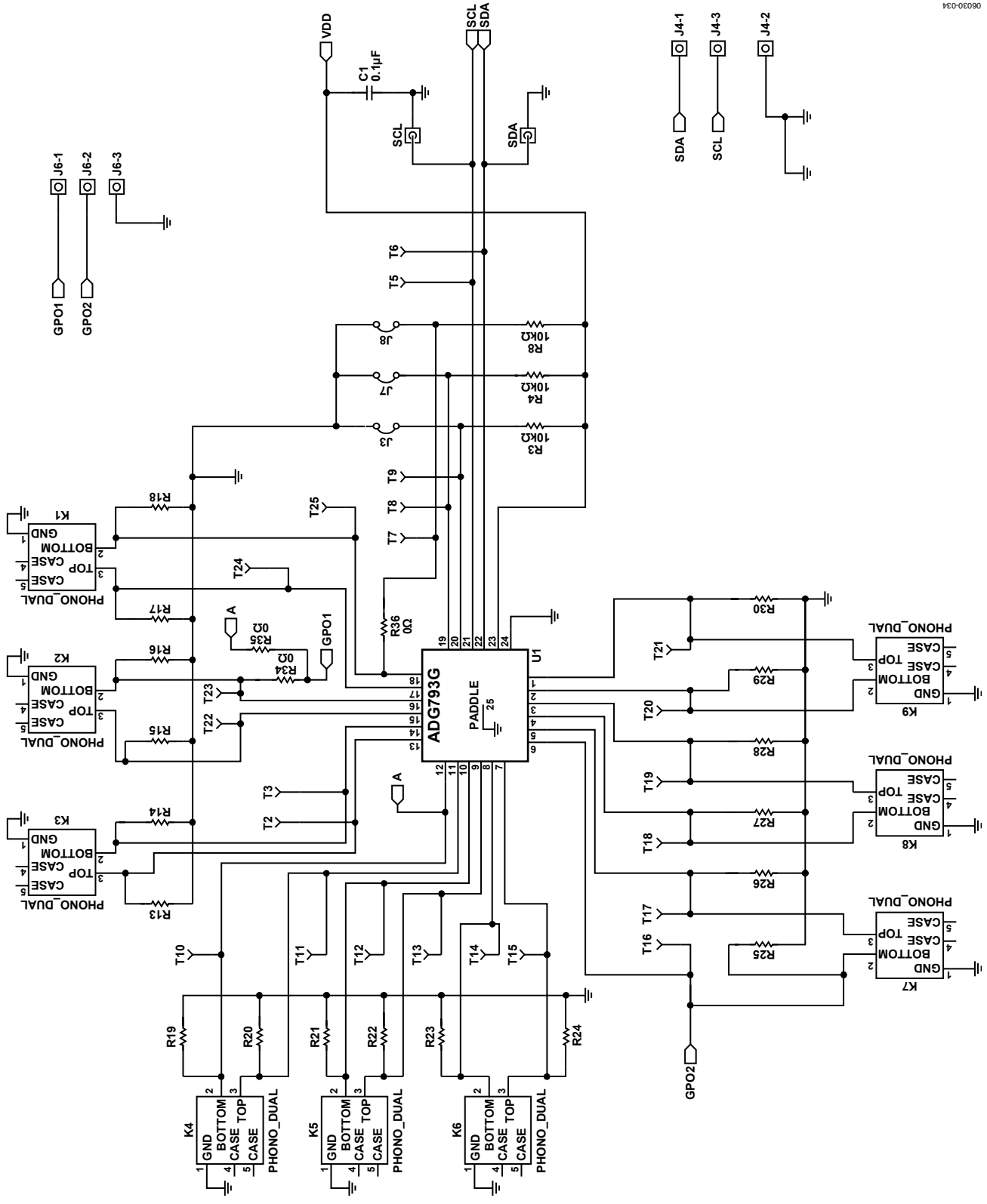
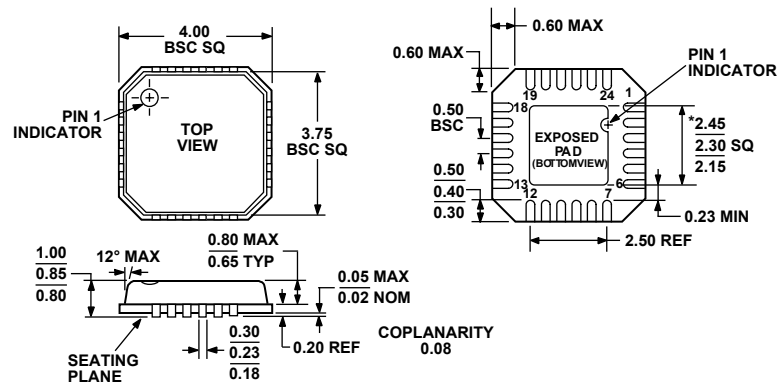


Figure 34. EVAL-ADG793GEB Schematic, Chip Section

## OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2  
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 35. 24-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm × 4 mm Body, Very Thin Quad  
(CP-24-2)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	I <sup>2</sup> C Speed	Package Description	Package Option
ADG793ABCPZ-REEL <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz	24-Lead LFCSP_VQ	CP-24-2
ADG793ABCPZ-500RL7 <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz	24-Lead LFCSP_VQ	CP-24-2
ADG793ACCPZ-REEL <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz, 3.4 MHz	24-Lead LFCSP_VQ	CP-24-2
ADG793ACCPZ-500RL7 <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz, 3.4 MHz	24-Lead LFCSP_VQ	CP-24-2
ADG793GBCPZ-REEL <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz	24-Lead LFCSP_VQ	CP-24-2
ADG793GBCPZ-500RL7 <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz	24-Lead LFCSP_VQ	CP-24-2
ADG793GCCPZ-REEL <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz, 3.4 MHz	24-Lead LFCSP_VQ	CP-24-2
ADG793GCCPZ-500RL7 <sup>1</sup>	-40°C to +85°C	100 kHz, 400 kHz, 3.4 MHz	24-Lead LFCSP_VQ	CP-24-2
EVAL-ADG793GEB <sup>2</sup>			Evaluation Board	

<sup>1</sup> Z = Pb-free part.

<sup>2</sup> Evaluation board is RoHS compliant.

**NOTES**

Purchase of licensed I<sup>2</sup>C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.