PIC18F87K22 FAMILY

PIC18F87K22 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87K22 family devices that you have received conform functionally to the current Device Data Sheet (DS39960**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87K22 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B5, C6**).

Data Sheet clarifications and corrections start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87K22 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)							
		A3	B1	B3	B5	C1	C3	C5	C6
PIC18F65K22	530h	3h	4h	5h	6h	10h	11h	12h	13h
PIC18F66K22	52Ch								
PIC18F85K22	536h								
PIC18F86K22	532h								
PIC18F67K22	518h								
PIC18F87K22	51Ch								

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XKXX/8XKXX Family Flash Microcontroller Programming Specification"* (DS39947) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)							
				A3	B1	B3	B5	C1	C3	C5	C6
Analog-to-Digital Converter (A/D)	A/D Offset	1.1	The A/D offset is greater than specified in the data sheet's A/D Converter Characteristics table.	X							
Analog-to-Digital Converter (A/D)	A/D Offset	1.2	The A/D offset is greater than specified in the data sheet's A/D Converter Characteristics table.		X	X	X	X	X	X	X
Ports	Leakage	2.	I/O port leakage is higher than the D060 spec in the data sheet.	X	X	X	X	X	X	X	X
High/Low-Voltage Detect (HLVD)	HLVD Trip	3.	The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts.	X	X	X	X	X	X	X	X
ECCP	Auto-Shutdown	4.	The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state.	X	X	X	X	X	X	X	X
EUSART	Synchronous Transmit	5.	When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted.	X	X	X	X	X	X	X	X
IPD and IDD	Maximum Limit	6.	Maximum current limits may be higher than specified in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial)"** of the data sheet.	X							
Ultra Low-Power Sleep	Sleep Entry	7.1	Entering Ultra Low-Power Sleep mode, by setting RETEN = 0 and SRETEN = 1, will cause the part not to be programmable through ICSP™.	X	X			X			
Ultra Low-Power Sleep	WDT Wake-up	7.2	Using the WDT to exit Ultra Low-Power Sleep mode when VDD>4.5V can cause the part to enter a Reset state requiring POR to exit.	X	X	X	X	X	X	X	X
Resets (BOR)	Enable/Disable	8.	An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled, when the High/Low-Voltage Detection (HLVD) module is not enabled (HLVDCON<4> = 0).	X	X	X	X	X	X	X	X
RG5 Pin	Leakage	9.	RG5 will cause excess pin leakage whenever it is driven low.		X						
External Memory Bus (EMB)	Wait States	10.	The CE signal will not be extended properly if Wait states are used.	X	X	X		X	X		
Primary Oscillator	XT Mode	11.	XT Primary Oscillator mode does not reliably function when the driving crystals are above 3 MHz.	X	X	X		X	X		
Timer1/3/5/7	Interrupt	12.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X		X	X	X	

Note 1: Only those issues indicated in the columns labeled B3 and C3 apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)							
				A3	B1	B3	B5	C1	C3	C5	C6
MSSP1	SPI Slave	13.	Slave samples SDI on both rising and falling edges of SCK.		X	X	X	X	X	X	X

Note 1: Only those issues indicated in the columns labeled B3 and C3 apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B5, C6**).

1. Module: Analog-to-Digital Converter (A/D)

1.1 The A/D will not meet the Microchip standard A/D specification. The A/D may be usable if tested at the user end. The possible issues are high offset error, high DNL error and multiple missing codes. The A/D can be tested and used for relative measurements.

A/D Offset

The A/D may have a high offset error, up to a maximum of 50 LSB; it can be used if the A/D is calibrated for the offset.

Work around

Method to Calibrate for Offset:

In Single-Ended mode, connect the A/D +ve input to ground and take the A/D reading. This will be the offset of the device and can be used to compensate for the subsequent A/D readings on the actual inputs.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X								

1.2 The A/D will meet the Microchip standard A/D specification when used as a 10-bit A/D. When used as a 12-bit A/D, the possible issues include high offset error (up to a maximum of ±25 LSBs at 25°C, ±30 LSBs at 85°C, 125°C and -40°C), high DNL error (up to a maximum of ±4 LSBs) and multiple missing codes (up to a maximum of 20). Users should evaluate the 12-bit A/D performance in their application using the suggested work around below. See Table 3 for guidance specifications.

A/D Offset:

The A/D may have high offset error, up to a maximum of ±25 LSBs at 25°C, ±30 LSBs at 85°C, 125°C and -40°C; it can be used if the A/D is calibrated for the offset.

Work around

Method to Calibrate for Offset:

In Single-Ended mode, connect A/D +ve input to ground and take the A/D reading. This will be the offset of the device and can be used to compensate for the subsequent A/D readings on the actual inputs.

TABLE 3: A/D CONVERTER CHARACTERISTICS

Param. No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
A01	NR	Resolution	—	—	12	bit	ΔVREF ≥ 5.0V
A03	EIL	Integral Linearity Error	—	—	±10.0	LSb	ΔVREF ≥ 5.0V
A04	EDL	Differential Linearity Error	—	—	+6.0/-4.0	LSb	ΔVREF ≥ 5.0V
A06	EOFF	Offset Error	—	—	±25	LSb	ΔVREF ≥ 5.0V, Temperature: 25°C
			—	—	±30	LSb	ΔVREF ≥ 5.0V, Temperature: ≥ 85°C, -40°C
A07	EGN	Gain Error	—	—	±15	LSb	ΔVREF ≥ 5.0V
A10	—	Monotonicity(1)	—				VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	AVDD – AVSS	V	
A21	VREFH	Reference Voltage High	AVSS + 3.0V	—	AVDD + 0.3V	V	
A22	VREFL	Reference Voltage Low	AVSS – 0.3V	—	AVDD – 3.0V	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
	X	X	X	X	X	X	X	

2. Module: Ports

The input leakage will not match the D060 specification in the data sheet. The leakage will meet the 200 nA specification at T_A = 25°C. At T_A = 85°C, the leakage will be up to a maximum of 2 µA.

Work around

None.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

3. Module: High/Low-Voltage Detect (HLVD)

The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts. High trip points that are close to the intended operating voltage are susceptible to this behavior.

Work around

Select a lower trip voltage that allows consistent start-up or clear any initial interrupts from the HLVD on start-up.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

4. Module: ECCP

The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

None.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

5. Module: EUSART

When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted. One or more bits of the intended transmit message may be incorrect.

Work around

Since this problem is related to the baud rate used, adding a fixed delay before loading the TXREGx may not be a reliable work around. Lower the baud rate until no errors occur, or when loading the TXREGx, check that the TRMT bit inside of the TXSTAx register is set instead of checking the TXxIF bit.The following code can be used:

EXAMPLE 1: EUSART SYNCHRONOUS TRANSMIT WORK AROUND

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

6. Module: IPD and IDD

The IPD and IDD limits will not match the data sheet. The values, in bold in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial)"**, reflect the updated silicon maximum limits.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial)

PIC18F87K22 Family (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature: -40°C ≤ TA ≤ +85°C for industrial					
Param. No.	**Device**	**Typ.**	**Max.**	**Units**	**Conditions**		
	Power-Down Current (IPD)(1)						
	All devices	10	500	nA	-40°C	VDD = 1.8V(4) (Sleep mode) Regulator Disabled	
		20	500	nA	+25°C		
		120	600	nA	+60°C		
		630	**2000**	nA	+85°C		
	All devices	50	700	nA	-40°C	VDD = 3.3V(4) (Sleep mode) Regulator Disabled	
		60	**900**	nA	+25°C		
		170	**1100**	nA	+60°C		
		700	**5000**	nA	+85°C		
	All devices	350	1300	nA	-40°C	VDD = 5V(5) (Sleep mode) Regulator Enabled	
		400	1400	nA	+25°C		
		550	1500	nA	+60°C		
		1350	4000	nA	+85°C		
	Supply Current (IDD) Cont.(2,3)						
	All devices	3.7	8.5	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_RUN** mode, SOSCSEL = 01)
		5.4	10	µA	+25°C		
		6.6	13	µA	+85°C		
	All devices	8.7	18	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		10	20	µA	+25°C		
		12	**35**	µA	+85°C		
	All devices	60	160	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		90	190	µA	+25°C		
		100	240	µA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{RETEN}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0).

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial) (Continued)

PIC18F87K22 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for industrial					
Param. No.	**Device**	**Typ.**	**Max.**	**Units**	**Conditions**		
	All devices	1.2	4	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_IDLE** mode, SOSCSEL = 01)
		1.7	5	µA	+25°C		
		2.6	6	µA	+85°C		
	All devices	1.6	7	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		2.8	9	µA	+25°C		
		4.1	**17**	µA	+85°C		
	All devices	60	150	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		80	180	µA	+25°C		
		100	240	µA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{RETEN}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0).

Work around

None.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X								

7. Module: Ultra Low-Power Sleep

7.1 Entering Ultra Low-Power Sleep mode, by setting RETEN = 0 and SRETEN = 1, will cause the part to not be programmable through ICSP™. This issue occurs when the RETEN fuse bit in CONFIG1L<0> is cleared to '0', the SRETEN bit in the WDTCON register is set to '1' and a SLEEP instruction is executed. This happens within the first 350 µs of code execution or whenever the above Sleep mode is entered and MCLR is disabled. Discontinue use of the MCLR disabled RG5 mode if ICSP™ reprogramming is necessary.

Work around

Use normal Sleep and Low-Power Sleep modes only, or on any Reset, ensure that at least 350 µs passes before executing a SLEEP instruction when ULP is enabled. To ensure the Ultra Low- Power Sleep mode is not enabled, the RETEN fuse bit in CONFIG1L<0> should be set to a '1', and the SRETEN bit in the WDTCON register should be cleared to a '0'. The following code can be used:

EXAMPLE 2: ULTRA LOW-POWER SLEEP WORK AROUND

```
//This will ensure the RETEN fuse is set
to 1
#pragma config RETEN = OFF
//This will ensure the SRETEN bit is 0
WDTCONbits.SRETEN = 0;
```

If the Ultra Low-Power Sleep mode is needed, then the user must ensure that the minimum time, before the first SLEEP instruction is executed, is greater than 350 µs.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X			X				

7.2 Using the WDT to exit Ultra Low-Power Sleep mode when V_{DD}>4.5V can cause the part to enter a Reset state that requires a POR to exit. The issue occurs when the RETEN fuse bit in CONFIG1L<0> is cleared to '0', the SRETEN bit in the WDTCON register is set to '1', V_{DD}>4.5V. Upon entering the failure state, the device ceases to respond to MCLR events and will only exit the Reset state upon experiencing a POR.

Work around

Do not use the Ultra Low-Power Sleep mode with V_{DD} above 4.5V.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

8. Module: Resets (BOR)

An unexpected Reset may occur if the Brown-out Reset (BOR) module is disabled, and then re-enabled when the High/ Low-Voltage Detection (HLVD) module is not enabled (HLVDCON<4> = 0). This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required, and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the HLVD (HLVDCON<4> = 1) prior to entering Sleep. If power consumption is an issue and low power is desired, do not use BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN (RCON<6> = 0).

   ```
   WDTCONbits.SBOREN = 0;
   ```

2. Enter Sleep mode (if desired).

   ```
   Sleep();
   ```

3. After exiting Sleep mode (if entered), enable the HLVD (HLVDCON<4> = 1).

   ```
   HLVDCONbits.HLVDEN = 1;
   ```

4. Wait for the internal reference voltage (TIRVST) to stabilize (typically 25 µs).

   ```
   while(!HLVDCONbits.IRVST);
   ```

5. Re-enable BOR by setting SBOREN (RCON<6> = 1).

   ```
   WDTCONbits.SBOREN = 1;
   ```

6. Disable the HLVD by clearing HLVDEN (HLVDCON<4> = 0).

   ```
   HLVDCONbits.HLVDEN = 0;
   ```

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X	X	X	X	X	X	

9. Module: RG5 Pin

RG5 will cause excess pin leakage whenever it is driven low. When RG5 is held at 0V, the pin will typically source an additional 160 µA of current.

Work around

In power-sensitive applications, using RG5 as an input, ensure that any input attached to this pin Idles high.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
	X							

10. Module: External Memory Bus (EMB)

The CE signal will not be extended properly if Wait states are used. The duration of the CE signal will remain 0 TCY despite the setting in MEMCON<5:4>.

Work around

None.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
X	X	X		X	X			

11. Module: Primary Oscillator (XT Mode)

On some parts, using the XT oscillator at the top end of its specified frequency range (3.0-4.0 MHz) may cause the part to cease driving the oscillator.

Work around

Use XT mode only for frequencies lower than 3.0 MHz.

Use HS mode if frequencies greater than 3.0 MHz on a crystal oscillator are required.

Affected Silicon Revisions

A1	B1	B3	B5	C1	C3	C5	C6	
X	X	X		X	X			

12. Module: Timer1/3/5/7

When Timer1, Timer3, Timer5 or Tmer7 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 3.

EXAMPLE 3: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A1	B1	B3	B5	C1	C3	C5	C6	
X	X	X		X	X	X		

13. Module: MSSP1

MSSP1 SPI Slave samples SDI on rising and falling edges of SCK.

The MSSP1 SPI in Slave mode improperly samples the SDI data input on both the rising and falling edges of the SCK clock input. This results in unexpected receive data.

Work around

Use MSSP2 for slave SPI operation.

Affected Silicon Revisions

A3	B1	B3	B5	C1	C3	C5	C6	
	X	X	X	X	X	X	X	

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39960**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Table 31-27: A/D Converter Characteristics has been corrected. The changes are shown in bold in the table below:

TABLE 31-27: A/D CONVERTER CHARACTERISTICS: PIC18F87K22 FAMILY (INDUSTRIAL)

Param. No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
A01	NR	Resolution	—	—	12	bit	ΔVREF ≥ 5.0V
A03	EIL	Integral Linearity Error	—	±1	±6.0	LSB	ΔVREF ≥ 5.0V
A04	EDL	Differential Linearity Error	—	±1	+3.0/-1.0	LSB	ΔVREF ≥ 5.0V
A06	EOFF	Offset Error	—	±1	**±18.0**	LSB	ΔVREF ≥ 5.0V
A07	EGN	Gain Error	—	±1	±8.0	LSB	ΔVREF ≥ 5.0V
A10	—	Monotonicity(1)	—	—	—	—	VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V	
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V	
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

2. Module: Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

In **Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)"**, the description of the Regulator Disabled mode has changed. The changes are shown in **bold** below:

When the regulator is disabled, the VCAP/VDDCORE pin must only **be tied to a 0.1 µF capacitor**. Refer to **Section 31.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

3. Module: DC Characteristics (Injection Current)

The following table of specifications for current injected into the microcontroller will be added to **Section 31.0 "Electrical Characteristics"**.

31.4 DC Characteristics: PIC18F87K22 Family (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 5.5V Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D160a	IICL	Input Low Injection Current	0	—	-5(1)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO
D160b	IICH	Input High Injection Current	0	—	+5(1)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO
D160c	∑IICT	Total Input Injection Current (sum of all I/O and control pins)	-20(1,2)	—	+20(1,2)	mA	Absolute instantaneous sum of all input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Injection currents > \| 0 \| can affect the A/D results.

2: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted.

4. Module: DC Characteristics (Input Low Voltage and Input High Voltage)

Input Low Voltage and Input High Voltage have been corrected. The changes are shown in bold in the table below:

31.3 DC Characteristics: PIC18F87K22 Family (Industrial/Extended)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O Ports:					
D030		with TTL buffer	**—**	**—**	**0.8**	V	**4.5V ≤ VDD ≤ 5.5V**
D030A			**—**	**—**	**0.15 VDD**	**V**	**VDD ≤ 4.5V**
D031		with Schmitt Trigger buffer	—	**—**	**0.2 VDD**	V	
		with I2C levels	**—**	**—**	**0.3 VDD**	**V**	
		with SMBus levels	**—**	**—**	**0.8**	**V**	**2.7V ≤ VDD ≤ 5.5V**
D032		$\overline{MCLR}$	**—**	**—**	0.2 VDD	V	
D033		OSC1	**—**	**—**	0.2 VDD	V	
D034		SOSCI	**—**	**—**	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O Ports:					
D040		with TTL buffer	2.0	**—**	**—**	V	4.5V ≤ VDD ≤ 5.5V
			0.25 VDD	**—**	**—**	V	**1.8V** ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	**—**	**—**	V	**2.0V ≤ VDD ≤ 5.5V**
		with I2C levels	**0.7 VDD**	**—**	**—**	**V**	
		with SMBus levels	**2.1**	**—**	**—**	**V**	**2.7V ≤ VDD ≤ 5.5V**
D042		$\overline{MCLR}$	0.8 VDD	**—**	**—**	V	
D043		OSC1 **(HS mode)**	**0.7 VDD**	**—**	**—**	V	
D043A		OSC1 (**EC/ECPLL mode)**	**0.8 VDD**	**—**	**—**	V	
D044		SOSCI	0.7 VDD	**—**	**—**	V	

5. Module: Product Identification System

The Product Identification System should be as follows:

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:(1,2)	PIC18F65K22, PIC18F65K22T PIC18F66K22, PIC18F66K22T PIC18F67K22, PIC18F67K22T PIC18F85K22, PIC18F85K22T PIC18F86K22, PIC18F86K22T PIC18F87K22, PIC18F87K22T
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:	PT = TQFP (Plastic Thin Quad Flatpack) MR = QFN (Plastic Quad Flat)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F87K22-I/PT 301 = Industrial temperature, TQFP package, QTP pattern #301.

b) PIC18F87K22T-I/PT = Tape and reel, Industrial temperature, TQFP package

c) PIC18F87K22T-E/PT = Tape and reel, Extended temperature, TQFP package

Note 1: F = Standard Voltage Range
2: T = In tape and reel PLCC and TQFP packages only
3: RSL = Silicon Revision A3 **or later**

6. Module: Oscillator Configurations

The following section should be included in the oscillator section of the data sheet, directly underneath **Section 3.6.4.3 "Compensating with the CCP Module in Capture Mode"**.

3.6.5 LFINTOSC OPERATION IN SLEEP

When the Watchdog Timer (WDT) or Real-Time Clock and Calendar (RTCC) modules are enabled and configured to use the LFINTOSC, the LFINTOSC will continue to run when the device is in Sleep, unlike other internal clock sources.

While in Sleep, the LFINTOSC has two power modes, a High-Power and a Low-Power mode, controlled by the INTOSCSEL bit in the CONFIG1L Configuration Word. The High-Power mode is the same as the LFINTOSC while the part is awake and conforms to the specifications outlined for that oscillator. The Low-Power mode consumes less current, but has a much lower accuracy and is not recommended for timing-sensitive applications.

7. Module: DC Characteristic (Comparator Specifications)

Table 31-2, Parameter D303, Comparator Response Time is incorrect, the correct specifications are as follows:

TABLE 31-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 1.8V ≤ VDD ≤ 5V, -40°C ≤ +125°C (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	40	mV	
D301	VICM	Input Common Mode Voltage	—	—	AVDD - 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time(1)	—	**675**	**1200**	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	µs	

Note 1: Response time measured with one comparator input at (AVDD - 1.5)/2, while the other input transitions from VSS to VDD.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document. Silicon issues 1 (A/D), 2 (BOR), 3 (HLVD) and 4 (Ports).

Rev B Document (12/2010)

Removed silicon issue 2 (Brown-out Reset). Changes were made to silicon issue 3 (HLVD). Added silicon issues 4 (ECCP), 5 (EUSART) and 6 (I_{PD} and I_{DD}).

Rev C Document (4/2011)

Added silicon issues 7 (Ultra Low-Power Sleep), 8 (Resets – BOR) and 9 (RG5 Pin). Removed data sheet clarifications 1-3 (Voltage Regulator Pins – ENVREG and V_{CAP}/V_{DDCORE}). Added data sheet clarification 1 (Electrical Characteristics).

Rev D Document (2/2012)

Added silicon issue 10 (External Memory Bus – EMB). Added data sheet clarifications 2 (Voltage Regulator Pins – ENVREG and V_{CAP}/V_{DDCORE}) and 3 (DC Characteristics – Injection Current).

Rev E Document (10/2012)

Added MPLAB X IDE; Added Silicon Revision C3.

Data Sheet Clarifications: Added Module 4, DC Characteristics (Input Low Voltage and Input High Voltage).

Rev F Document (12/2013)

Added silicon issues 1.2 (Analog-to-Digital Converter) and 11 (Primary Oscillator - XT Mode); Other minor corrections.

Rev G Document (3/2014)

Data Sheet Clarifications: Added Module 5; Other minor corrections.

Rev H Document (9/2014)

Added Module 7.2; Other minor corrections.

Rev J Document (9/2014)

Added silicon revision C5.

Rev K Document (03/2015)

Added silicon revision C6; Other minor corrections.

Added Module 12. Timer1/3/5/7

Data Sheet Clarifications: added Module 6.

Rev L Document (7/2015)

Added silicon revision B5; Other minor corrections.

Rev M Document (9/2016)

Added silicon issue 13 (MSSP1).

Rev N Document (01/2017)

Data Sheet Clarifications: Added Module 7 – DC Characteristic (Comparator Specifications). Other minor corrections.

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