FEUL610Q178-01

ML610Q178
User's Manual

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NOTES

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q178.

The following manuals are also available. Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual for ML610QXXX
Description about the connection between uEASE and ML610QXXX

■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

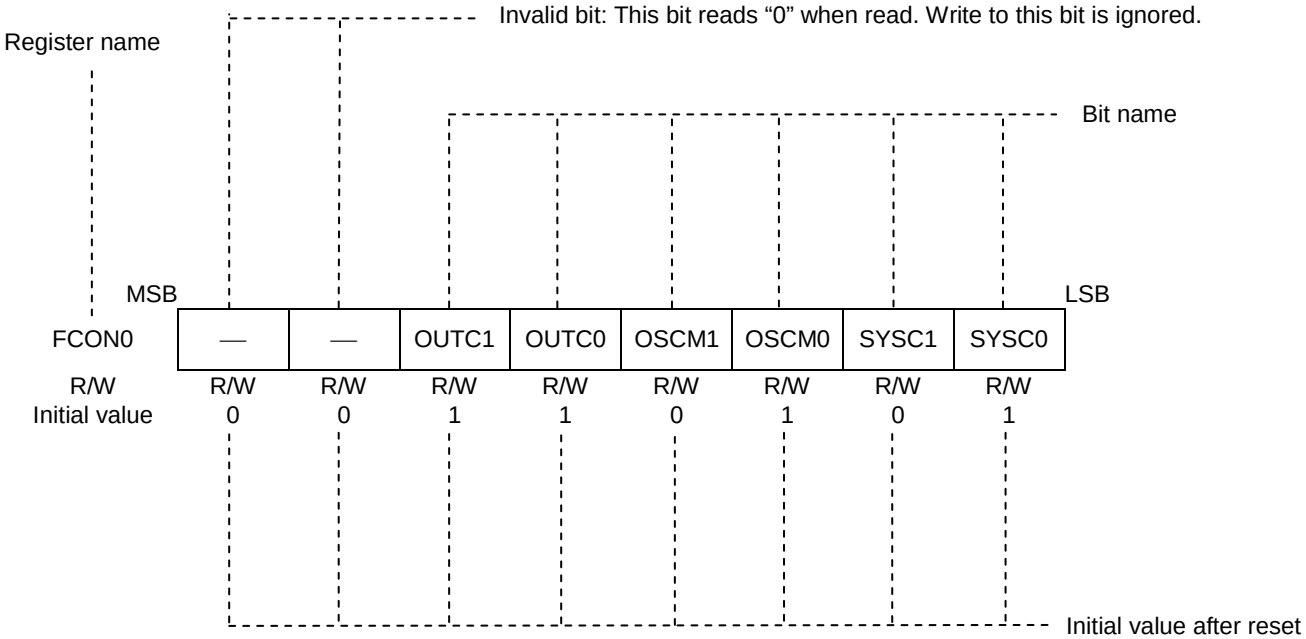


Table of Contents

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 7

Chapter 8

Chapter 9

Chapter 10

Chapter 11

Chapter 12

Chapter 13

Chapter 14

Chapter 15

Chapter 16

Chapter 17

Chapter 18

Chapter 19

Chapter 20

Chapter 21

Chapter 22

Chapter 23

Chapter 24

Chapter 25

Chapter 26

Chapter 27

Chapter 28

Chapter 29

Chapter 30

Chapter 31

Chapter 32

Appendixes

Revision History

Chapter 1

Overview

1. Overview

1.1 Features

Equipped with a 8-bit CPU nX-U8/100, the ML610Q178 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I^2C bus interface (master), Battery level detect circuit, LCD driver. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture.
In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 μs (at 32.768kHz system clock)
    Approx 0.122 μs (at 8.192MHz system clock)@DV_{DD} = 2.2 to 5.5V

- Internal memory
  - Has 128-Kbyte flash ROM(64K × 16-bit) built in. (1K byte of test domain that it cannot be used is included)
  - Has 4-Kbyte RAM (4096 × 8 bits) built in.

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 23 maskable interrupt sources (Internal source: 19, External source: 4)

- Time base counter
  - Low-speed time base counter × 1 channel
  - High-speed time base counter × 1 channel

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 6ch (16-bit configuration available)
  - Clock output is possible for 2ch

- PWM
  - Resolution 16 bits × 2 channel(IGBT control)

- Synchronous serial port
  - 2ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-duplex
  - TXD/RXD × 2 channels
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit /2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode(400kbps@4MHz), Standard mode (100kbps@4MHz)

- Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 16ch (Maximum)
  - Conversion time: 12.75 μs per channel

- General-purpose ports 74（Maximum）
  - Non-maskable interrupt input port × 1ch
  - Input-only port × 6ch
  - Output-only port × 8ch (including secondary functions)
  - Input/output port× 27ch (including secondary functions)
  - Input/output port× 32ch (including selection of LCD)

- LCD driver
  - 160 dots maximum. (40 seg × 4 com), 1/1 to 1/4 duty
  - Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz, 32Hz, 128Hz, 171Hz, 256Hz)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Battery level detect function
  - Judgment voltages: One of 4 levels
  - Judgment accuracy: ±2% (Typ.)

- Reset
  - Reset through the RESET_N pin
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock:
    Crystal oscillation (32.768 kHz), Built-in RC oscillation (32.7kHz)
  - High-speed clock
    Built-in PLL oscillation, Crystal / ceramic oscillation (8MHz), external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)

  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

- Shipment
  - 100-pin QFP (QFP100-P-1420-0.65-BK)
    ML610Q178-xxxGA (blank product: ML610Q178-NNNGA)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: −40°C to 85°C
  - Operating voltage: V_{DD} =2.2V to 5.5V,V_{REF}= 4.5V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML610Q178

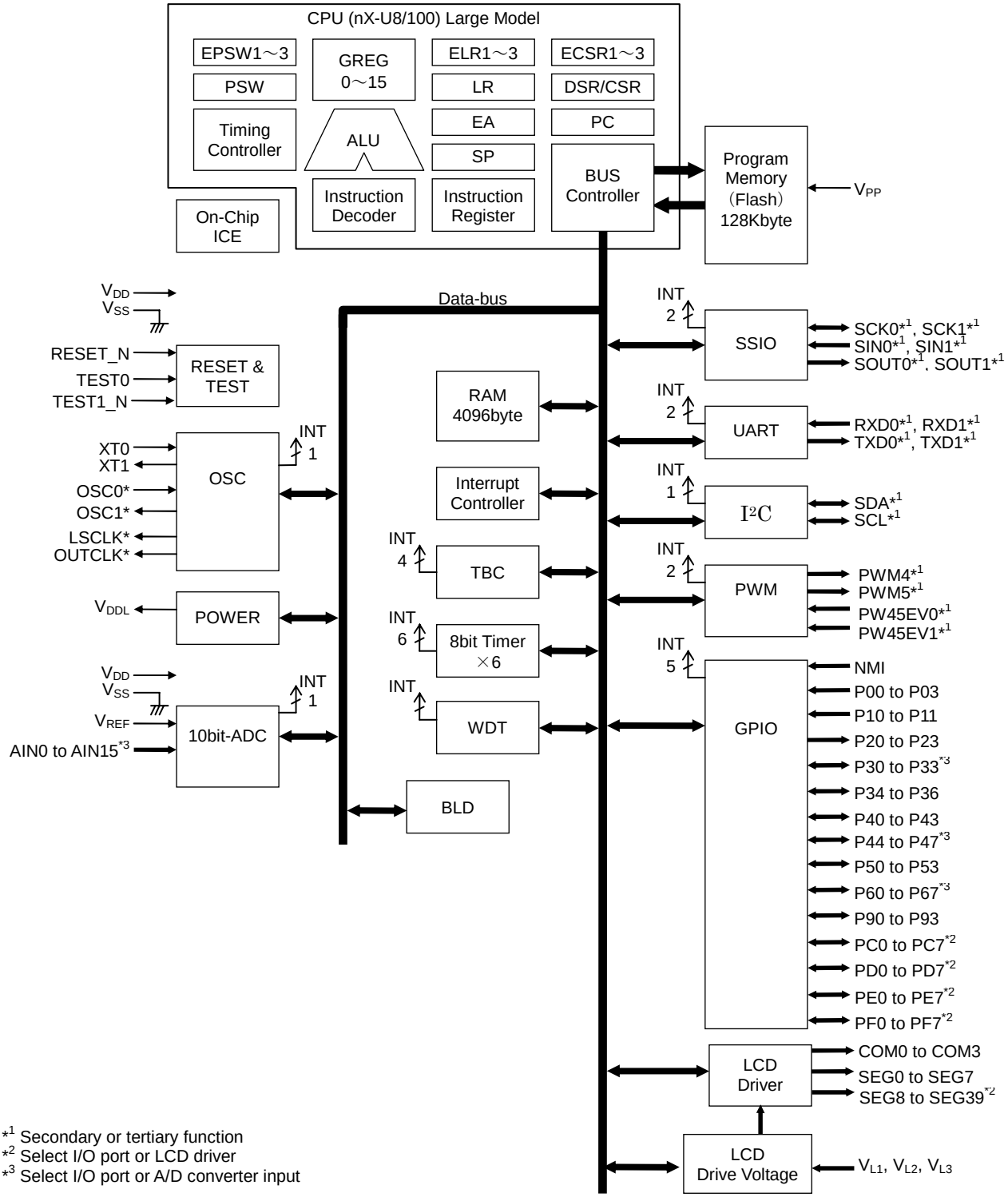
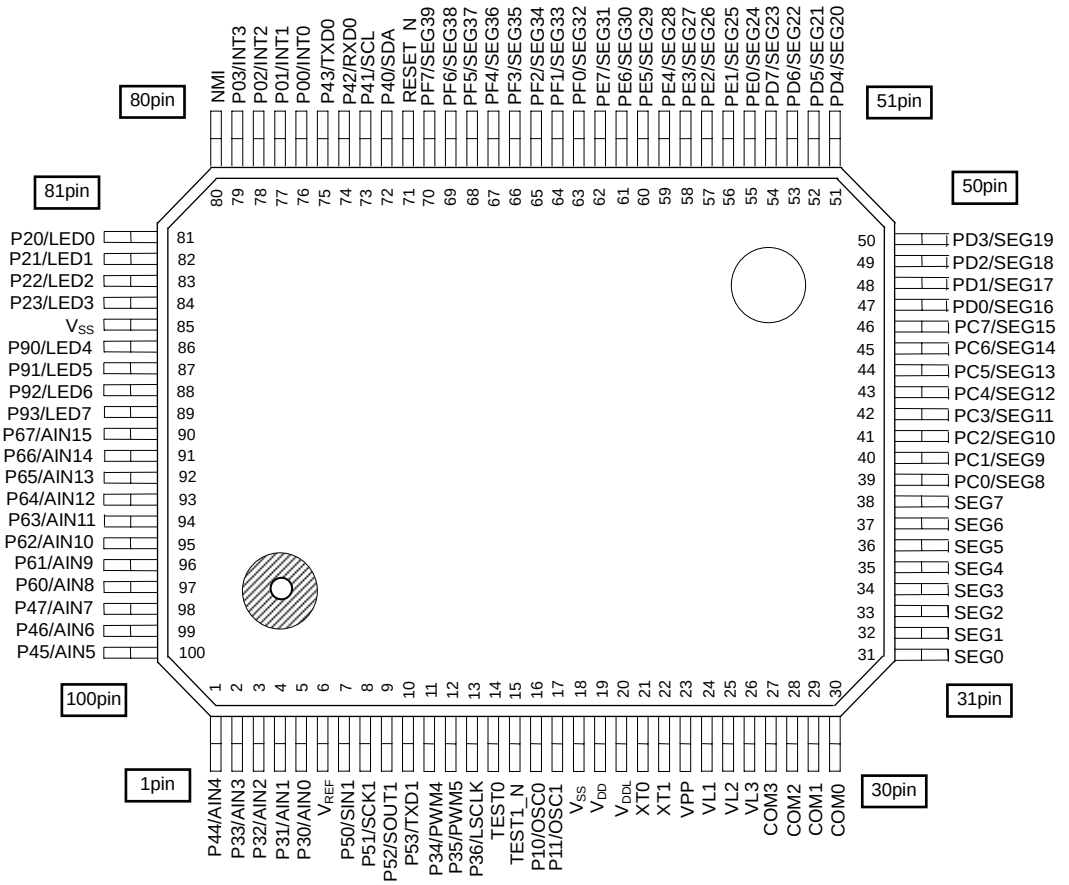


Figure 1-1 Block Diagram of ML610Q178

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML610Q178 QFP Package



(NC) : No Connection

Figure 1-3 Pin Layout of ML610Q178 Package

1.3.2 List of Pins

Table 1-1 lists the pins of the ML610Q178.
In the I/O column, "—" denotes a power supply pin (for primary functions only), "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Table 1-1 (1/4) List of Pins

Pin No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
18,85	Vss	—	Negative power supply pin	—	—	—	—	—	—
19	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
20	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
23	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
24	V_{L1}	—	Power supply pin for LCD bias	—	—	—	—	—	—
25	V_{L2}	—	Power supply pin for LCD bias	—	—	—	—	—	—
26	V_{L3}	—	Power supply pin for LCD bias	—	—	—	—	—	—
14	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—
15	TEST1_N	I	Input pin for testing	—	—	—	—	—	—
71	RESET_N	I	Reset input pin	—	—	—	—	—	—
21	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
22	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
6	V_{REF}	I	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—
80	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—
76	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—
77	P01/EXI1	I	Input port / External interrupt	—	—	—	—	—	—
78	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—
79	P03/EXI3/ RXD1	I	Input port / External interrupt / UART1 data input	—	—	—	—	—	—
16	P10	I	Input port	OSC0	I	High-speed clock oscillation pin	—	—	—
17	P11	I	Input port	OSC1	O	High-speed clock oscillation pin	—	—	—
81	P20/ LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	—	—	—
82	P21/ LED1	O	Output port / LED drive	OUTCLK	O	High-speed clock output	—	—	—
83	P22/ LED2	O	Output port / LED drive	—	—	—	TM9OUT	O	Timer9 output
84	P23/ LED3	O	Output port / LED drive	—	—	—	TMBOUT	O	TimerB output

Pin No.	Primary function			Secondary function			Tertiary function			Fourthry function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
5	P30/ PW45EV 1/AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
4	P31/AIN1	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
3	P32/AIN2	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
2	P33/AIN3	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
11	P34	I/O	Input/output port	—	—	—	PWM4	O	PWM4 output	—	—	—
12	P35	I/O	Input/output port	—	—	—	PWM5	O	PWM5 output	—	—	—
13	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
72	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input	—	—	—
73	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
74	P42	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
75	P43	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UAR1 data output
1	P44/ T0P4CK/ AIN4	I	Input port / Timer0 external clock input / PWM4 external clock input/ Successive approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input	—	—	—
100	P45/ T1P5CK/ AIN5	I	Input port / Timer1 external clock input / PWM5 external clock input/ Successive approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthry function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
99	P46/ T8ACK/ AIN6	I	Input port / Timer8 external clock input / TimerA external clock input / Successive approximation type ADC input	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
98	P47/ T9BCK/ AIN7	I	Input port / Timer9 external clock input / TimerB external clock input / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
7	P50	I/O	Input/output port	—	—	—	SIN1	I	SSIO1 data input	—	—	—
8	P51	I/O	Input/output port	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output	—	—	—
9	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT1	O	SSIO1 data output	—	—	—
10	P53	I/O	Input/output port	TXD1	O	UART1 data input	—	—	—	TXD0	O	UAR0 data output
97	P60/ AIN8	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
96	P61/ AIN9	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
95	P62/ AIN10	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
94	P63/ AIN11	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
93	P64/ AIN12	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthry function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
92	P65/ AIN13	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
91	P66/ AIN14	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
90	P67/ AIN15	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
86	P90/ LED4	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
87	P91/ LED5	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
88	P92/ LED6	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
89	P93/ LED7	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
30	COM0	O	LCD common pin	—	—	—	—	—	—	—	—	—
29	COM1	O	LCD common pin	—	—	—	—	—	—	—	—	—
28	COM2	O	LCD common pin	—	—	—	—	—	—	—	—	—
27	COM3	O	LCD common pin	—	—	—	—	—	—	—	—	—
31	SEG0	O	LCD segment pin	—	—	—	—	—	—	—	—	—
32	SEG1	O	LCD segment pin	—	—	—	—	—	—	—	—	—
33	SEG2	O	LCD segment pin	—	—	—	—	—	—	—	—	—
34	SEG3	O	LCD segment pin	—	—	—	—	—	—	—	—	—
35	SEG4	O	LCD segment pin	—	—	—	—	—	—	—	—	—
36	SEG5	O	LCD segment pin	—	—	—	—	—	—	—	—	—
37	SEG6	O	LCD segment pin	—	—	—	—	—	—	—	—	—
38	SEG7	O	LCD segment pin	—	—	—	—	—	—	—	—	—
39	PC0	I/O	Input/output port	SEG8	O	LCD segment pin	—	—	—	—	—	—
40	PC1	I/O	Input/output port	SEG9	O	LCD segment pin	—	—	—	—	—	—
41	PC2	I/O	Input/output port	SEG10	O	LCD segment pin	—	—	—	—	—	—
42	PC3	I/O	Input/output port	SEG11	O	LCD segment pin	—	—	—	—	—	—
43	PC4	I/O	Input/output port	SEG12	O	LCD segment pin	—	—	—	—	—	—
44	PC5	I/O	Input/output port	SEG13	O	LCD segment pin	—	—	—	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthry function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
45	PC6	I/O	Input/output port	SEG14	O	LCD segment pin	—	—	—	—	—	—
46	PC7	I/O	Input/output port	SEG15	O	LCD segment pin	—	—	—	—	—	—
47	PD0	I/O	Input/output port	SEG16	O	LCD segment pin	—	—	—	—	—	—
48	PD1	I/O	Input/output port	SEG17	O	LCD segment pin	—	—	—	—	—	—
49	PD2	I/O	Input/output port	SEG18	O	LCD segment pin	—	—	—	—	—	—
50	PD3	I/O	Input/output port	SEG19	O	LCD segment pin	—	—	—	—	—	—
51	PD4	I/O	Input/output port	SEG20	O	LCD segment pin	—	—	—	—	—	—
52	PD5	I/O	Input/output port	SEG21	O	LCD segment pin	—	—	—	—	—	—
53	PD6	I/O	Input/output port	SEG22	O	LCD segment pin	—	—	—	—	—	—
54	PD7	I/O	Input/output port	SEG23	O	LCD segment pin	—	—	—	—	—	—
55	PE0	I/O	Input/output port	SEG24	O	LCD segment pin	—	—	—	—	—	—
56	PE1	I/O	Input/output port	SEG25	O	LCD segment pin	—	—	—	—	—	—
57	PE2	I/O	Input/output port	SEG26	O	LCD segment pin	—	—	—	—	—	—
58	PE3	I/O	Input/output port	SEG27	O	LCD segment pin	—	—	—	—	—	—
59	PE4	I/O	Input/output port	SEG28	O	LCD segment pin	—	—	—	—	—	—
60	PE5	I/O	Input/output port	SEG29	O	LCD segment pin	—	—	—	—	—	—
61	PE6	I/O	Input/output port	SEG30	O	LCD segment pin	—	—	—	—	—	—
62	PE7	I/O	Input/output port	SEG31	O	LCD segment pin	—	—	—	—	—	—
63	PF0	I/O	Input/output port	SEG32	O	LCD segment pin	—	—	—	—	—	—
64	PF1	I/O	Input/output port	SEG33	O	LCD segment pin	—	—	—	—	—	—
65	PF2	I/O	Input/output port	SEG34	O	LCD segment pin	—	—	—	—	—	—
66	PF3	I/O	Input/output port	SEG35	O	LCD segment pin	—	—	—	—	—	—
67	PF4	I/O	Input/output port	SEG36	O	LCD segment pin	—	—	—	—	—	—
68	PF5	I/O	Input/output port	SEG37	O	LCD segment pin	—	—	—	—	—	—
69	PF6	I/O	Input/output port	SEG38	O	LCD segment pin	—	—	—	—	—	—
70	PF7	I/O	Input/output port	SEG39	O	LCD segment pin	—	—	—	—	—	—

1.3.3 Pin Description

Table 1-2 shows the pin description.
In the I/O column, "—" denotes an input pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Table 1-2 Pin Description

Pin name	I/O	Description	Primary/ Secondary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C_L) (see Measuring Circuit 1) between this pin and V_{SS} .	—	—
V_{PP}	—	Power supply pin for programming Flash ROM.	—	—
V_{L1}	—	Power supply pins for LCD bias (external input)	—	—
V_{L2}	—	Power supply pins for LCD bias (external input)	—	—
V_{L3}	—	Power supply pins for LCD bias (external input)	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I	Input pin for testing. Has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	—	—
XT1	O		—	—
OSC0	I	External input pin for high-speed clock. This function is allocated to the secondary function of the P10 pin.	Secondary	—
OSC1	O		Secondary	—
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin and P36 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—

Pin name	I/O	Description	Primary/ Secondary	Logic
General-purpose input port				
P00 to P03	I	General-purpose input ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P10 to P11	I			
General-output input port				
P20 to P23	O	General-purpose output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P90 to P93	O	General-purpose output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30 to P36	I/O	General-purpose input/output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P40 to P47				
P50 to P53				
P60 to P67				
PC0 to PC7		General-purpose input/output ports.Provided with a LCD segment for each port. Cannot be used as ports if LCD segment are used.		
PD0 to PD7				
PE0 to PE7				
PF0 to PF7				

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P43 pin and the fourthly function of the P53 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the secondary function of the P42 pin.	Secondary	Positive
TXD1	O	UART1 data output pin. Allocated to the secondary function of the P53 pin and the fourthly function of the P43 pin.	Secondary	Positive
RXD1	I	UART1 data input pin. Allocated to the primary function of the P03 pin and the secondary function of the P52 pin.	Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P44 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and P45 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and P46 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P50 pin .	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P51 pin.	Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P52 pin.	Tertiary	Positive
PWM				
PWM4	O	PWM4 output pin. Allocated to the tertiary function of the P34 and P43 pins.	Tertiary	Positive
PWM5	O	PWM5 output pin. Allocated to the tertiary function of the P35and P47 pins.	Tertiary	Positive
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
PW45EV0 PW45EV1	I	Control start /stop pin for PWM4 and PWM5. Allocated to the primary function of the P00 pin and P30 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0–EXI3	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P03 pins.	Primary	Positive/ Negative

Pin name	I/O	Description	Primary/ Secondary	Logic
Timer				
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
T8ACK	I	External clock input pin for timer 8 and timer A. Allocated to the primary function of the P46 pin.	Primary	—
T9BCK	I	External clock input pin for timer 9 and timer B. Allocated to the primary function of the P47 pin.	Primary	—
TM9OUT	O	Timer9 overflow output pin. Allocated to the secondary function of the P22 pin.	Tertiary	Positive
TMBOUT	O	TimerB overflow output pin. Allocated to the secondary function of the P23 pin.	Tertiary	Positive
LED drive				
LED0-LED7	O	Pins for LED driving. Allocated to the primary function of the P20-P23 and P90-P93 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0–AIN15	I	Analog inputs to Ch0–Ch15 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P33 , P44 to P47 and P60-P67 pins.		
LCD driver				
COM0 to COM3	O	LCD common output pins.	—	—
SEG0 to SEG7	O	LCD segment output pins.	—	—
SEG8 to SEG39	O	LCD segment output pins. Allocated to the secondary function of the PC0 to PC7 and PD0 to PD7 and PE0 to PE7 and PF0 to PF7 pins.	—	—

1.3.4 Termination of Unused Pins

Table 1-3 shows the recommended termination of unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	open
RESET_N	open
TEST0	open
TEST1_N	open
V_{REF}	Connect to V_{DD}
P00 to P03	Connect V_{DD} or V_{SS}
P10 to P11	Connect V_{DD} or V_{SS}
P20 to P23	open
P30 to P33 (AIN0 to AIN3)	open
P34 to P36	open
P40 to P43	open
P44 to P47 (AIN4 to AIN7)	open
P50 to P53	open
P60 to P67 (AIN8 to AIN15)	open
P90 to P93	open
COM0 to COM3	open
SEG0 to SEG7	open
PC0 to PC7（SEG8 to15）	open
PD0 to PD7（SEG16 to 23）	open
PE0 to PE7（SEG24 to 31）	open
PF0 to PF7（SEG32 to 39）	open

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

Chapter 2

CPU and Memory Space

2. CPU and Memory Space

2.1 Overview

This LSI incorporates 8-bit CPU nX-U8/100, and a LARGE model is selected for the memory model.
For details of the CPU nX-U8/100, refer to the "nX-U8/100 Core Instruction Manual".

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The ROM window area contains data having a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of 2 segment and has a total capacity of 128 Kbytes (64 Kwords).
Figure 2-1 shows the configuration of the program memory space.

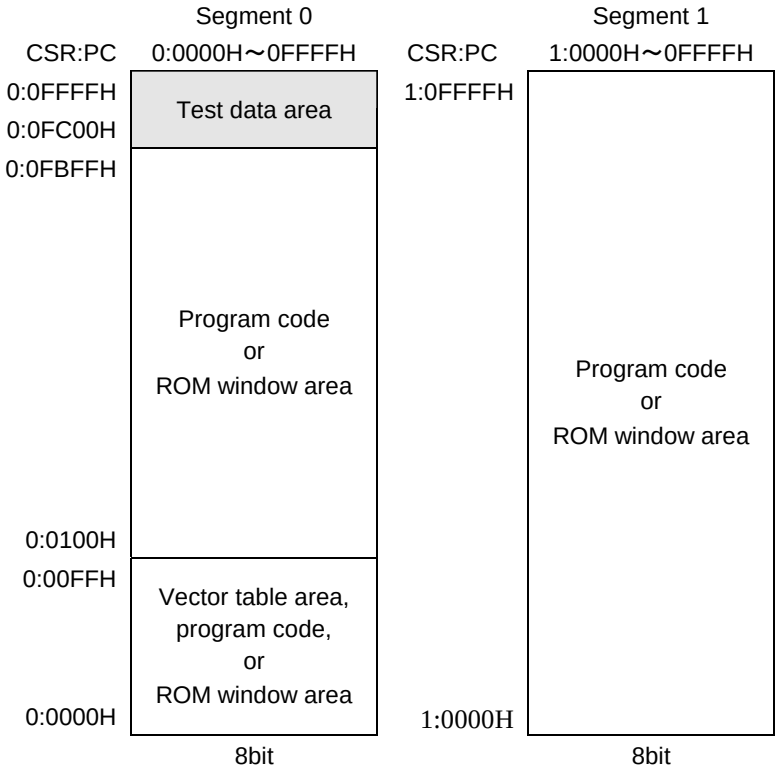


Figure 2-1 Configuration of Program Memory Space

Notes:
- The 1K-byte (512-word) test data area (0:FC00H to 0:FFFFH) of Segment 0 cannot be used as a program code area. Out of the test data area, the area 0:FC00H to 0:FDFFH is writable and erasable and the area 0:FE00H to 0:FFFFH is disabled for both write and read. Always write "0FFH" to the test data area 0:FC00H to 0:FDFFH for write. Operation is not guaranteed if the state where it does not write in or any other value than "0FFH" is written.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space for fail-safe reasons.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 4-Kbyte RAM area, SFR area, and the ROM reference area of Segment 8.
The data memory stores 8-bit data and is specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by instructions.
Figure 2-2 shows the configuration of the data memory space.

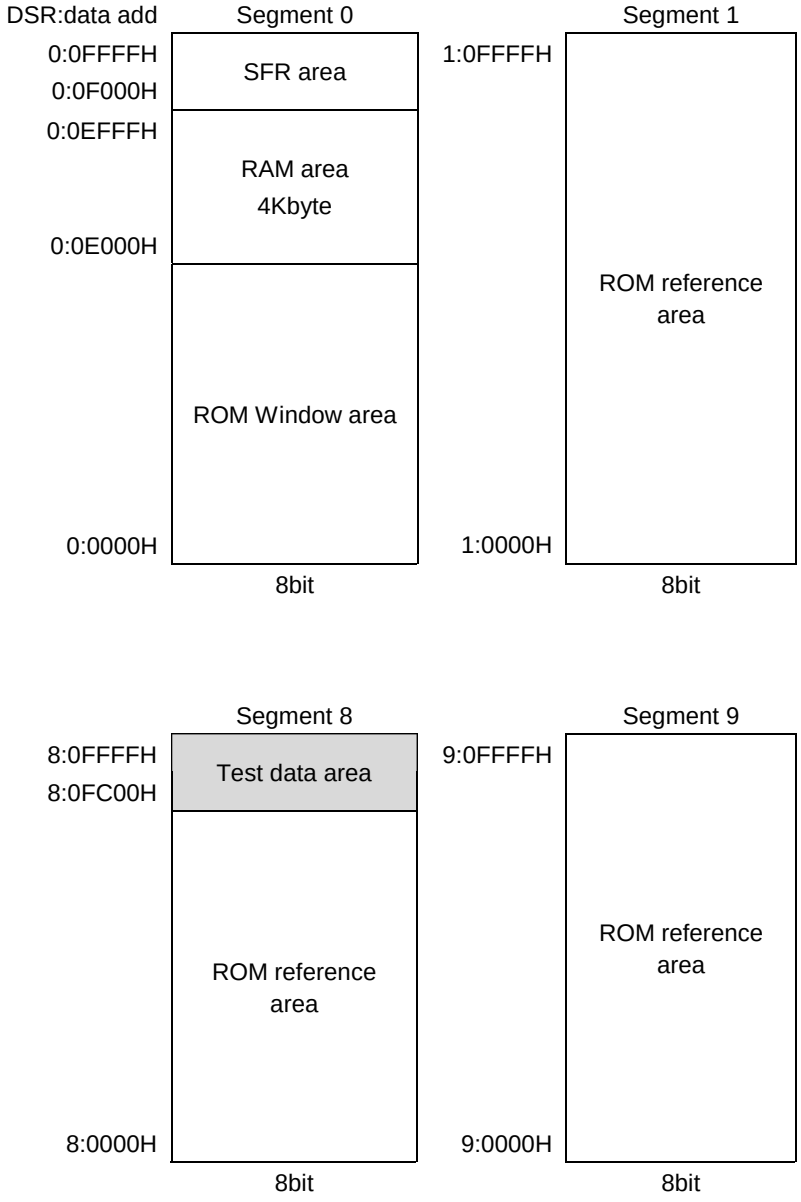


Figure 2-2 Configuration of Data Memory Space

Notes:
- The contents of the 4-Kbyte RAM area are undefined at system reset. Initialize this area by software.
- The contents of the segment 0 of program memory space are read from the ROM reference area of a segment 8.
- The contents of the segment 1 of program memory space are read from the ROM reference area of a segment 9.

2.4 Instruction Length

One instruction has a length of 16 bits.

2.5 Data Type

The two data types of byte (8 bits) and word (16 bits) are supported.

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) used to retain a data segment. For details of DSR, refer to the "nX-U8/100 Core Instruction Manual".

[Description of Bits]

- **DSR3-DSR0** (bits 3-0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Data segment 1
0	0	1	0	Setting prohibited
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Data segment 8
1	0	0	1	Data segment 9
1	0	1	0	Setting prohibited
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Chapter 3

Reset Function

3 Reset Function

3.1 Overview

This LSI has the four reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

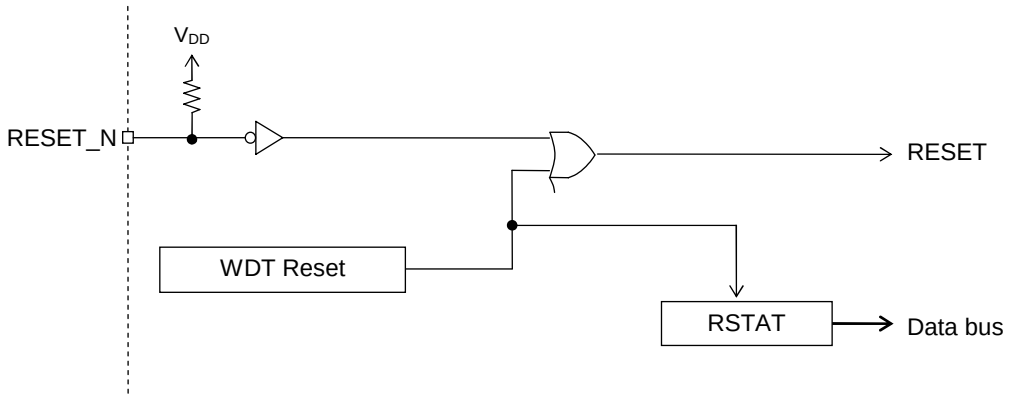
- Reset by the RESET_N pin
- Reset by the 2nd watchdog timer (WDT) overflow
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESER_N pin has an internal pull-up resistor
- 125 ms, 500m sec, 2 sec, or 8 sec can be selected as the watchdog timer (WDT) overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT : Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	—	R/W	8	—

3.2.2 Reset Status Register (RSTAT)

Address: 0F001H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	—	—	—	WDTR	—	—
R/W	R	R	R	R	R	R/W	R	R
Initial value	0	0	0	0	0	0	0	x

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]

- **WDTR** (bit 2)
  The WDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

Note:
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1 Operation of System Reset Mode

System reset has the highest priority among all the processings and any other processing being executed up to then is cancelled. The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by watchdog timer (WDT) overflow
- Software reset by the BRK instruction (only the CPU is reset)

In system reset mode, the following processing is performed.

(1) The power circuit is initialized, but not initialized by the reset by the BRK instruction execution. For the details of the power circuit, refer to Chapter 30, "Power Circuit".
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
   - All the registers in CPU are initialized.
   - The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
   - The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEEVL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 4

MCU Control Function

4. MCU Control Function

4.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

(1) System reset mode
(2) Program run mode
(3) HALT mode
(4) STOP mode

For system reset mode, see Chapter 3, "Reset Function".
This LSI has a block control function which can reduce the supply current more by shut the operation(reset the register and stop the clock) of the unused function.

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which shut the unused operation(reset the register and stop the clock) of the function.

4.1.2 Configuration

Figure 4-1 shows an operating state transition diagram.

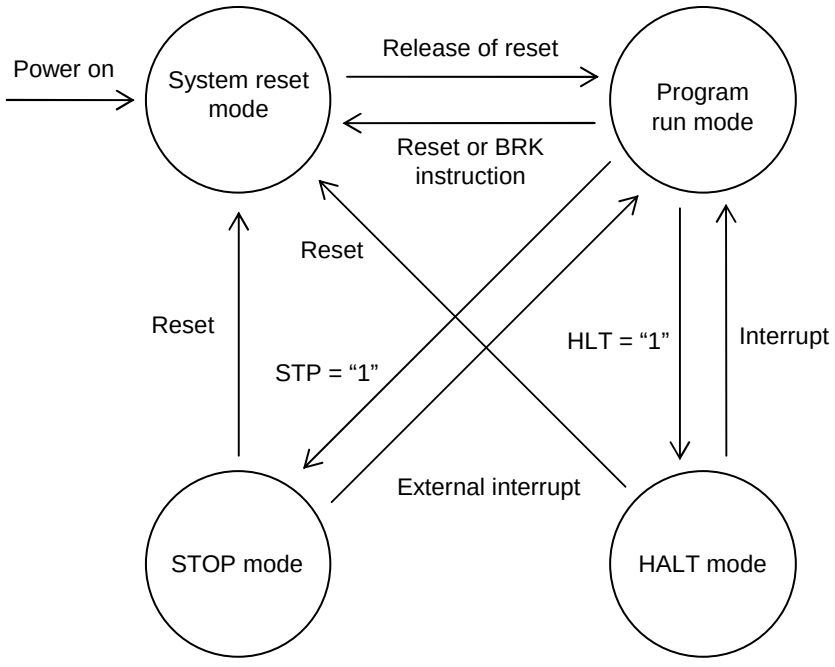


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	—	W	8	—
0F009H	Standby control register	SBYCON	—	W	8	00H
0F028H	Block control register 0	BLKCON0	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	—	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	—	R/W	8	00H

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: – (Undefined)

	7	6	5	4	3	2	1	0
STPACP	—	—	—	—	—	—	—	—
W	W	W	W	W	W	W	W	W
Initial value	—	—	—	—	—	—	—	—

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".
During a system reset, the stop code acceptor is disabled.

Note:
The stop code acceptor is not enabled on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	—	—	—	—	—	—	STP	HLT
W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. When the NMI interrupt request or the P00–P03 interrupt request enabled by the interrupt enable register 1 (IE1) is issued, the STP bit is set to "0" and the LSI returns to the program run mode.

- **HLT** (bit 0)
  The HALT bit is used for setting a HALT mode. When the HALT bit is set to "1", the mode is changed to the HALT mode. When the NMI interrupt request, WDT interrupt request, or enabled (the interrupt enable flag is "1") interrupt request is issued, the HALT bit is set to "0" and the mode is returned to program run mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Prohibited

Note:
The mode can not be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).
When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. Refer to the "nX-U8/100 Core Instruction Manual" for details of PSW.

4.2.4 Block Control Register 0 (BLKCON0)

Address: 0F028H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON0	—	—	—	—	—	—	DTM1	DTM0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON0 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DTM1** (bit 1)
  DTM1 controls the timer 1 operation.

DTM1	Description
0	Enables Timer 1 operation (initial value).
1	Disables Timer 1 operation.

- **DTM0** (bit 0)
  DTM0 controls the timer 0 operation.

DTM0	Description
0	Enables Timer 0 operation (initial value).
1	Disables Timer 0 operation.

Note:
- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 8, "Timers" for details of the timer operation.

4.2.5 Block Control Register 2 (BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C0	—	—	—	DUA1	DUA0	DSIO1	DSIO0
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DI2C0** (bit 7)
  DI2C0 controls the operation of I^2C bus interface.

DI2C0	Description
0	Enables the operation of I^2C bus interface (initial value).
1	Disables the operation of I^2C bus interface.

- **DUA1** (bit 3)
  DUA1 controls the operation of UART1.

DUA1	Description
0	Enables the operation of UART1(initial value).
1	Disables the operation of UART1.

- **DUA0** (bit 2)
  DUA0 controls the operation of UART0.

DUA0	Description
0	Enables the operation of UART0(initial value).
1	Disables the operation of UART0.

- **DSIO1** (bit 1)
  DSIO1 controls the operation of the synchronous serial port 0.

DSIO1	Description
0	Enables the operation of SSIO1 (initial value).
1	Disables the operation of SSIO1.

- **DSIO0** (bit 0)
  DSIO0 controls the operation of the synchronous serial port 0.

DSIO0	Description
0	Enables the operation of SSIO0 (initial value).
1	Disables the operation of SSIO0.

Note:

- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 13, "I^2C bus interface" for details of the I^2C bus interface operation.
- Refer to Chapter 12, "UART" for details of the UART operation.
- Refer to Chapter 11, "Synchronous Serial Port" for details of the SSIO operation.

4.2.6 Block Control Register 4 (BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	—	DLCD	DBLD	—	—	—	—	DSAD
R/W	R	R/W	R/W	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DLCD** (bit 6)
  DLCD controls the operation of the LCD driver.

DLCD	Description
0	Enable the operation of the LCD driver (initial value).
1	Disable the operation of the LCD driver.

- **DBLD** (bit 5)
  The DBLD bit is used to control BLD (Battery Level Detector) operation. When the DBLD bit is set to "1", the circuits related to BLD are reset and turned off.

DBLD	Description
0	Enable the operation of the BLD (initial value).
1	Disable the operation of the BLD.

- **DSAD** (bit 0)
  The DSAD bit is used to control SA type A/D converter operation. When the DSAD bit is set to "1", the circuits related to SA type A/D converter are reset and turned off.

DSAD	Description
0	Enable operating SA type A/D converter (initial value)
1	Disable operating SA type A/D converter

Note:
- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 23, "LCD driver" for details of the LCD driver operation.
- Refer to Chapter 27, "Battery Level Detector" for details of the Battery Level Detector operation.
- Refer to Chapter 24, "Successive Approximation Type A/D Converter" for details of the successive approximation type A/D converter operation.

4.2.7 Block Control Register 6 (BLKCON6)

Address: 0F02EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON6	—	—	—	—	DTMB	DTMA	DTM9	DTM8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON6 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DTMB** (bit 3)
  DTMB controls the operation of the TimerB.

DTMB	Description
0	Enable the operation of the TimerB (initial value).
1	Disable the operation of the TimerB.

- **DTMA** (bit 2)
  DTMA controls the operation of the TimerA.

DTMA	Description
0	Enable the operation of the TimerA (initial value).
1	Disable the operation of the TimerA.

- **DTM9** (bit 1)
  DTM9 controls the operation of the Timer9.

DTM9	Description
0	Enable the operation of the Timer9 (initial value).
1	Disable the operation of the Timer9.

- **DTM8** (bit 0)
  DTMB controls the operation of the Timer 8.

DTM8	Description
0	Enable the operation of the Timer8 (initial value).
1	Disable the operation of the Timer8.

Note:
• If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
• Refer to Chapter 8, "Timer" for details of the Timer operation.

4.2.8 Block Control Register 7 (BLKCON7)

Address: 0F02FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON7	—	—	—	—	—	—	DPW5	DPW4
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON7 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DPW5** (bit 1)
  DPW5 controls the operation of the PWM5.

DPW5	Description
0	Enable the operation of the PWM5 (initial value).
1	Disable the operation of the PWM5.

- **DPW4** (bit 0)
  DPW4 controls the operation of the PWM4.

DPW4	Description
0	Enable the operation of the PWM4 (initial value).
1	Disable the operation of the PWM4.

Note:
- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 10, "PWM" for details of the PWM operation.

4.3 Description of Operation

4.3.1 Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt or NMI interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2 HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a NMI interrupt request, a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE0–IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK) and the HALT mode is returned to the program run mode released.
Figure 4-2 shows the operation waveforms in HALT mode.

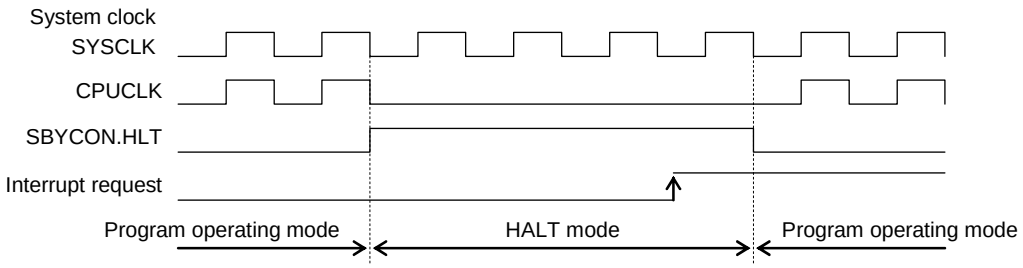


Figure 4-2 Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3 STOP Mode

The STOP mode is the state where low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by writing "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the stop code acceptor is disabled.
When a NMI interrupt request or an interrupt-enabled (the interrupt enable flag is "1") P00 to P03 interrupt request is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 STOP Mode When CPU Operates with Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When the NMI interrupt request or the interrupt-enabled (the interrupt enable flag is "1") P00 to P03 interrupt request is issued, the STP bit is set to "0" and low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before the STOP mode is entered, high-speed oscillation does not start.
When an interrupt request occurs, the STOP mode is released after counting a built-in RC oscillation clock 128 times., the mode is returned to the program mode, and the low-speed clock(LSCLK) restarts supply to the peripheral circuits. If the high-speed clock already started oscillation at this time, the high-speed clocks (OSCLK and HSCLK) also restart supply to the peripheral circuits. After waiting for low-speed crystal oscillation start time(T_{XTL}) and low-speed crystal oscillation stable time(8192-pulse count), the low-speed clock changes from a built-in RC oscillation clock to the low-speed crystal oscillation clock. Simultaneously, low-speed oscillation clock change interruption (LOSCINT) is generated.
Refer to appendix C, "Electrical Characteristics" for T_{XTL}.
Figure 4-3 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.

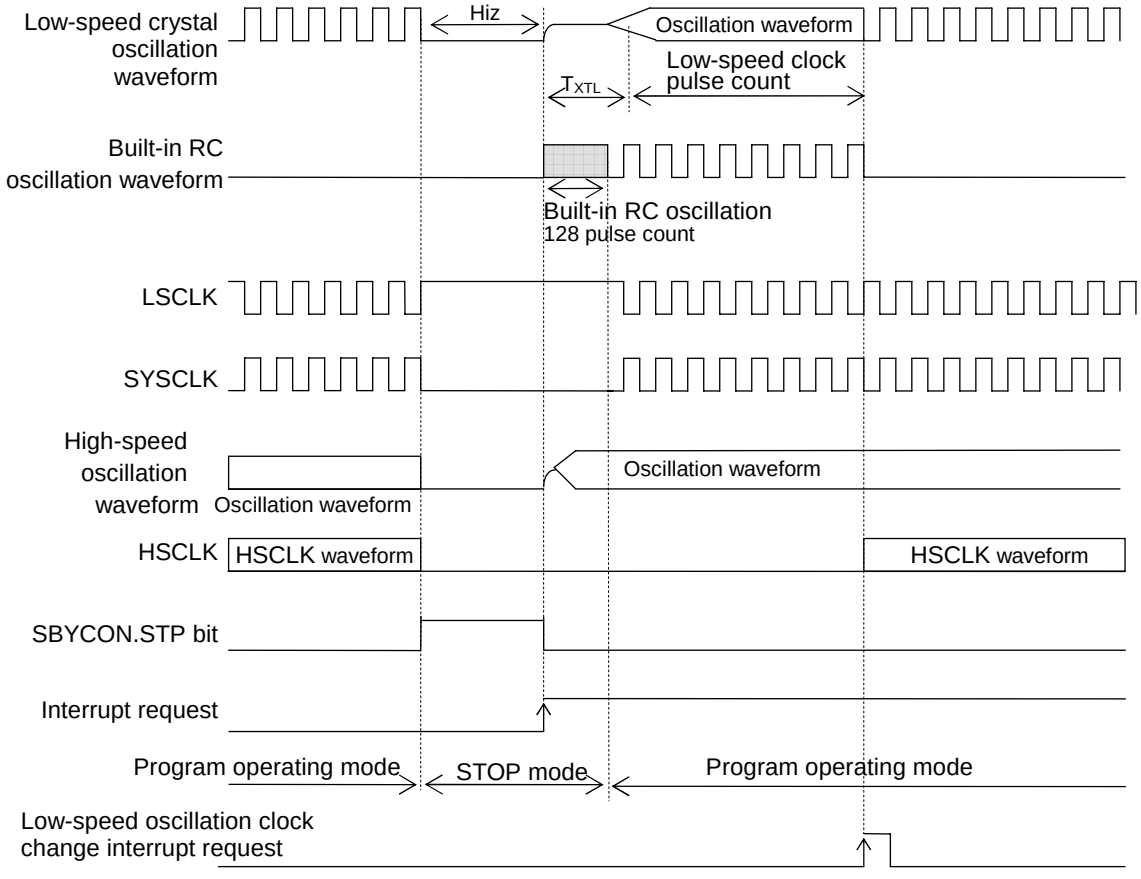


Figure 4-3 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.3.2 STOP Mode When CPU Operates with High-Speed Clock

When the CPU is operating with a high-speed clock and the STP bit of SBYCON is set to "1" with the stop code acceptor enabled, the STOP mode is entered and high-speed oscillation and low-speed oscillation stop.
When the NMI interrupt request or the interrupt-enabled (the interrupt enable flag is "1") P00 to P03 interrupt request is issued, the STP bit is set to "0" and the low-speed and high-speed oscillation restart.
When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (T_{XTH}) and the high-speed clock (OSCLK) oscillation stabilization time (4096-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
The low-speed clock (LSCLK) restarts supply to the peripheral circuits after counting a built-in RC oscillation clock 128 times. After the elapse of the low-speed oscillation start time (T_{XTL}) and the oscillation stabilization time (8192-pulse count), the clock is returned to the built-in RC oscillation clock to a low-speed crystal oscillation clock. Simultaneously, low-speed oscillation clock change interruption (LOSCINT) is generated.
Figure 4-4 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.

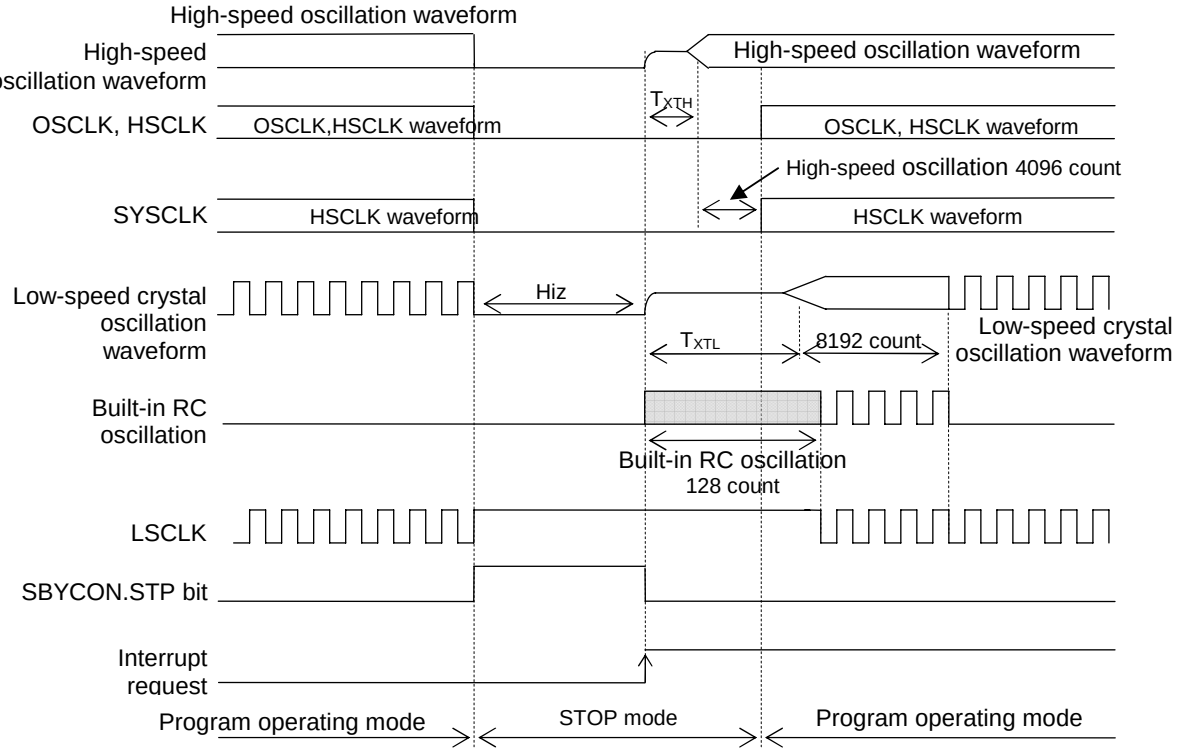


Figure 4-4 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
The STOP mode is entered after the instruction that sets the STP bit to "1" and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to "1".

4.3.3.3 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE3), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from STOP/HALT mode.

Table 4-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
∗	∗	—	0	Not returned from STOP/HALT mode.
3	∗	—	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0, 1, 2	∗	—	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
∗	∗	∗	0	Not returned from STOP/HALT mode.
∗	∗	0	1	
∗	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2, 3	1	1	1	
0,1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Notes:
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither nonmaskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.4 Block control function

To use this block control function, supply current can be reduced more, by stopping completely operation of the unused function.
The initial value of each bit of each block control register is "0", and operation of each block is enabled. If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".

BLKCON0,6 register controls (enables or disables) the operation of Timer .
BLKCON2 register controls (enables or disables) the operation of I^2C UART and SSIO.
BLKCON4 register controls (enables or disables) the operation of the LCD driver, Battery level detecter successive-approximation type A/D converter.
BLKCON7 register controls (enables or disables) the operation of PWM.

Notes:
- If the appropriate bit of the block register is set to "1", all relevant registers are initialized.
- Refer to the relevant chapter for details of operation or notes of each block.

Chapter 5

Interrupts (INTs)

5. Interrupts (INTs)

5.1 Overview

This LSI has 25 interrupt sources (External interrupts: 5 sources, Internal interrupts: 20 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 6, "Clock Generation Circuit"
Chapter 7, "Time Base Counter"
Chapter 8, "Timer"
Chapter 9, "Watchdog Timer"
Chapter 10, "PWM"
Chapter 11, "Synchronous Serial Port"
Chapter 12, "UART"
Chapter 13, "I^2C bus interface"
Chapter 14, "NMI"
Chapter 15, "Port0"
Chapter 23, "Successive Approximation Type A/D Converter"

5.1.1 Features

- 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
- 23 maskable interrupt sources (Internal sources: 19, External sources: 4)
- Software interrupt (SWI): 64 sources max.
- External interrupts allow edge selection and sampling selection.

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H

5.2.2 Interrupt Enable Register 0 (IE0)

Address: 0F010H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE0	—	ELOSC	—	—	—	—	—	—
R/W	R	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE0 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **ELOSC** (bit 6)
  ELOSC is the enable flag for the Low-speed clock change interrupt (LOSCINT).

ELOSC	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	—	—	—	—	EP03	EP02	EP01	EP00
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **EP00** (bit 0)
  EP00 is the enable flag for the input port P00 pin interrupt (P00INT).

EP00	Description
0	Disabled (initial value)
1	Enabled

- **EP01** (bit 1)
  EP01 is the enable flag for the input port P01 pin interrupt (P01INT).

EP01	Description
0	Disabled (initial value)
1	Enabled

- **EP02** (bit 2)
  EP02 is the enable flag for the input port P02 pin interrupt (P02INT).

EP02	Description
0	Disabled (initial value)
1	Enabled

- **EP03** (bit 3)
  EP03 is the enable flag for the input port P03 pin interrupt (P03INT).

EP03	Description
0	Disabled (initial value)
1	Enabled

5.2.4 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	EI2C0	—	—	—	—	ESAD	ESIO1	ESIO0
R/W	R/W	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]

- **ESIO0** (bit 0)
  ESIO0 is the enable flag for the synchronous serial port 0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

- **ESIO1** (bit 1)
  ESIO1 is the enable flag for the synchronous serial port 1 interrupt (SIO1INT).

ESIO1	Description
0	Disabled (initial value)
1	Enabled

- **ESAD** (bit 2)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

- **EI2C0** (bit 7)
  EI2C0 is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

EI2C0	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	—	—	—	—	ETM9	ETM8	ETM1	ETM0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

[Description of Bits]

- **ETM0** (bit 0)
  ETM0 is the enable flag for the timer 0 interrupt (TM0INT).

ETM0	Description
0	Disabled (initial value)
1	Enabled

- **ETM1** (bit 1)
  ETM1 is the enable flag for the timer 1 interrupt (TM1INT).

ETM1	Description
0	Disabled (initial value)
1	Enabled

- **ETM8** (bit 2)
  ETM8 is the enable flag for the timer 8 interrupt (TM8INT).

ETM4	Description
0	Disabled (initial value)
1	Enabled

- **ETM9** (bit 3)
  ETM9 is the enable flag for the timer 9 interrupt (TM9INT).

ETM5	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	—	—	—	—	—	—	EUA1	EUA0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **EUA1** (bit 1)
  EUA1 is the enable flag for the UART1 interrupt (UA1INT).

EUA1	Description
0	Disabled (initial value)
1	Enabled

5.2.7 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	ETMB	ETMA	—	—	—	—	—	—
R/W	R/W	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

- **ETMA** (bit 6)
  ETMA is the enable flag for the timer A interrupt (TMAINT).

ETMA	Description
0	Disabled (initial value)
1	Enabled

- **ETMB** (bit 7)
  ETMB is the enable flag for the timer B interrupt (TMBINT).

ETMB	Description
0	Disabled (initial value)
1	Enabled

5.2.8 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	EL32H	—	EL128H	—	—	—	EPW5	EPW4
R/W	R/W	R	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

- **EPW4** (bit 0)
  EPW4 is the enable flag for the PWM4 interrupt (PW4INT).

EPW4	Description
0	Disabled (initial value)
1	Enabled

- **EPW5** (bit 0)
  EPW5 is the enable flag for the PWM5 interrupt (PW5INT).

EPW5	Description
0	Disabled (initial value)
1	Enabled

- **EL128H** (bit 5)
  EL128H is the enable flag for the time base counter 128 Hz interrupt (TL128HINT).

EL16H	Description
0	Disabled (initial value)
1	Enabled

- **EL32H** (bit 7)
  EL32H is the enable flag for the time base counter 32Hz interrupt (TL32HINT).

EL32H	Description
0	Disabled (initial value)
1	Enabled

5.2.9 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	—	—	—	—	E2H	—	—	E16H
R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]

- **E16H** (bit 0)
  E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

- **E2H** (bit 3)
  E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

5.2.10 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	—	QLOSC	—	—	—	—	QNMI	QWDT
R/W	R	R/W	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT) are non-maskable interrupts that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

- **QNMI** (bit 1)
  QNMI is the request flag for the NMI interrupt (NMINT).

QNMI	Description
0	No request (initial value)
1	Request

- **QLOSC** (bit 6)
  QLOSC is the request flag for the Low-speed clock change interrupt (LOSCINT).

QLOSC	Description
0	No request (initial value)
1	Request

Note:
• When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	—	—	—	—	QP03	QP02	QP01	QP00
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QP00** (bit 0)
  QP00 is the request flag for the input port P00pin interrupt (P00INT).

QP00	Description
0	No request (initial value)
1	Request

- **QP01** (bit 1)
  QP01 is the request flag for the input port P01 pin interrupt (P01INT).

QP01	Description
0	No request (initial value)
1	Request

- **QP02** (bit 2)
  QP02 is the request flag for the input port P02 pin interrupt (P02INT).

QP02	Description
0	No request (initial value)
1	Request

- **QP03** (bit 3)
  QP03 is the request flag for the input port P03 pin interrupt (P03INT).

QP03	Description
0	No request (initial value)
1	Request

Note:
• When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.12 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	QI2C0	—	—	—	—	QSAD	QSIO1	QSIO0
R/W	R/W	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QSIO0** (bit 0)
  QSIO0 is the request flag for the synchronous serial port 0 interrupt (SIO0INT).

QSIO0	Description
0	No request (initial value)
1	Request

- **QSIO1** (bit 1)
  QSIO1 is the request flag for the synchronous serial port 1 interrupt (SIO1INT).

QSIO1	Description
0	No request (initial value)
1	Request

- **QSAD** (bit 2)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT)

QSAD	Description
0	No request (initial value)
1	Request

- **QI2C0** (bit 7)
  QI2C0 is the request flag for the successive approximation type A/D converter interrupt (I2C0INT)

QI2C0	Description
0	No request (initial value)
1	Request

Note:
• When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	—	—	—	—	QTM9	QTM8	QTM1	QTM0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTM0** (bit 0)
  QTM0 is the request flag for the timer 0 interrupt (TM0INT).

QTM0	Description
0	No request (initial value)
1	Request

- **QTM1** (bit 1)
  QTM1 is the request flag for the timer 1 interrupt (TM1INT).

QTM1	Description
0	No request (initial value)
1	Request

- **QTM8** (bit 2)
  QTM8 is the request flag for the timer 8 interrupt (TM8INT).

QTM8	Description
0	No request (initial value)
1	Request

- **QTM9** (bit 3)
  QTM9 is the request flag for the timer 9 interrupt (TM9INT).

QTM9	Description
0	No request (initial value)
1	Request

Note:
- When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	—	—	—	—	—	—	QUA1	QUA0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QUA1** (bit 1)
  QUA1 is the request flag for the UART1 interrupt (UA1INT).

QUA1	Description
0	No request (initial value)
1	Request

Note:
- When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.15 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	QTMB	QTMA	—	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTMA** (bit 6)
  QTMA is the request flag for the timer A interrupt (TMAINT).

QTMA	Description
0	No request (initial value)
1	Request

- **QTMB** (bit 7)
  QTMB is the request flag for the timer B interrupt (TMBINT).

QTMB	Description
0	No request (initial value)
1	Request

Note:
- When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.16 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	—	Q128H	—	—	—	QPW5	QPW4
R/W	R/W	R	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPW4** (bit 0)
  QPW4 is the request flag for the PWM4 interrupt (PW4INT).

QPW4	Description
0	No request (initial value)
1	Request

- **QPW5** (bit 1)
  QPW5 is the request flag for the PWM5 interrupt (PW5INT).

QPW5	Description
0	No request (initial value)
1	Request

- **Q128H** (bit 5)
  Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

- **Q32H** (bit 7)
  Q32H is the request flag for the time base counter 32Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Note:
- When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.17 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	—	—	—	—	Q2H	—	—	Q16H
R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **Q16H** (bit 0)
  Q16H is the request flag for the time base counter 16 Hz interrupt (T16HINT).

Q16H	Description
0	No request (initial value)
1	Request

- **Q2H** (bit 3)
  Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Note:
- When an interrupt is generated by the instruction to write to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the the interrupt shift cycle starts after the next 1 instruction is executed.

5.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT), interrupt enable/disable for 23 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1 to 7). WDTINT and NMIINT are non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-1 Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
2	NMI interrupt	NMINT	000AH
3	Low-speed clock change interrupt	LOSCINT	000CH
5	P00 interrupt	P00INT	0010H
6	P01 interrupt	P01INT	0012H
7	P02 interrupt	P02INT	0014H
8	P03 interrupt	P03INT	0016H
13	Synchronous serial port 0 interrupt	SIO0INT	0020H
14	Synchronous serial port 1 interrupt	SIO1INT	0022H
15	Successive approximation type A/D converter interrupt	SADINT	0024H
20	I^2C bus interface interrupt	I2C0INT	002EH
21	Timer 0 interrupt	TM0INT	0030H
22	Timer 1 interrupt	TM1INT	0032H
23	Timer 8 interrupt	TM8INT	0034H
24	Timer 9 interrupt	TM9INT	0036H
29	UART 0 interrupt	UA0INT	0040H
30	UART 1 interrupt	UA1INT	0042H
43	Timer A interrupt	TMAINT	005CH
44	Timer B interrupt	TMBINT	005EH
45	PWM 4 interrupt	PW4INT	0060H
46	PWM 5 interrupt	PW5INT	0062H
50	TBC128Hz interrupt	T128HINT	006AH
52	TBC32Hz interrupt	T32HINT	006EH
53	TBC16Hz interrupt	T16HINT	0070H
56	TBC2Hz interrupt	T2HINT	0076H

Note:
When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
Also define the unused interrupt vector for the measure against fail-safe.

5.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW toEPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to"1".
(6) Load the interrupt start address into PC.

5.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2.
(2) Transfer CSR to ECSR2.
(3) Transfer PSW to EPSW2.
(4) Set the ELEVEL field to "2".
(5) Load the interrupt start address into PC.

5.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW to EPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to "1".
(6) Load the interrupt start address into PC.

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

State A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW

Example of description: State A-1-1

```
Intrpt_A-1-1;          ; A-1-1 state
  DI                   ; Disable interrupt
  :
  :
  :
  RTI                  ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: State A-1-2

```
Intrpt_A-1-2;          ; Start
PUSH ELR, EPSW         ; Save ELR and EPSW at the
                         beginning
  EI                   ; Enable interrupt
  :
  :
  :
  :
  :
  POP PC, PSW          ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: A-2-2

```
Intrpt_A-2-2;           ; Start
  PUSH ELR, EPSW,       ; Save ELR, EPSW, LR at
  LR                      the beginning

  EI                    ; Enable interrupt
   :
   :
   :

  BL Sub_1              ; Call subroutine Sub_1
   :

  POP PC, PSW, LR       ; Return PC from the stack
                        ; Return PSW from the stack
                        ; Return LR from the stack
                        ; End
```

```
Sub_1;                  ;
DI                      ; Disable interrupt
                           :
                           :
                           :
RT                      ; Return PC from
                          LR
                        ; End of subroutine
```

State B: Non-maskable interrupt is being processed

B-1: When the interrupt processing is not executed in the interrupt routine.

- Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to PC and those of the EPSW register to PSW.

B-2: When the interrupt processing is executed in the interrupt routine.

B-2-1: When a subroutine is not called by a program when the interrupt routine is executed.

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH ELR, EPSW" instruction to save the interrupt return address and the state of EPSW to the stack.
- Processing at the end of interrupt routine execution.
  Specify "POP PC, PSW" instead of the RTI instruction to return the saved data of the interrupt return address to PC, and the saved data of EPSW to PSW.

B-2-2: When a subroutine is called by a program when the interrupt routine is executed.

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR, ELR, EPSW" instruction to save the interrupt return address, the subroutine return address and the state of EPSW to the stack.
- Processing at the end of interrupt routine execution.
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: B-1

```
Intrpt_B-1;          ; State of B1
   RTI               ; Return PC from ELR
                     ; Return PSW from EPSW
                     ; End
```

Example of description: B-2-1

```
Intrpt_B-2-1:        ; Start
  PUSH  ELR, EPSW    ; Save ELR, EPSW
                       at the beginning
   :
   :
   :
  POP PC, PSW        ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2;        ; Start
   PUSH              ; Save ELR, EPSW, LR at
ELR, EPSW, LR        the beginning
    :
    :
    :
    BL Sub_1         ; Call subroutine Sub_1
:
   POP
   PC, PSW, LR       ; Return PC from the stack
                     ; Return PSW from the stack
                     ; Return LR from the stack
   RTI               ; End
```

```
Sub_1;
                        :
                        :
                        :
RT                  ; Return PC from LR
                    ; End of subroutine
```

5.3.5 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

Reference:
For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Chapter 6

Clock Generation Circuit

6. Clock Generation Circuit

6.1 Overview

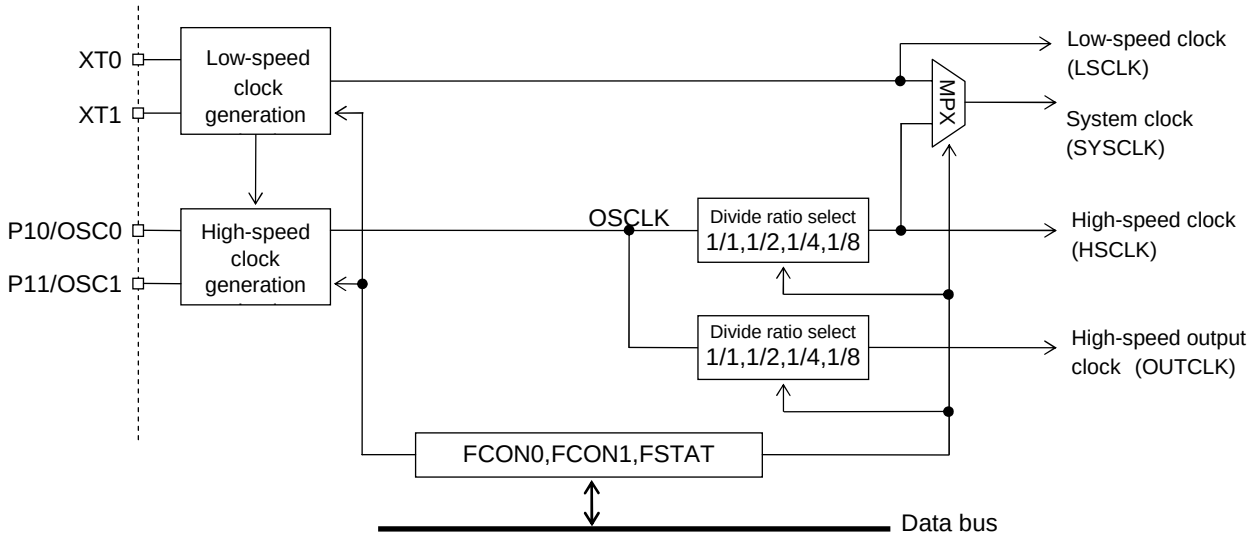
The clock generation circuit generates and supplies a low-speed clock (LSCLK), high-speed clock (HSCLK), system clock (SYSCLK), and high-speed output clock (OUTCLK). LSCLK and HSCLK operate as the time-base clocks for peripheral circuits, SYSCLK as the basic operating clock of the CPU, and OUTCLK as the clock to be output from ports.
For the output ports used for OUTCLK, see Chapter 17, "Port 2".
For the STOP mode mentioned in this chapter, see Chapter 4, "MCU Control Function".

6.1.1 Features

- Low-speed clock generation circuit:
  – 32.768 kHz crystal oscillation mode
  – Built-in RC oscillation (32.7kHz) mode
- High-speed clock generation circuit
  – Built-in PLL oscillation mode
  – Crystal / ceramic oscillation mode
  – External clock input mode

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1
FSTAT : Frequency status register 1

Figure 6-1 Configuration of Clock Generation Circuit

Note:
After power-on or a system reset, OSCLK starts operating with the clock generated by dividing the built-in PLL oscillation by 8. And HSCLK starts operating with the clock generated by dividing the OSCLK by 8 At initialization by software, set the FCON0 or FCON1 register so as to switch the clock to the required one.

6.1.3 List of Pins

Pin name	Input/Output	Description
XT0	I	Pin for connecting a crystal for low-speed clock
XT1	O	Pin for connecting a crystal for low-speed clock
P10/OSC0	I	The crystal or the ceramic oscillator connecting pin for high-speed clocks Used for the secondary function of the P10 pin.
P11/OSC1	O	The crystal or the ceramic oscillator connecting pin for high-speed clocks Used for the secondary function of the P11 pin.

6.1.4 Clock Configuration

Figure 6-2 shows the clock condiguration.

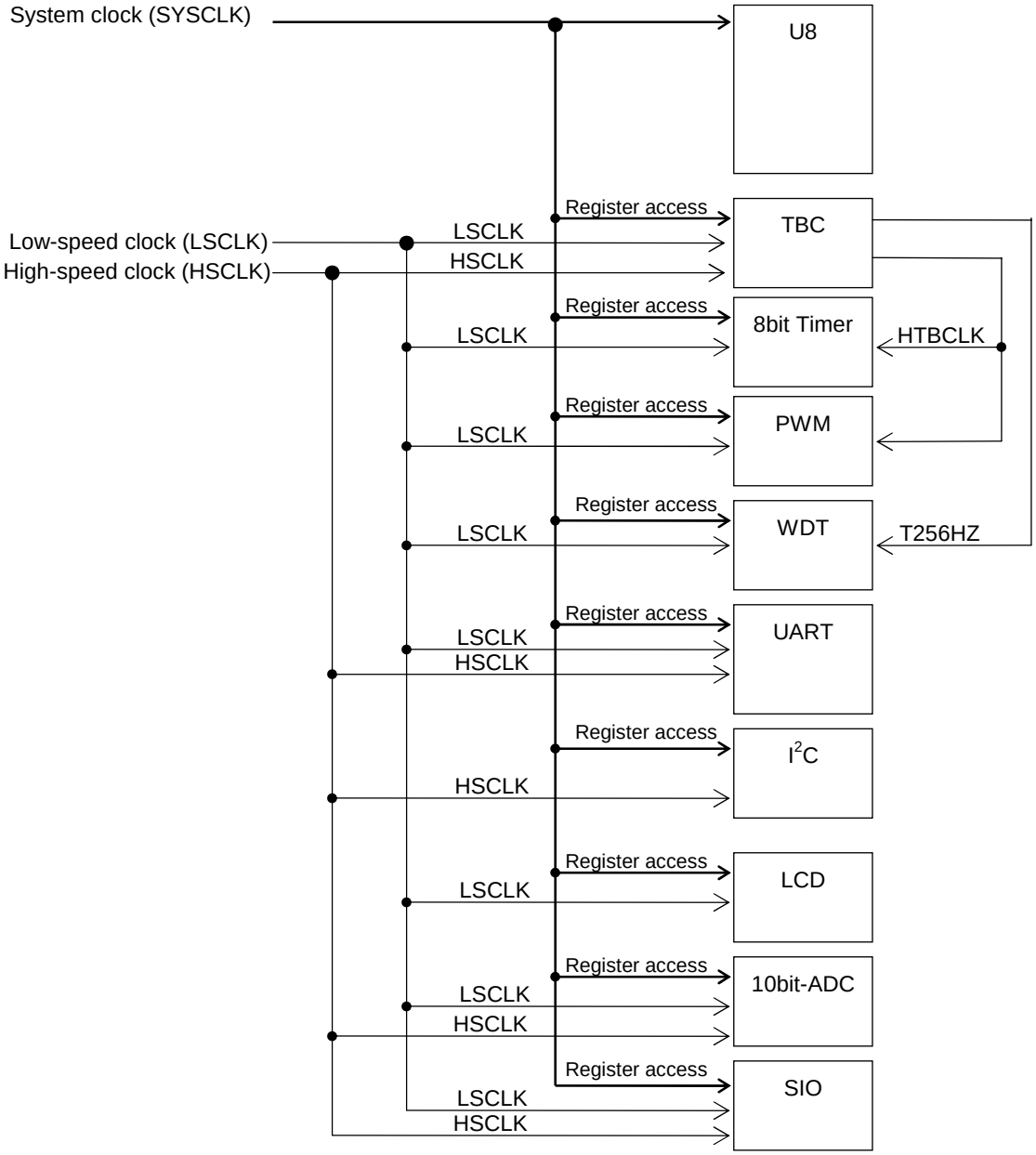


Figure 6-2 Clock Configuration

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	83H
0F070H	Frequency status register	FSTAT	—	R/W	8	00H

6.2.2 Frequency Control Register 0(FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bits
Initial value: 3BH

	7	6	5	4	3	2	1	0
FCON0	—	—	OUTC1	OUTC0	OSCM1	OSCM0	SYSC1	SYSC0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	1	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSC1, SYSC0** (bits 1, 0)
  The SYSC1 and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuit (the high-speed time base counter is included). OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected. The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 8.4 MHz. At system reset, 1/8OSCLK is selected.

SYSC1	SYSC0	Description
0	0	OSCLK（1/2OSCLK in built-in PLL oscillation mode）
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (Initial value)

- **OSCM1, OSCM0** (bits 3, 2)
  The OSCM1 and OSCM0 bits are used to select the mode of the high-speed clock generation circuit. Crystal / ceramic oscillation mode, PLL oscillation mode, or external clock input mode can be selected.
  The setting of OSCM1 and OSCM0 can be changed only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0"). At system reset, PLL oscillation mode is selected.

– When switching the high-speed oscillation mode, please first switch back to low speed clock before switching to other high-speed clock (set the ENOSC bit and SYSCLK bit of FCON1 to "0").

OSCM1	OSCM0	Description
0	0	Prohibited
0	1	Crystal / ceramic oscillation mode
1	0	Built-in PLL oscillation mode(initial value)
1	1	External clock input mode

- **OUTC1, 0** (bits 5, 4)
  The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the secondary function of the port is used. OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (Initial value)

Note:

- To switch the mode of the high-speed clock generation circuit using the OSCM1 and OSCM0 bits, stop the high-speed oscillation and set the system clock to the low-speed clock (set the ENOSC bit and SYSCLK of FCON1 to "0").
- Connect to P10/OSC0, P11/OSC1 pin the oscillator which does not exceed 8.4MHz. And in P10/OSC pin external clock mode, input a clock that does not exceed 8.4 MHz. And
- the frequency of the high-speed output clock does not exceed 8.4 MHz.

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8 bits
Initial value: 83H

	7	6	5	4	3	2	1	0
FCON1	LPLL	—	—	—	—	—	ENOSC	SYSCLK
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	1	0	0	0	0	0	1	1

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSCLK** (bit 0)
  The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 1, 2, 4, 8) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

- **ENOSC** (bit 1)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator.

ENOSC	Description
0	Disables high-speed oscillation
1	Enables high-speed oscillation (initial value)

- **LPLL** (bit 7)
  The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
  When the LPLL bit is set to "1", this indicates that having started supply of OSCLK. When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillating clock is under count..
  LPLL is a read-only bit.

LPLL	Description
0	Disables the use of PLL oscillation
1	Enables the use of PLL oscillation (initial value)

6.2.4 Frequency Status Register (FSTAT)

Address: 0F070H
Access: R/W
Access size: 8 bits
Initial value: 04H

	7	6	5	4	3	2	1	0
FCON1	—	—	—	—	—	LOSCS	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	0	0

FSTAT is a special function register (SFR) to show the status of each oscillation.

[Description of Bits]

- **LOSCS** (bit 2)
  LOSCS shows the oscillation state of a low-speed crystal oscillation circuit. Generating of low-speed oscillation interruption will change LOSCS. LOSCS is set to "1" when going into stop mode, but low-speed oscillation interruption is not generated.

LOSCS	Description
0	The low-speed crystal oscillation circuit counts a low-speed crystal oscillation clock 8192 times, and supplies it to a low-speed clock.
1	The low-speed crystal oscillation circuit is the state which the oscillation stops or the tate where oscillation stable time is counted. (initial value) or the state where it is operating in the built-in RC oscillating circuit

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Clock Generation Circuit (32.768 crystal oscillation circuit)

Figure 6-3 shows the configuration of the low-speed clock generation circuit.
A low-speed clock generation circuit is provided with an external 32.768 kHz crystal. To match the oscillation frequency by using a trimmer capacitor, connect external capacitors (C_{GL} and C_{DL}) as required.

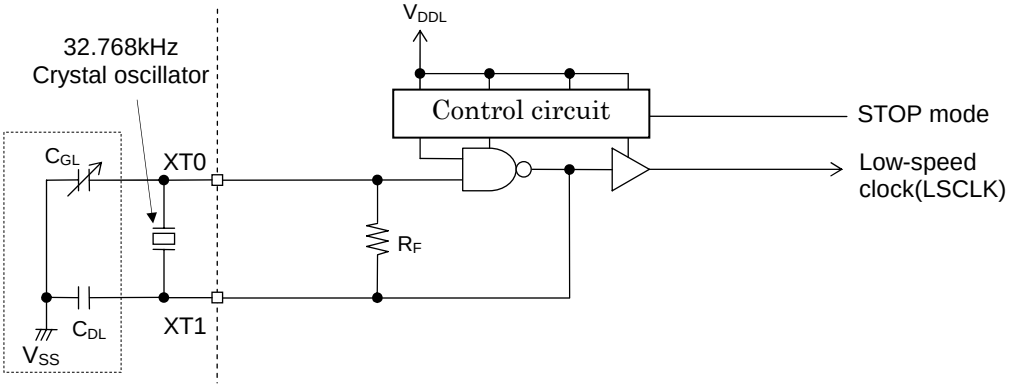


Figure 6-3 Circuit Configuration of 32.768 kHz Crystal Oscillation Mode

Notes:
- Install a crystal as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.
- Note that oscillation may stop due to condensation.

6.3.1.2 Low-speed clock generation circuit (built-in RC oscillating circuit)

Figure 6-4 shows The circuit configuration of a low-speed clock generation circui
After counting RC oscillation clock 128 times, supply of a low-speed oscillation clock is started.

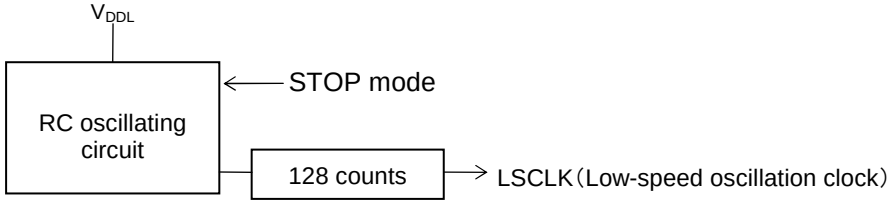


Figure 6-4 Circuit Configuration of 32kHz RC oscillation mode

6.3.1.3 Operation of the Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power ON reset.
After counting a built-in RC oscillation clock 128 times, a built-in RC oscillation clock is supplied to a circumference circuit as a low-speed clock after powered on. After waiting low-speed crystal oscillation starting time(T_{XTL}) and low-speed crystal oscillation stable time(8192 counts), the low-speed clock changes from a built-in RC oscillation clock to a low-speed crystal oscillation clock. Moreover, low-speed oscillation clock change interruption(LOSCINT) is generated simultaneously.
The low-speed clock generation circuit stops the oscillation in STOP mode. When oscillation is resumed by releasing of the STOP mode by external interrupt, after counting a built-in RC oscillation clock 128 times, a built-in RC oscillation clock is supplied to a circumference circuit as a low-speed clock after powered on. After waiting low-speed crystal oscillation starting time(T_{XTL}) and low-speed crystal oscillation stable time(8192 counts), the low-speed clock changes from a built-in RC oscillation clock to a low-speed crystal oscillation clock. Moreover, low-speed oscillation clock change interruption(LOSCINT) is generated simultaneously. For STOP mode, see Chapter 4, "MCU Control Function".
Figure 6-5 shows the waveforms of the low-speed clock generation circuit. For the low-speed oscillation start time (T_{XTL}), see Appendix C, "Electrical Characteristics".

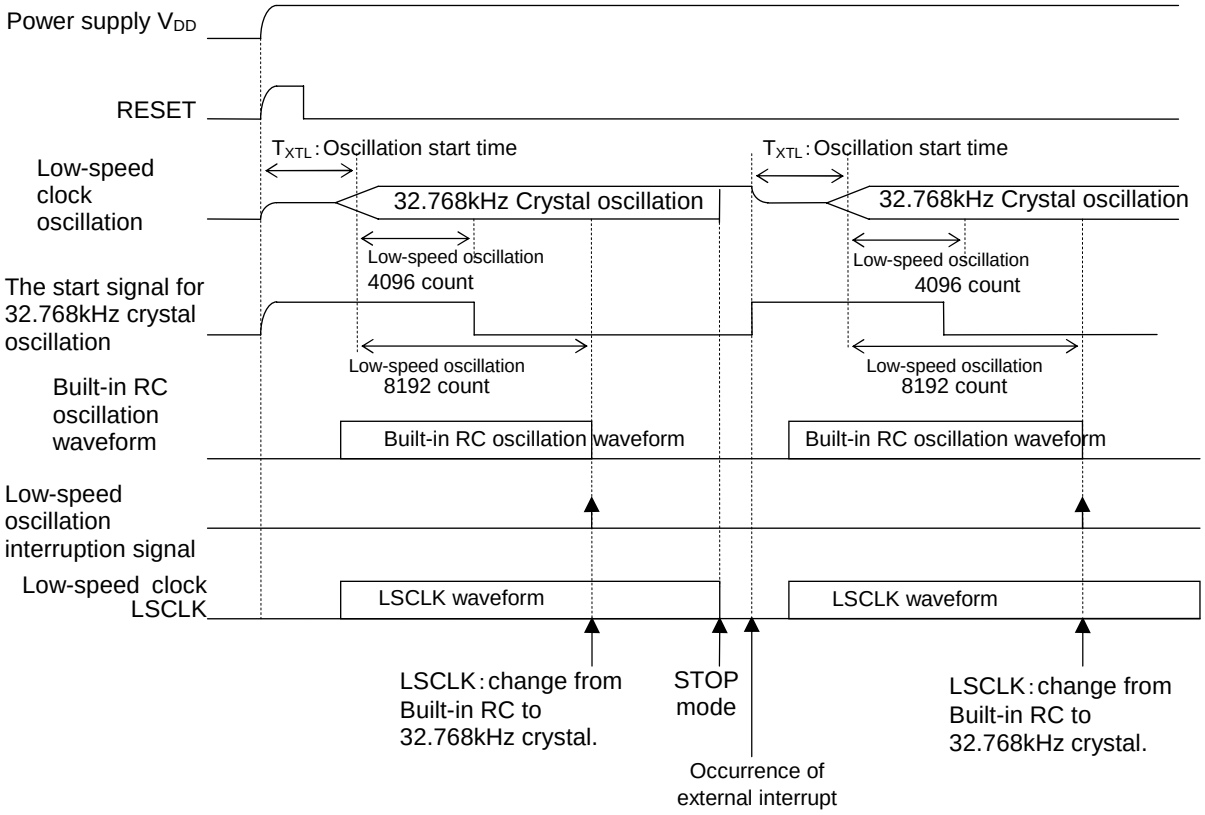


Figure 6-5 Operation of the Low-Speed Clock Generation Circuit

Note:

After powering on, CPU starts with a high-speed clock. It is desirable to set an operation clock as a low speed clock, after checking that the low speed clock is oscillating by setting Interrupt request bit of the 128Hz low-speed time base counter (Q128H) as 1. When an system clock is changed to a low speed clock before the low speed clock oscillated, the CPU does not operate until the oscillation of a low speed clock starts.

6.3.2 High-Speed Clock

The high-speed clock generation circuit can choose built-in PLL (Phase Locked Loop) oscillation mode, crystal / ceramic oscillation mode, and a high-speed external clock input mode.

6.3.2.1 Built-in PLL Oscillation Mode

The PLL oscillation circuit generates a clock of 16 MHz (= Low-speed clock × 500).
In built-in PLL oscillation mode (OSCM0 = "0", OSCM1 = "1"), supply of OSCLK (high-speed oscillation clock) is started when PLL oscillation clock pulse count reaches 8192 after oscillation is enabled (ENOSC is set to "1").
In PLL oscillation mode, both the P10/OSC0 and P11/OSC1 pins can be used as general-purpose input ports.
Figure 6-6 shows the circuit configuration in PLL oscillation mode.

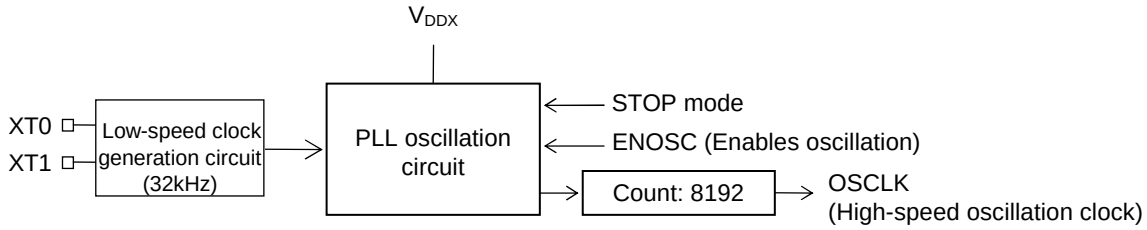


Figure 6-6 Circuit Configuration in PLL Oscillation Mode

Note:
When OSCLK is selected through SYSC1 or SYSC0 of FCON0 in PLL oscillation mode, about 8MHz, which is the same as 1/2OSCLK, is selected.

6.3.2.2 Crystal/Ceramic Oscillation Mode

In crystal/ceramic oscillation mode, both the OSC0/P10 pin and the OSC1/P11 pin are used for crystal/ceramic oscillation.
In this mode, a crystal unit or a ceramic resonator is externally connected to the OSC0/P10 and OSC1/P11 pins. If the high-speed oscillation clock pulse count reaches 4096 after oscillation is enabled, the clock is output to OSCLK (high-speed oscillation clock).
Figure 6-7 shows the circuit configuration in crystal/ceramic oscillation mode.

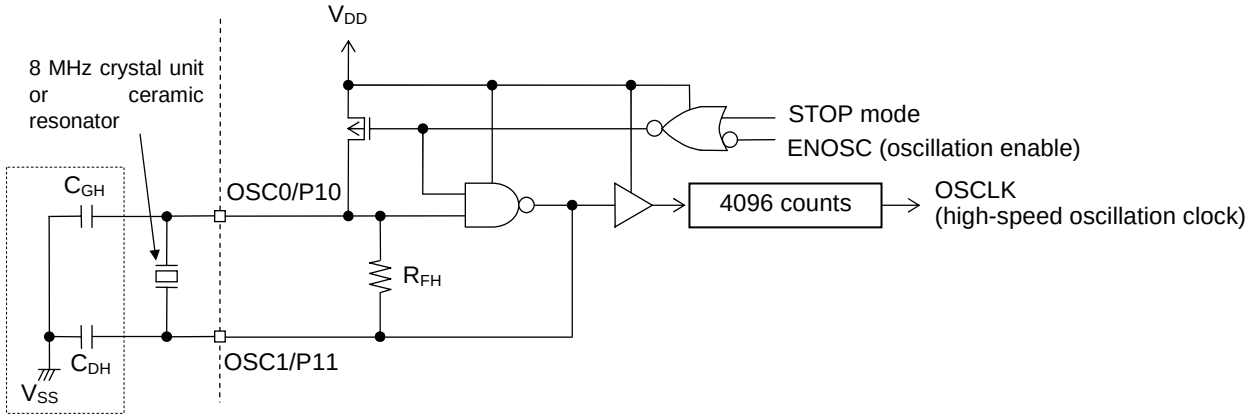


Figure 6-7 Circuit Configuration of Crystal/Ceramic Oscillation Mode

Notes:
- Mount a crystal unit or a ceramic resonator as close to the LSI as possible and make sure that neither signals causing noise nor power supply wiring are near the crystal unit or ceramic resonator and their wiring.

- Be aware that oscillation may stop due to condensation.
- The frequency of the crystal unit or ceramic resonator connected to the OSC0 and OSC1/P11 pins must not exceed 8.4 MHz.

6.3.2.3 High-Speed External Clock Input Mode

In high-speed external clock input mode, an external clock is input from the P10/OSC0 pin.
Figure 6-8 shows the circuit configuration in high-speed external clock input mode.

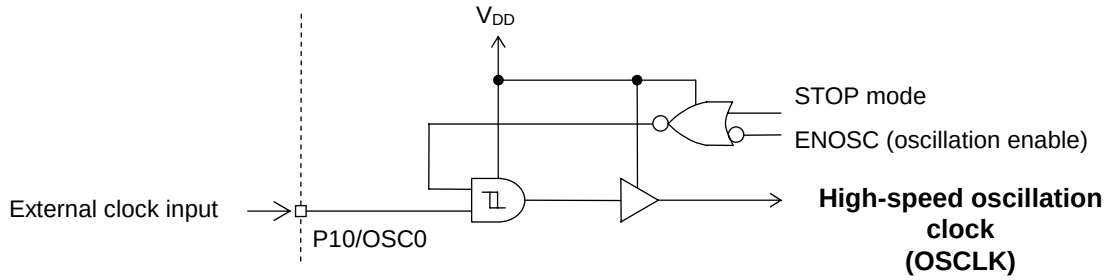


Figure 6-8 Circuit Configuration in High-Speed External Clock Input Mode

Notes:

- Since a diode is connected between the P10/OSC0 pin and DV_{DD} and between the P10/OSC0 pin and DV_{SS}, do not apply voltages higher than DV_{DD} and lower than DV_{SS} to the P10/OSC0 pin.
- If the P10/OSC0 pin is left open in high-speed external clock input mode, excessive current can flow. Therefore, be sure to input a "H" level (DV_{DD}) or a "L" level (DV_{SS}) to the P10/OSC0 pin.
- The clock that is input must not exceed 8.4 MHz.

6.3.2.4 Operation of High-Speed Clock Generation Circuit

The high-speed clock generation circuit starts with built-in PLL oscillation mode by reset generation at the time of the power supply injection. The LSI shifts to a system reset mode by reset generation at the time of the power on and shifts to a program operation mode after oscillation stabilization period (8192 counts) for high-speed clock, and a CPU starts operations. High-speed oscillation clock (OSCLK) is supplied to the peripheral circuits at the same time.
Figure 6-9 shows the waveforms of the high-speed clock generation circuit at power-on.

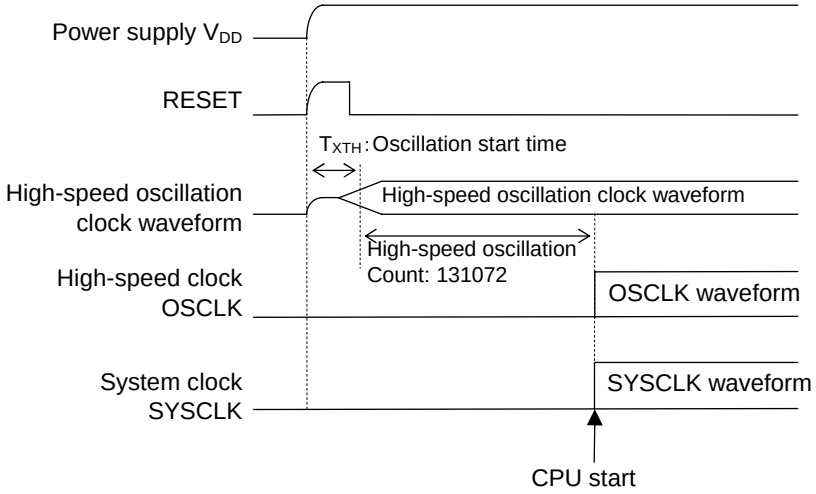


Figure 6-9 Operation of the High-Speed Clock Generation Circuit at Power-On

For the high-speed clock generation circuit, starting/stopping oscillation can be controlled by the frequency control register 1 (FCON1).
Setting the ENOSC bit of FCON1 to "1" starts oscillation. After the start of oscillation, HSCLK starts to be supplied to the peripheral circuits following a lapse of the high-speed oscillation start period (T_{XTH}/T_{EXT}) in each mode and the oscillation stabilization period of the high-speed oscillation clock (OSCLK).
The high-speed clock generation circuit stops oscillation when it enters STOP mode by software. It resumes oscillation when the STOP mode is released by an external interrupt. Then, HSCLK starts to be supplied to the peripheral circuits following a lapse of the high-speed oscillation start period (T_{XTH}/T_{EXT}) in each mode and the oscillation stabilization period of the high-speed clock (OSCLK). The oscillation stabilization period is the duration of 128 clock pulses in high-speed external clock input mode, the duration of 8192 clock pulses in built-in PLL oscillation mode and the duration of 4096 clock pulses in crystal/ceramic oscillation mode.
Figure 6-10 shows the waveforms of the high-speed clock generation circuit in crystal/ceramic oscillation mode.

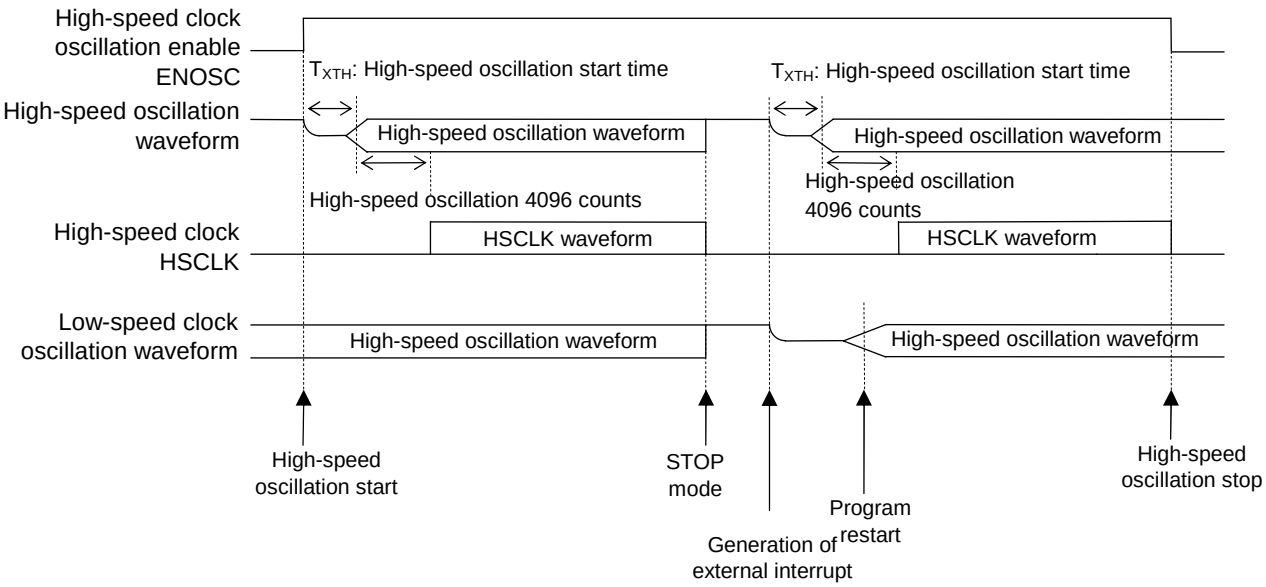


Figure 6-10 Operation of the High-Speed Clock Generation Circuit in Crystal/Ceramic Oscillation Mode

6.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-11 shows a flow of system clock switching processing (HSCLK→LSCLK) and Figure 6-12 shows a flow of system clock switching processing (LSCLK→HSCLK).

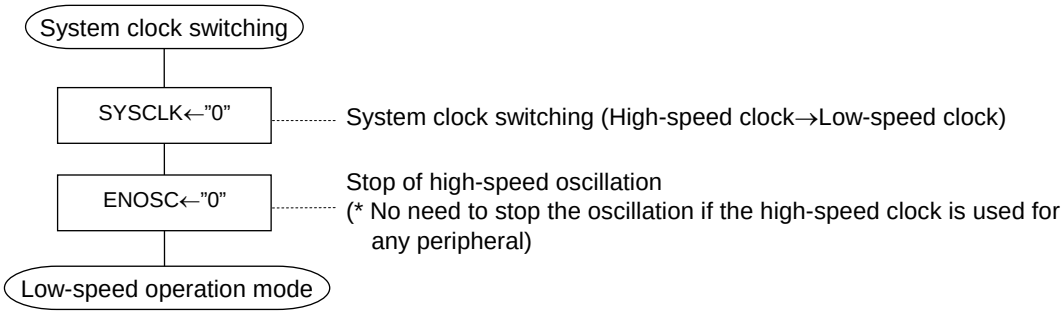


Figure 6-11 Flow of System Clock Switching Processing (HSCLK→LSCLK)

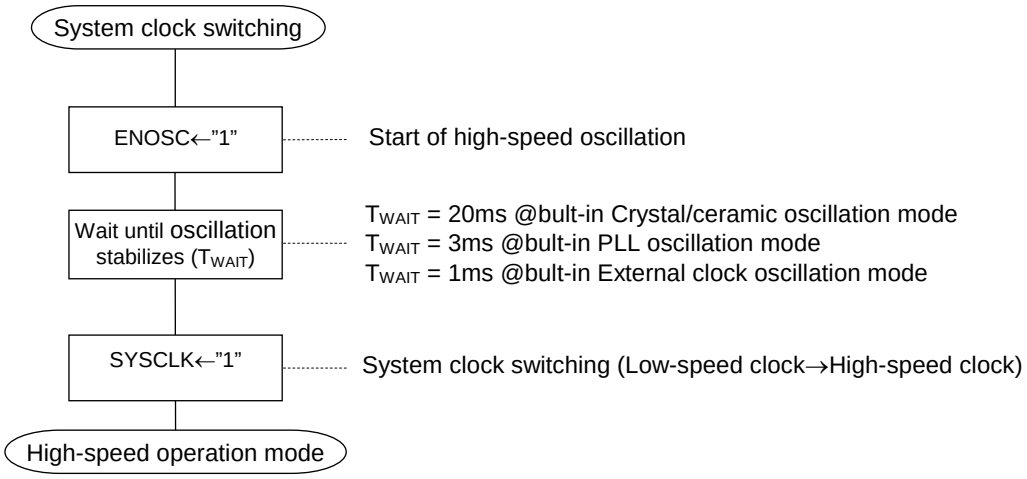


Figure 6-12 Flow of System Clock Switching Processing (LSCLK→HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Register setup of the port

For enable a clock output function, each related port register needs to be set up. Refer to the Chapter 17, "Port 2", the Chapter 18, "Port 3" for details of each register.

6.4.1 When the P21 pin (OUTCLK:output) operates as the high-speed clock output function

The high-speed clock output is selected as the secondary function of the P21 pin by setting P21MD bit (P2MOD register: bit1) to "1".

register	P2MOD register (Address:0F214H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	P23MD	P22MD	**P21MD**	P20MD
value	-	-	-	-	*	*	**1**	*

The state of the P21 pin is selected as CMOS output mode by setting P21C1 bit (P2CON1 register:bit1) to "1" and setting P21C0 bit (P2CON0 register:bit1) to "1".

register	P2CON1 register (Address:0F213H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	P23C1	P22C1	**P21C1**	P20C1
value	-	-	-	-	*	*	**1**	*

register	P2CON0 register (Address:0F212H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	P23C0	P22C0	**P21C0**	P20C0
value	-	-	-	-	*	*	**1**	*

As for P21D bit (P2D register:bit1), neither "0" nor "1" is problematic.

register	P2D register (Address:0F210H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	P23D	P22D	**P21D**	P20D
value	-	-	-	-	*	*	**	*

- : not exist
* : no relation to the high-speed clock output function
**: Don't care

Note:
Since the P21 pin (Port 2) is only for output, it does not have a register which chooses the input/output direction.

6.4.2 When the P20 pin (LSCLK:output) operates as the low-speed clock output function

The low-speed clock output is selected as the secondary function of the P20 pin by setting P20MD bit (P2MOD register: bit0) to "1".

register	P2MOD register (Address:0F214H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	P23MD	P22MD	P21MD	**P20MD**
value	-	-	-	-	*	*	*	**1**

The state of the P20 pin is selected as CMOS output mode by setting P20C1 bit (P2CON1 register:bit0) to "1" and setting P20C0 bit (P2CON0 register:bit0) to "1".

register	P2CON1 register (Address:0F213H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	P23C1	P22C1	P21C1	**P20C1**
value	-	-	-	-	*	*	*	**1**

register	P2CON0 register (Address:0F212H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	P23C0	P22C0	P21C0	**P20C0**
value	-	-	-	-	*	*	*	**1**

As for P20D bit (P2D register:bit0), neither "0" nor "1" is problematic.

register	P2D register (Address:0F210H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	P23D	P22D	P21D	**P20D**
value	-	-	-	-	*	*	*	******

- : not exist
* : no relation to the low-speed clock output function
**: Don't care

Note:
Since the P20 pin (Port 2) is only for output, it does not have a register which chooses the input/output direction.

6.4.3 When the P36 pin (LSCLK:output) operates as the low-speed clock output function

The low-speed clock output is selected as the secondary function of the P36 pin by setting P36MD bit (P3MOD register: bit6) to "1".

register	P3MOD1 register (Address: 0F21DH)							
bit	7	**6**	5	4	3	2	1	0
bit name	-	**P36MD1**	P35MD1	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
value	-	**0**	*	*	*	*	*	*

register	P3MOD1 register (Address: 0F21CH)							
bit	7	**6**	5	4	3	2	1	0
bit name	-	**P36MD0**	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
value	-	**1**	*	*	*	*	*	*

The state of the P36 pin is selected as CMOS output mode by setting P36C1 bit (P3CON1 register:bit6) to "1" and setting P36C0 bit (P3CON0 register:bit6) to "6".

register	P3CON1 register (Address: 0F21AH)							
bit	7	6	5	4	3	2	1	0
bit name	-	**P36C0**	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
value	-	**1**	*	*	*	*	*	*

register	P3CON0 register (Address: 0F21BH)							
bit	7	6	5	4	3	2	1	0
bit name	-	**P36C0**	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
value	-	**1**	*	*	*	*	*	*

P36 is set as an output pin by setting a P36DIR bit (P3DIR register:bit6) as "0."

register	P3DIR register (Address: 0F219H)							
bit	7	6	5	4	3	2	1	0
bit name	-	**P36 DIR**	P35 DIR	P34 DIR	P33 DIR	P32 DIR	P31 DIR	P30DIR
value	-	**0**	*	*	*	*	*	*

As for P36D bit (P3D register:bit6), neither "0" nor "1" is problematic.

register	P3D register (Address: 0F218H)							
bit	7	6	5	4	3	2	1	0
bit name	-	**P36 D**	P35 D	P34 D	P33 D	P32 D	P31 D	P30D
value	-	******	*	*	*	*	*	*

- : not exist
* : no relation to the low-speed clock output function
**: Don't care

Note:
Since the P36 pin (Port 3) is only for output, it does not have a register which chooses the input/output direction.

Chapter 7

Time Base Counter

7. Time Base Counter

7.1 Overview

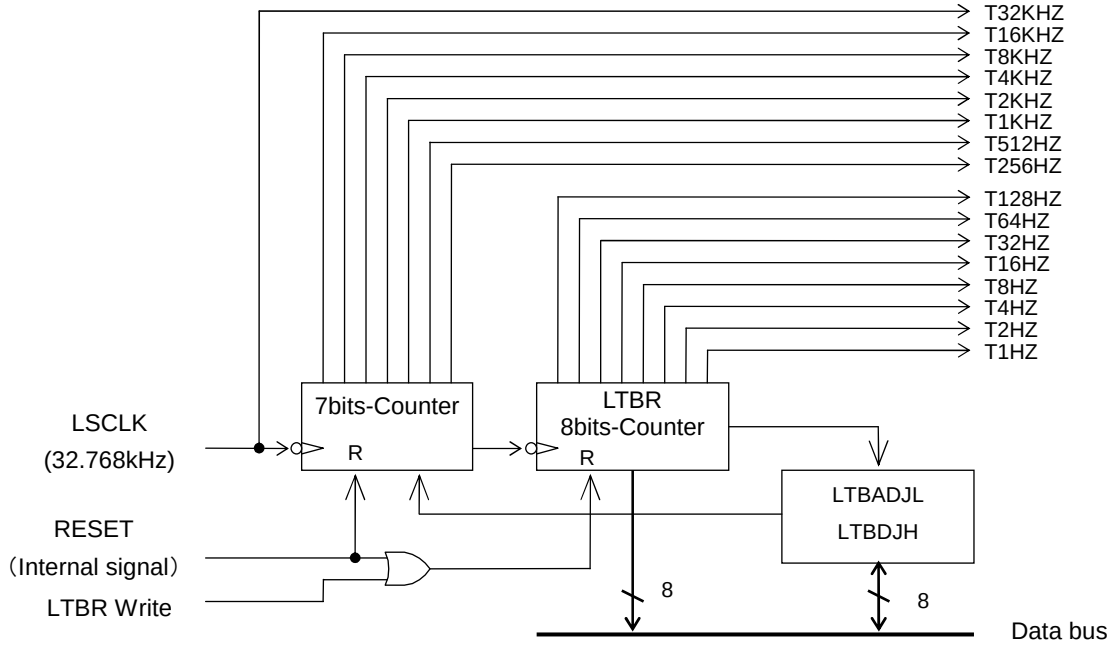
This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 6, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 5, "Interrupts".

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- Adjustment of the frequency by the low-speed time base counter frequency adjustment register (LTBADJH, LTBADJL) is possible for LTBC.(adjustment range: Approx -488ppm to +488ppm adjustment accuracy: Approx 0.48 ppm)
- HTBC generates HTB1 to HTB32 signals by dividing the high-speed clock (HSCLK) frequency.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

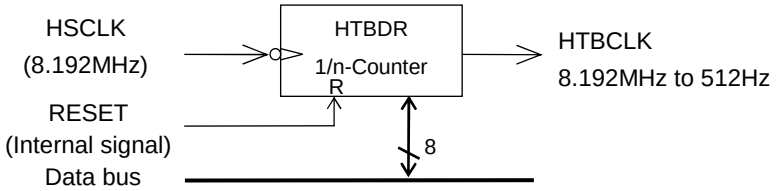
7.1.2 Configuration

Figure 7-1 and Figure 7-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.



LTBR: Low-speed time base counter register
LTBADJL: Low-speed time base counter frequency adjustment register
LTBADJH: High-speed time base counter frequency adjustment register

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)



HTBDR: High-speed time base counter frequency divide register

Figure 7-2 Configuration of High-Speed Time Base Counter

Note:
The frequency of HSCLK is changed by setting of SYSC1 bit and SYSC0 bit in the frequency control register 0 (FCON0).

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	—	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter. The T128HZ to T1HZ outputs are set to "0" when write operation is performed for LTBR.

Note:
A TBC interrupt (128Hz interrupt, 32Hz interrupt, 16Hz interrupt, or 2Hz interrupt) may occur depending on the LTBR write timing (see Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR"). Therefore, take care in software programming, refer to Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR".

7.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	—	—	—	—	HTD3	HTD2	HTD1	HTD0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the divide ratio of the 4-bit, 1/n counter.

[Description of Bits]

- **HTD3 to HTD0** (bits 3-0)
  The HTD3-HTD0 bits are used to set the frequency divide ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Divide ratio	Frequency of HTBCLK (*1)
0	0	0	0	× 1/16 (initial value)	512 kHz
0	0	0	1	× 1/15	546 kHz
0	0	1	0	× 1/14	585 kHz
0	0	1	1	× 1/13	630 kHz
0	1	0	0	× 1/12	683 kHz
0	1	0	1	× 1/11	745 kHz
0	1	1	0	× 1/10	819 kHz
0	1	1	1	× 1/9	910 kHz
1	0	0	0	× 1/8	1024kHz
1	0	0	1	× 1/7	1170kHz
1	0	1	0	× 1/6	1365kHz
1	0	1	1	× 1/5	1638kHz
1	1	0	0	× 1/4	2048kHz
1	1	0	1	× 1/3	2731kHz
1	1	1	0	× 1/2	4096kHz
1	1	1	1	× 1/1	8192kHz

*1: Indicates the frequency when the high-speed oscillation clock, HSCLK, is 8192kHz.

7.2.4 Low-Speed Time Base Counter Frequency Adjustment Registers L and H (LTBADJL, LTBADJH)

Address: 0F00CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJL	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F00DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJH	—	—	—	—	—	LADJS	LADJ9	LADJ8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBADJL and LTBADJH are special function registers (SFRs) to set the frequency adjustment values of the low-speed time base clock.

[Description of Bits]

- **LADJS, LADJ9-LADJ8** (bits 2-0) **LADJ7-LADJ0** (bits 7-0)
  The LADJS and LADJ9 to LADJ0 bits are used to adjust frequency.
  Adjustment range: Approx. −488ppm to +488ppm.
  Adjustment accuracy: Approx. 0.48ppm
  See Section 7.3.3, "Low-Speed Time Base Counter Frequency Adjustment Function" for the correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T32HZ, T16HZ, and T1HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T2HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-3 shows an example of program to read LTBR.

```
        LEA     offset LTBR         ; EA←LTBR address
MARK:
        L       R0,     [EA]        ; 1st read
        L       R1,     [EA]        ; 2nd read
;
        CMP     R0,     R1          ; Comparison for LTBR
        BNE     MARK                ; To MARK when the values do not coincide
;
            :
```

Figure 7-3 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid. Since an interrupt occurs if a falling edge occurs in the T128Hz to T1Hz outputs during writing to LTBR, take care in software programming.
Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

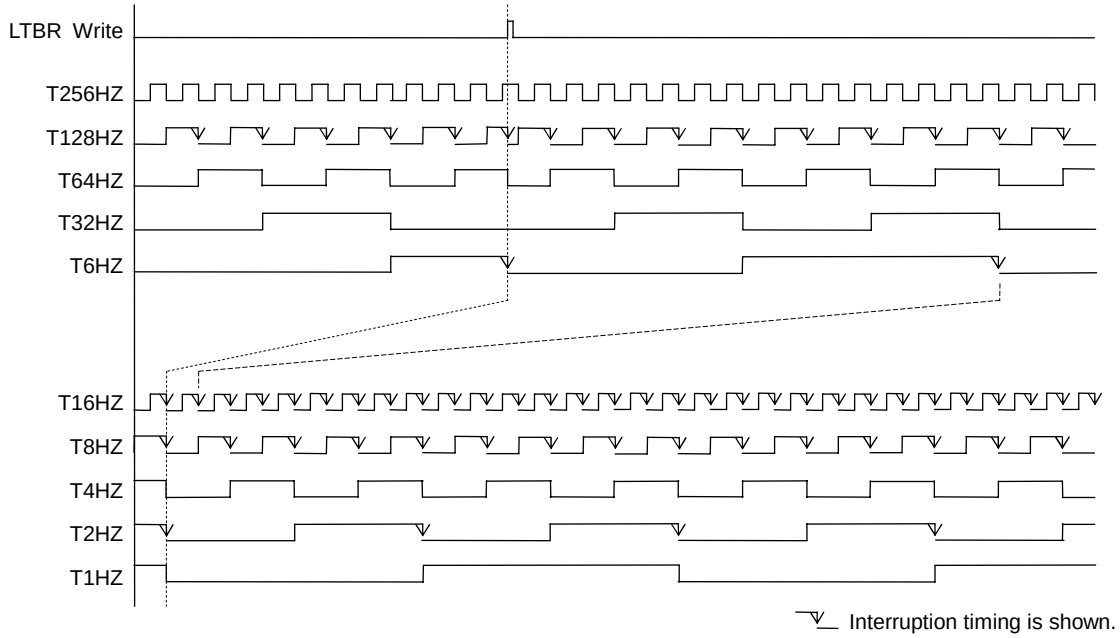


Figure 7-4 Interrupt Timing and Reset Timing by Writing to LTBR

Note:
Since QnH may be set to "1" immediately after the instruction of QnH when an instruction of "LTBR=0x00; QnH=0;" is located, locate an instruction of LTBR=0x00; NOP; QnH=0; (Locate the NOP instruction between LTBR=0x00; and QnH=0;.).

7.3.2 High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16×HSCLK to 1/1×HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as a timer.
Figure 7-5 shows the output waveform of HTBCLK.

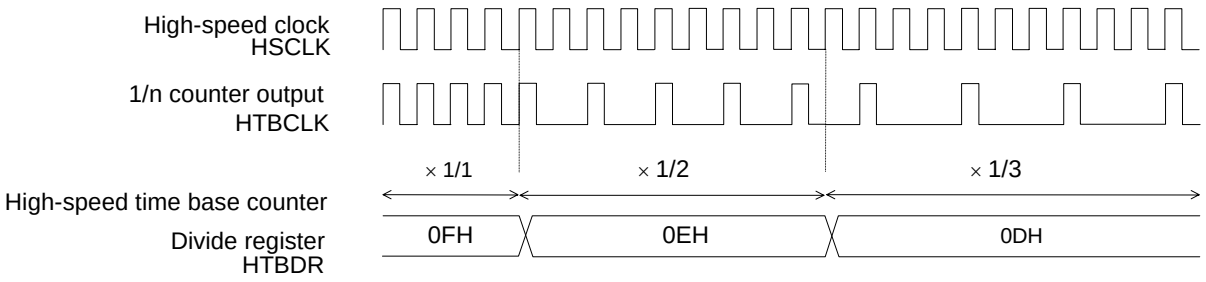


Figure 7-5 Output Waveform of HTBCLK

7.3.3 Low-Speed Time Base Counter Frequency Adjustment Function

Frequency adjustment (Adjustment range: Approx. –488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) is possible for outputs of T8KHZ to T1HZ of LTBC by using the low-speed time base counter frequency adjust registers (LTBADJH and LTBADJL).
Table7-1 shows correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

Table 7-1 Correspondence between Frequency Adjustment Values (LTBADJH, LTBADJL) and Adjustment Ratio

LADJ10 to 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	–0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	–0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	–487.80
1	0	0	0	0	0	0	0	0	0	0	400H	–488.28

The adjustment values (LADJ10 to LADJ0) to be set in LTBADJH and LTBADJL can be obtained by using the following equations:

Adjustment value = Frequency adjustment ratio × 2097152 (decimal)
= Frequency adjustment ratio × 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (gaining time)
Adjustment value = +15.0ppm × 2097152 (decimal)
= $+15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≅ 01Fh (hexadecimal)

Example 2: When adjusting –25.5ppm (losing time)
Adjustment value = –25.5ppm × 2097152 (decimal)
= $-25.5 \times 10^{-6} \times 2097152$
= –53.477376 (decimal)
≅ 7CCh (hexadecimal)

Note:
The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function.
The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

Chapter 8

Timers

8. Timers

8.1 Overview

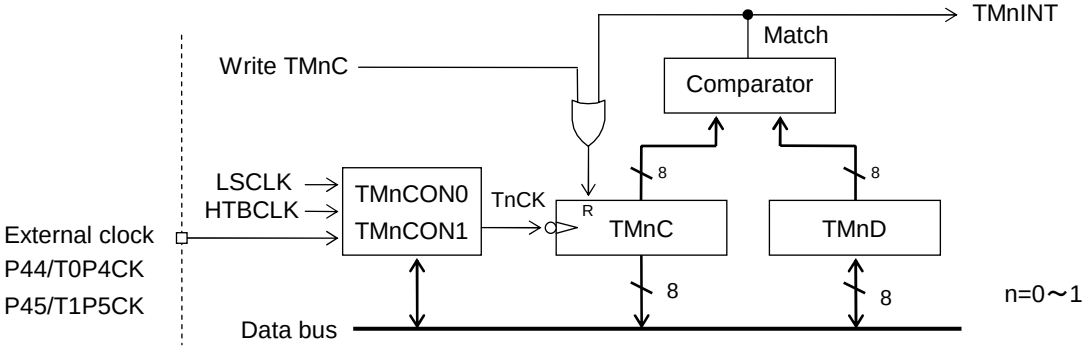
This LSI has a 6-channels of 8-bit timers.
For input clocks, see Chapter 6, "Clock Generation Circuit".

8.1.1 Features

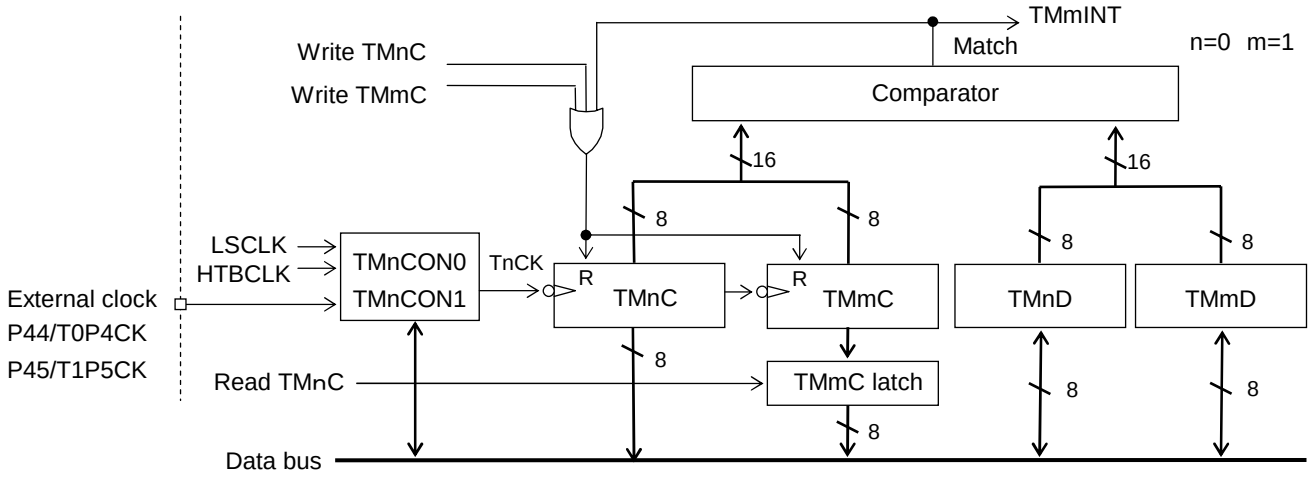
- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=0,1,8 to B) and timer data register (TMnD) coincide.
- A timer configured by combining timer 0 and timer 1, timer 8 and timer 9, timer A and timer B can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK), high-speed time base clock (HTBCLK), or external clock can be selected.
- The timer out signal of a timer 9 and Timer B (TM9OUT,TMBOUT) can be outputted.
- Positive logic or negative logic can be selected for the output logic of TM9OUT, TMBOUT signal.
- Auto reload timer mode and one shot timer mode can be selected.

8.1.2 Configuration

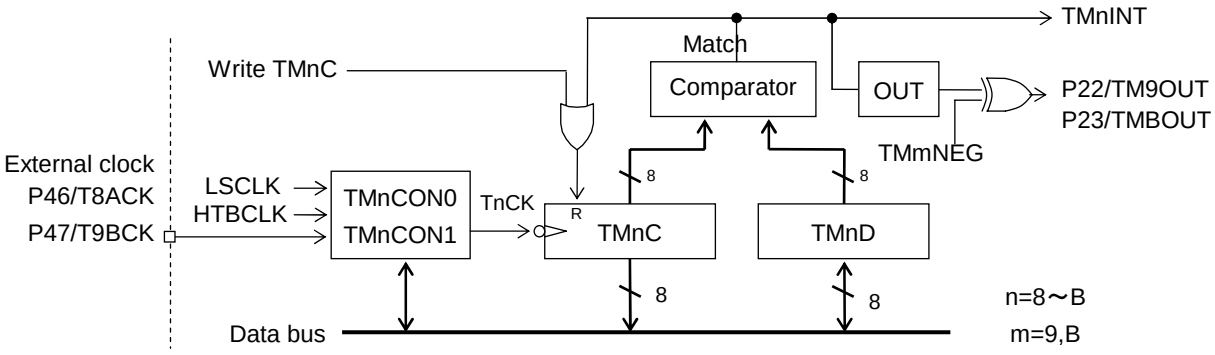
Figure 8-1 shows the configuration of the timers.



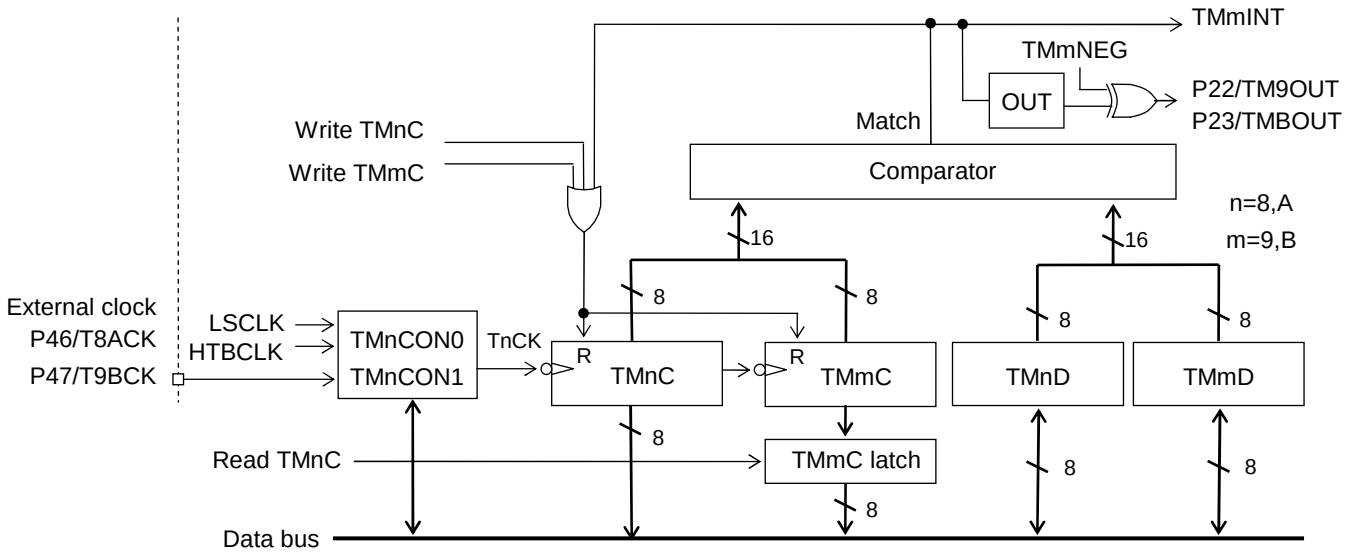
(a) At the 8bit timer mode (Timer 0 to 1)



(b) At the 16bit timer mode (timer 0 to 1)



(c) 8-bit Timer Mode (Timers 8 to B)



(d) At the 16-bit Timer Mode (Timers 8 to B)

TMnCON0 : Timer control register 0
TMnCON1 : Timer control register 1
TMmD, TMnD : Timer data registers
TMmC, TMnC: Timer counter registers

Figure 8-1 Configuration of Timers

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H
0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R/W	8	00H
0F8E0H	Timer 2 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 2 counter register	TM8C		R/W	8	00H
0F8E2H	Timer 2 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 2 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 3 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 3 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 3 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 3 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer 4 data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer 4 counter register	TMAC		R/W	8	00H
0F8EAH	Timer 4 control register 0	TMACON0	TMACON	R/W	8/16	00H
0F8EBH	Timer 4 control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer 5 data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer 5 counter register	TMBC		R/W	8	00H
0F8EEH	Timer 5 control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer 5 control register 1	TMBCON1		R/W	8	00H

8.2.2 Timer 0 Data Register (TM0D)

Address: 0F030H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM0D	T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM0D is a special function register (SFR) to set the value to be compared with the timer 0 counter register (TM0C) value.

Note:
Set TM0D when the Timer 0 stops (T0STAT bit of TM0CON1 register is "0").
When "00H" is written in TM0D, TM0D is set to "01H".

8.2.3 Timer 1 Data Register (TM1D)

Address: 0F034H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM1D	T1D7	T1D6	T1D5	T1D4	T1D3	T1D2	T1D1	T1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM1D is a special function register (SFR) to set the value to be compared with the value of the timer 1 counter register (TM1C).

Note:
Set TM1D when the Timer 1 stops (T1STAT bit of TM1CON1 register is "0").
When "00H" is written in TM1D, TM1D is set to "01H".

8.2.4 Timer 8 Data Register (TM8D)

Address: 0F8E0H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM2D	T8D7	T8D6	T8D5	T8D4	T8D3	T8D2	T8D1	T8D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM8D is a special function register (SFR) to set the value to be compared with the value of the timer 8 counter register (TM8C).

Note:
Set TM8D when the Timer 8 stops (T8STAT bit of TM8CON1 register is "0").
When "00H" is written in TM8D, TM8D is set to "01H".

8.2.5 Timer 9 Data Register (TM9D)

Address: 0F8E4H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM3D	T9D7	T9D6	T9D5	T9D4	T9D3	T9D2	T9D1	T9D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM9D is a special function register (SFR) to set the value to be compared with the value of the timer 9 counter register (TM9C).

Note:
Set TM9D when the Timer 9 stops (T9STAT bit of TM9CON1 register is "0").
When "00H" is written in TM9D, TM9D is set to "01H".

8.2.6 Timer A Data Register (TMAD)

Address: 0F8E8H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM4D	TAD7	TAD6	TAD5	TAD4	TAD3	TAD2	TAD1	TAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMAD is a special function register (SFR) to set the value to be compared with the value of the timer A counter register (TMAC).

Note:
Set TMAD when the Timer A stops (TASTAT bit of TMACON1 register is "0").
When "00H" is written in TMAD, TMAD is set to "01H".

8.2.7 Timer B Data Register (TMBD)

Address: 0F8ECH
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMBD	TBD7	TBD6	TBD5	TBD4	TBD3	TBD2	TBD1	TBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMBD is a special function register (SFR) to set the value to be compared with the value of the timer B counter register (TMBC).

Note:
Set TMBD when the Timer B stops (TBSTAT bit of TMBCON1 register is "0").
When "00H" is written in TMBD, TMBD is set to "01H".

8.2.8 Timer 0 Counter Register (TM0C)

Address: 0F031H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0C	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM0C is performed, TM0C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM0C) or the higher counter (TM1C), both the lower and higher counters are set to "0000H".

During timer operation, the contents of TM0C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TM0C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-1 TM0C Read Enable/Disable during Timer Operation

Timer clock T0CK	System clock SYSCLK	TM0C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM0C twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.9 Timer 1 Counter Register (TM1C)

Address: 0F035H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1C	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM1C is performed, TM1C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM0C) or the higher counter (TM1C), both the lower and higher counters are set to "0000H".
When reading TM1C in 16-bit timer mode, be sure to read TM0C first since the count value of TM1C is stored in the TM1C latch when TM0C is read.

During timer operation, the contents of TM1C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TM1C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-2 TM1C Read Enable/Disable during Timer Operation

Timer clock T1CK	System clock SYSCLK	TM1C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM1C twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.10 Timer 8 Counter Register (TM8C)

Address: 0F8E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8C	T8C7	T8C6	T8C5	T8C4	T8C3	T8C2	T8C1	T8C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM8C is performed, TM8C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM8C) or the higher counter (TM3C), both the lower and higher counters are set to "0000H".

During timer operation, the contents of TM8C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TM8C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-3 TM8C Read Enable/Disable during Timer Operation

Timer clock T8CK	System clock SYSCLK	TM8C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM8C twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.11 Timer 9 Counter Register (TM9C)

Address: 0F8E5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9C	T9C7	T9C6	T9C5	T9C4	T9C3	T9C2	T9C1	T9C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM9C is performed, TM9C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM8C) or the higher counter (TM9C), both the lower and higher counters are set to "0000H".
When reading TM9C in 16-bit timer mode, be sure to read TM8C first since the count value of TM9C is stored in the TM9C latch when TM8C is read.

During timer operation, the contents of TM9C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TM9C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-4 TM9C Read Enable/Disable during Timer Operation

Timer clock T9CK	System clock SYSCLK	TM9C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM9C twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.12 Timer A Counter Register (TMAC)

Address: 0F8E9H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMAC	TAC7	TAC6	TAC5	TAC4	TAC3	TAC2	TAC1	TAC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMAC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMAC is performed, TMAC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TMAC) or the higher counter (TMBC), both the lower and higher counters are set to "0000H".

During timer operation, the contents of TMAC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TMAC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-5 TMAC Read Enable/Disable during Timer Operation

Timer clock TACK	System clock SYSCLK	TMAC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMAC twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.13 Timer B Counter Register (TMBC)

Address: 0F8EDH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBC	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMBC is performed, TMBC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TMAC) or the higher counter (TMBC), both the lower and higher counters are set to "0000H".
When reading TMBC in 16-bit timer mode, be sure to read TMAC first since the count value of TMBC is stored in the TMBC latch when TMAC is read.

During timer operation, the contents of TMBC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TMBC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-6 TMBC Read Enable/Disable during Timer Operation

Timer clock TBCK	System clock SYSCLK	TMBC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMBC twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

8.2.14 Timer 0 Control Register 0 (TM0CON0)

Address: 0F032H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON0	—	—	—	—	—	T01M16	T0CS1	T0CS0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON0 is a special function register (SFR) to control timer 0.
Rewrite TM0CON0 while the timer 0 is stopped (T0STAT of the TM0CON1 register is "0").

[Description of Bits]

- **T0CS1, T0CS0** (bits 1, 0)
  The T0CS1 and T0CS0 bits are used for selecting the operation clock of timer 0. LSCLK, HTBCLK, or the external clock (P44/T0P0CK) can be selected by these bits.

T0CS1	T0CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer 0 does not operate)
1	1	External clock (P44/T0P0CK)

- **T01M16** (bit 2)
  The T01M16 bit is used for selecting the operating mode of timer 0 or timer 1. When the T01M16 bit is set to "1", timer 0 and timer 1 are connected and they operate as a 16-bit timer.
  In 8-bit timer mode, each timer 0 and timer 1 are operate as independent 8-bit timer.
  In 16-bit timer mode, timer 0 and timer 1 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 1 is incremented by a timer 0 overflow signal. A timer 0 interrupt (TM0INT) is not generated.

T01M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

8.2.15 Timer 1 Control Register 0 (TM1CON0)

Address: 0F036H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON0	—	—	—	—	—	—	T1CS1	T1CS0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON0 is a special function register (SFR) to control timer 1.
Rewrite TM1CON0 while timer 1 is stopped (T1STAT of the TM1CON1 register is "0").

[Description of Bits]

- **T1CS1, T1CS0** (bits 1, 0)
  The T1CS1 and T1CS0 bits are used for selecting the operation clock of timer 1. LSCLK, HTBCLK, or the external clock (P45/T1P1CK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T01M16 of TM0CON to "1", the values of T1CS1 and T1CS0 are invalid.

T1CS1	T1CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	External clock (P45/ T1P1CK)

8.2.16 Timer 8 Control Register 0 (TM8CON0)

Address: 0F8E2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON0	T8OST	—	T89M16	—	—	—	T8CS1	T8CS0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON0 is a special function register (SFR) to control timer 8.
Rewrite TM8CON0 while the timer 8 is stopped (T8STAT of the TM8CON1 register is "0").

[Description of Bits]

- **T8CS1, T8CS0** (bits 1, 0)
  The T8CS1 and T8CS0 bits are used for selecting the operation clock of timer 8. LSCLK, HTBCLK, or the external clock (P04/T08P0CK) can be selected by these bits.

T8CS1	T8CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited
1	1	External clock

- **T89M16** (bit 5)
  The T89M16 bit is used for selecting the operating mode of timer 8 or timer 9. When the T89M16 bit is set to "1", timer 8 and timer 9 are connected and they operate as a 16-bit timer.
  In 8-bit timer mode, each timer 8 and timer 9 are operate as independent 8-bit timer.
  In 16-bit timer mode, timer 8 and timer 9 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 9 is incremented by a timer 8 overflow signal. A timer 8 interrupt (TM8INT) is not generated.

T89M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **T8OST** (bit 7)
  T8OST is a bit which selects the timer mode of a timer 8.If T8OST is set to "1", one shot timer mode can be used.

T8OST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.17 Timer 9 Control Register 0 (TM9CON0)

Address: 0F8E6H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON0	T9OST	T9NEG	—	—	—	—	T9CS1	T9CS0
R/W	R/W	R/W	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON0 is a special function register (SFR) to control timer 9.
Rewrite TM9CON0 while timer 9 is stopped (T9STAT of the TM9CON1 register is "0").

[Description of Bits]

- **T9CS1, T9CS0** (bits 1, 0)
  The T9CS1 and T9CS0 bits are used for selecting the operation clock of timer 9. LSCLK, HTBCLK, or the external clock (P47/T9BCK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T89M16 of TM8CON to "1", the values of T9CS1 and T9CS0 are invalid.

T9CS1	T9CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	External clock (P47/ T9BCK)

- **T9NEG** (bit 6)
  A T9NEG bit selects the output logic of TM9OUT. TM9OUT output is "0" in positive logic, and "1" in negative logic.

T9NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **T9OST** (bit 7)
  T9OST bit selects the timer mode of a timer 9.If T9OST is set to "1", one shot timer mode can be used.
  When T89M16 of TM8CON0 has chosen "1" and 16-bit timer mode, the value of T9OST becomes invalid.

T9OST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.18 Timer A Control Register 0 (TMACON0)

Address: 0F8EAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON0	TAOST	—	TABM16	—	—	—	TACS1	TACS0
R/W	R/W	R	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON0 is a special function register (SFR) to control timer A.
Rewrite TMACON0 while the timer A is stopped (TASTAT of the TMACON1 register is "0").

[Description of Bits]

- **TACS1, TACS0** (bits 1, 0)
  The TACS1 and TACS0 bits are used for selecting the operation clock of timer A. LSCLK, HTBCLK, or the external clock (P46/T8ACK) can be selected by these bits.

TACS1	TACS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	External clock (P46/ T8ACK)

- **TABM16** (bit 2)
  The TABM16 bit is used for selecting the operating mode of timer A or timer B. When the TABM16 bit is set to "1", timer A and timer B are connected and they operate as a 16-bit timer.
  In 8-bit timer mode, each timer A and timer B are operate as independent 8-bit timer.
  In 16-bit timer mode, timer A and timer B are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer B is incremented by a timer A overflow signal. A timer A interrupt (TMAINT) is not generated.

TABM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **TAOST** (bit 7)
  TAOST bit selects the timer mode of a timer 9.If TAOST is set to "1", one shot timer mode can be used.
  When TABM16 of TMACON0 has chosen "1" and 16-bit timer mode, the value of TBOST becomes invalid.

TAOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.19 Timer B Control Register 0 (TMBCON0)

Address: 0F8EEH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON0	TBOST	TBNEG	—	—	—	—	TBCS1	TBCS0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON0 is a special function register (SFR) to control timer B.
Rewrite TMBCON0 while timer B is stopped (TBSTAT of the TMBCON1 register is "0").

[Description of Bits]

- **TBCS1, TBCS0** (bits 1, 0)
  The TBCS1 and TBCS0 bits are used for selecting the operation clock of timer B. LSCLK, HTBCLK, or the external clock (P47/T9BCK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting TABM16 of TM0CON to "1", the values of TBCS1 and TBCS0 are invalid.

TBCS1	TBCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	External clock (P47/ T9BCK)

- **TBNEG** (bit 6)
  A TBNEG bit selects the output logic of TMBOUT. The initial value of a TMBOUT output is "0" in positive logic, and "1" in negative logic.

TBNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **TBOST** (bit 7)
  TBOST bit selects the timer mode of a timer B.If TBOST is set to "1", one shot timer mode can be used.

TBOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.20 Timer 0 Control Register 1 (TM0CON1)

Address: 0F033H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON1	T0STAT	—	—	—	—	—	—	T0RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON1 is a special function register (SFR) to control a timer 0.

[Description of Bits]

- **T0RUN** (bit 0)
  The T0RUN bit is used for controlling count stop/start of timer 0.

T0RUN	Description
0	Stops counting
1	Starts counting

- **T0STAT** (bit 7)
  The T0STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 0.

T0STAT	Description
0	Counting stopped
1	Counting in progress

8.2.21 Timer 1 Control Register 1 (TM1CON1)

Address: 0F037H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON1	T1STAT	—	—	—	—	—	—	T1RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON1 is a special function register (SFR) to control timer 1.

[Description of Bits]

- **T1RUN** (bit 0)
  The T1RUN bit is used for controlling count stop/start of timer 1.
  In 16-bit timer mode, be sure to set this bit to "0". Timer 1 is incremented caused by a timer 0 overflow signal regardless of the value of T1RUN.

T1RUN	Description
0	Stops counting
1	Starts counting

- **T1STAT** (bit 7)
  The T1STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 1.
  In 16-bit timer mode, this bit will read "0".

T1STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.22 Timer 8 Control Register 1 (TM8CON1)

Address: 0F8E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON1	T8STAT	—	—	—	—	—	—	T8RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON1 is a special function register (SFR) to control timer 8.

[Description of Bits]

- **T8RUN** (bit 0)
  The T8RUN bit is used for controlling count stop/start of timer 8.

T8RUN	Description
0	Stops counting
1	Starts counting

- **T8STAT** (bit 7)
  The T8STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 8.

T8STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.23 Timer 9 Control Register 1 (TM9CON1)

Address: 0F8E7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON1	T9STAT	—	—	—	—	—	—	T9RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON1 is a special function register (SFR) to control timer 9.

[Description of Bits]

- **T9RUN** (bit 0)
  The T9RUN bit is used for controlling count stop/start of timer 9.
  In 16-bit timer mode, be sure to set this bit to "0". Timer 9 is incremented caused by a timer 0 overflow signal regardless of the value of T9RUN.

T9RUN	Description
0	Stops counting
1	Starts counting

- **T9STAT** (bit 7)
  The T9STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 9.
  In 16-bit timer mode, this bit will read "0".

T9STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.24 Timer A Control Register 1 (TMACON1)

Address: 0F8EBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON1	TASTAT	—	—	—	—	—	—	TARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON1 is a special function register (SFR) to control timer A.

[Description of Bits]

- **TARUN** (bit 0)
  The TARUN bit is used for controlling count stop/start of timer A.
  In 16-bit timer mode, be sure to set this bit to "0". Timer A is incremented caused by a timer 0 overflow signal regardless of the value of TARUN.

TARUN	Description
0	Stops counting
1	Starts counting

- **TASTAT** (bit 7)
  The TASTAT bit is used for indicating "counting stopped"/"counting in progress" of timer A.
  In 16-bit timer mode, this bit will read "0".

TASTAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.25 Timer B Control Register 1 (TMBCON1)

Address: 0F8EFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON1	TBSTAT	—	—	—	—	—	—	TBRUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON1 is a special function register (SFR) to control timer B.

[Description of Bits]

- **TBRUN** (bit 0)
  The TBRUN bit is used for controlling count stop/start of timer B.
  In 16-bit timer mode, be sure to set this bit to "0". Timer B is incremented caused by a timer 0 overflow signal regardless of the value of TBRUN.

TBRUN	Description
0	Stops counting
1	Starts counting

- **TBSTAT** (bit 7)
  The TBSTAT bit is used for indicating "counting stopped"/"counting in progress" of timer B.
  In 16-bit timer mode, this bit will read "0".

TBSTAT	Description
0	Counting stopped.
1	Counting in progress.

8.3 Description of Operation

When the TnRUN bit of timer 0,1,8 to B control register 1 (TMnCON1) is set to "1", the timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer 0,1,8 to B control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.

When the count value of TMnC and the timer 0,1,8 to B data register (TMnD) coincide, timer 0,1,8 to B interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing.

Whenever the value of the count value of TMnC and the preset value of a timer n data register (TMnD) is in agreement, the output value of timer out (TM9OUT, TMBOUT) is reversed. This timer out can be outputted outside as ternary function of a port 2. Timer out is set to "0" to the time of system reset, and a timer count stop.

When the TnRUN bit is set to "0", TMnC stops incrementing after counting the falling of the timer clock (TnCK) once. Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 0–7 control register 1 (TMnCON1) is "0". When the TnRUN bit is set to "1" again, TMnC restarts incrementing from the previous value. To initialize TMnC to "00H", perform a write operation to TMnC.
The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n = 0,1,8 \text{ to } B)$$

TMnD: Timer 0,1,8 to B data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 0,1,8 to B control register 0 (TMnCON0)

After the TnRUN bit is set to "1", the timer is synchronized by the timer clock to start counting. Therefore, an error of a maximum of 1 clock period occurs until the first timer interrupt occurs. The timer interrupt periods from the second time onward are constant.
Figure 8-2 shows the operation timing diagram of Timer 0,1,8 to B.

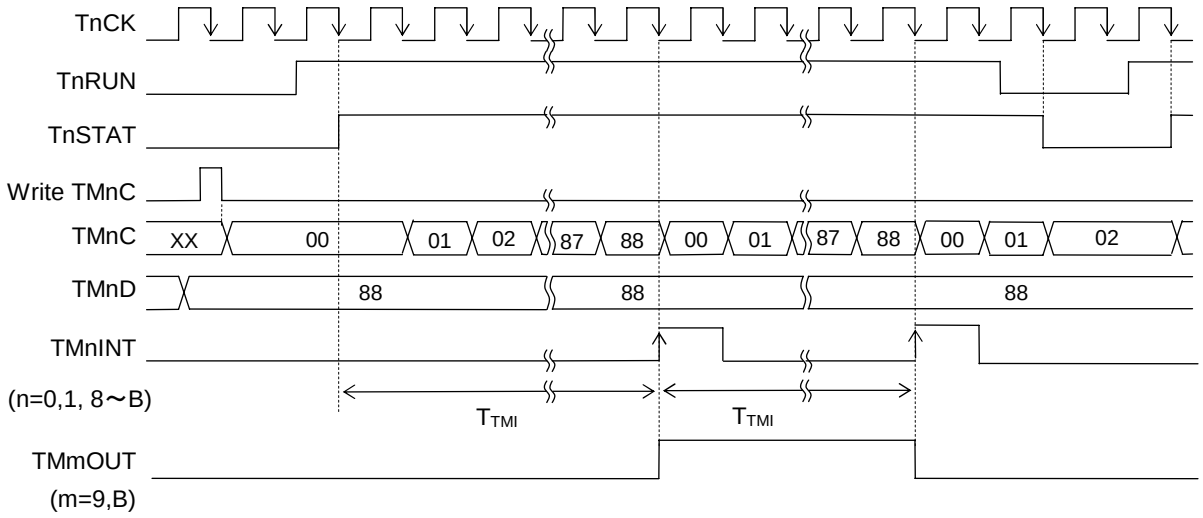


Figure 8-2 Operation Timing Diagram of Timer 0,1,8 to B

Note:
Even if "0" is written to the TnRUN bit, counting operation continues up to the falling edge (the timer 0,1,8 to B status flag (TnSTA) is in a "1" state) of the next timer clock pulse. Therefore, the timer 0,1,8 to B interrupt (TMnINT) may occur.

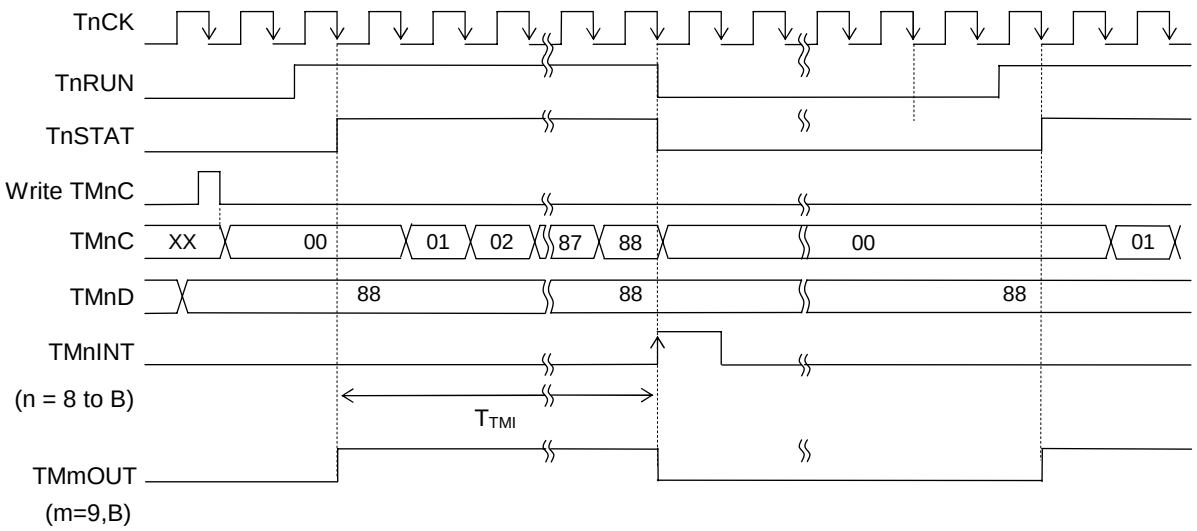


Figure 8-3 One-shot timer mode Operation Timing Diagram of Timer 8 to B

Note:
When the count value of TMnC and the value of a timer 8 to B data register (TMnD) are in agreement, a TnRUN bit is cleared automatically.

Chapter 9

Watchdog Timer

9 Watchdog Timer

9.1 Overview

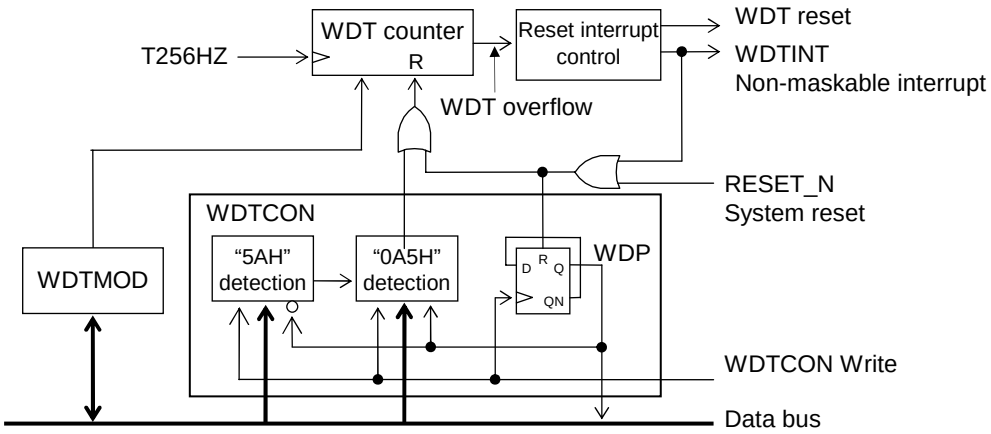
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, "Interrupts," and for WDT interrupt see Chapter 3, "Reset Function".

9.1.1 Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Non maskable interruption is required at the first overflow.
- Reset generated by the second overflow

9.1.2 Configuration

Figure 9-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 9-1 Configuration of Watchdog Timer

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	−	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	−	R/W	8	02H

9.2.2 Watchdog Timer Control Register（WDTCON）

Address：0F00EH
Access：W
Access size：8 bits
Initial value：00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0**（bit 0）
  The value of the internal pointer (WDP) is read from this bit.
  WDT is reset to "0" when the system reset and the overflow of the WDT counter, and reverse every write operation to WDTCON.

- **d7～d0**（bits 7～0）
  This bit is used to write data to clear the WDT counter.
  WDT counter can be cleared by writing in "5AH", when an internal pointer is "0", and then writing in "0A5H", when WDP is "1".

Note:
After the WDT interrupt (WDTINT) occurs, writing to the WDTCON register is disabled for about 15.25us. Therefore, when the WDT cleared , confirm that the WDP is reversed by writing to the WDTCON register.
Refer to an example of programing "9.3.1 Handling example when you do not want to use the watch dog timer".

9.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	–	–	–	–	–	–	WDT1	WDT0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT1～0** (bits 1～0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set a overflow period (TWOV) of the WDT counter. One of 125ms, 500ms, 2s, and 8s can be selected.

WDT1	WDT0	Description
0	0	125ms
0	1	500ms
1	0	2s (initial value)
1	1	8s

9.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start..
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (TWOV) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 9-1.

Table 9-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125ms	Approx 121ms
0	1	500ms	Approx 496ms
1	0	2000ms	Approx 1996ms
1	1	8000ms	Approx 7996ms

Figure 9-2 shows an example of watchdog timer operation.

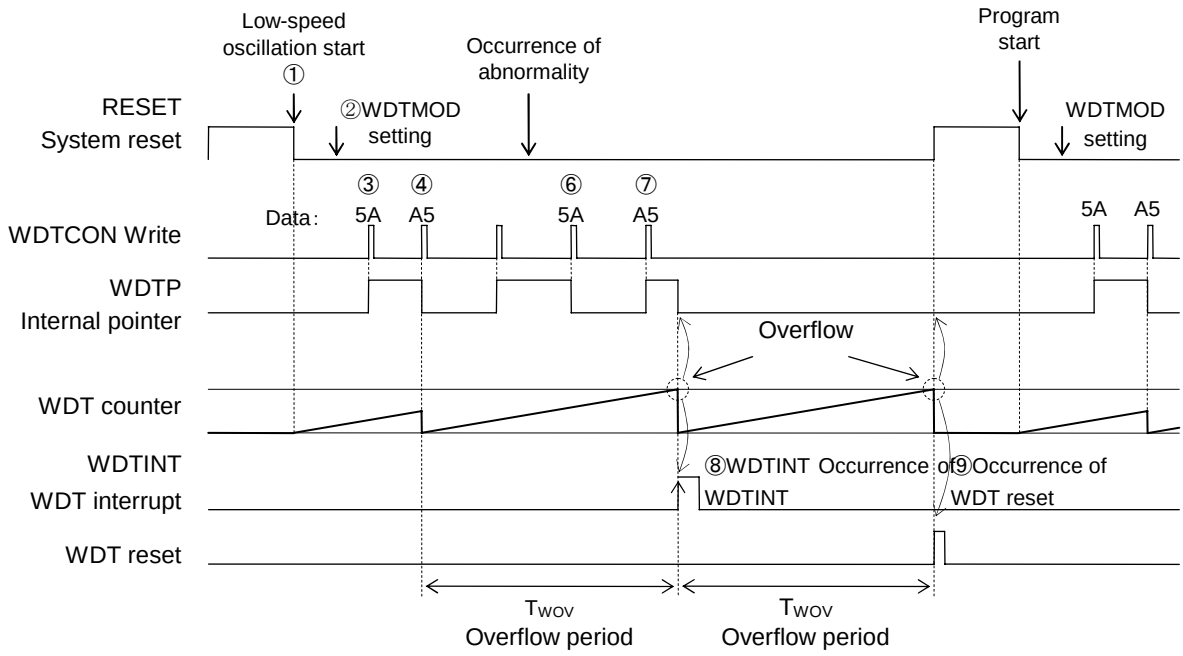


Figure 9-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
③ "5AH" is written to WDTCON. (Internal pointer 0→1)
④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1→0)
⑤ "5AH" is written o WDTCON. (Internal pointer 0→1)
⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1→0)
⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in ⑥. (Internal pointer 0→1)
⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case, the WDT counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.25us).
⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Note:
- In STOP mode, the watchdog timer operation also stops.
- In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
- The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

9.3.1 Handling example when you do not want to use the watch dog timer

WDT counter is a free-run counter that starts count-up automatically after the system reset released and the low-speed clock (LSCLK) starts oscillating. If the WDT counter gets overflow, the WDT non-maskable interrupt occurs and then a system reset occurs. Therefore, it is needed to clear the WDT counter even if you do not want to use the WDT as a fale-safe function.
See following example programming codes to clear the WDT counter in the interrupt routine.

Example programming code:

```
__DI();                    // Disable multi-interrupts
do
{
   WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
 __EI();
```

Chapter 10

PWM

10. PWM

10.1 Overview

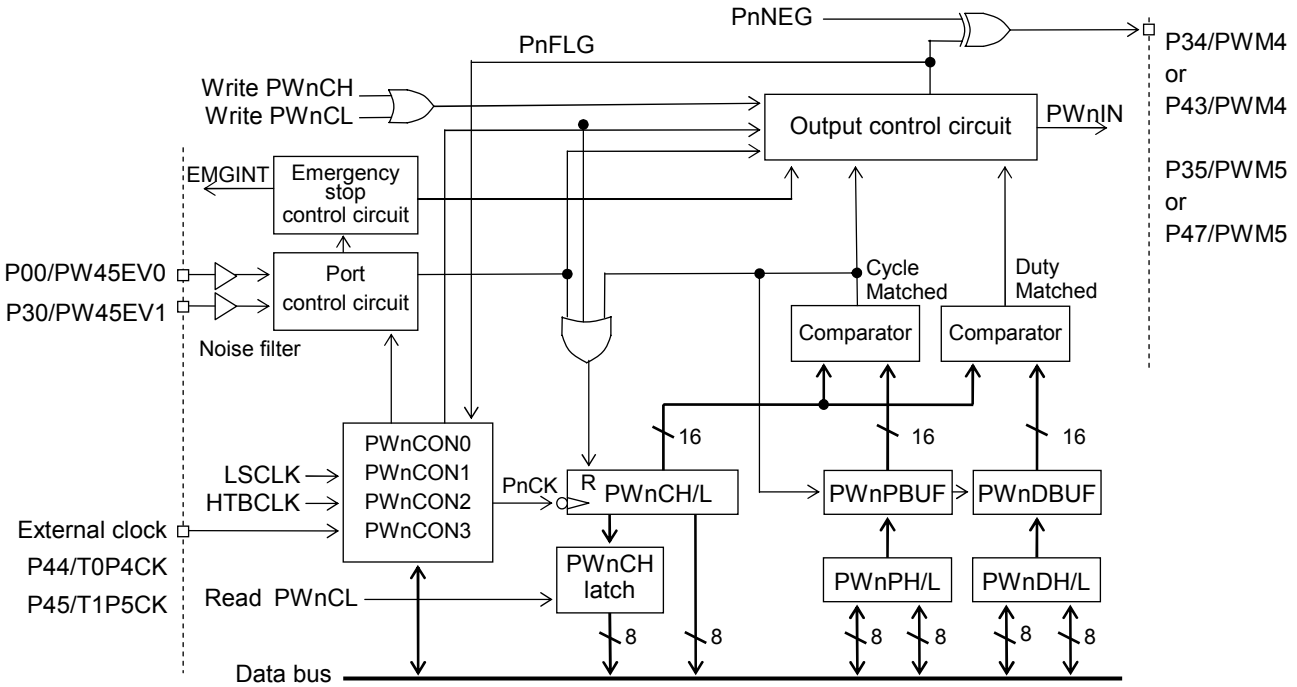
This LSI includes two channels of 16-bit PWM (Pulse Width Modulation).
The PWM4 output (PWM4) function is assigned to P34 (Port 3) and P43 (Port 4) as the tertiary function. The PWM5 output (PWM5) function is assigned to P35 (Port 3) and P47 (Port 4) as the tertiary function. For the functions of Port 3 and Port 4, see Chapter 18, “Port 3” and Chapter 19, “Port 4”.

10.1.1 Features

- The PWM signals with the periods of approximately 244ns (@HTBCLK=8.192MHz) to 2s (@LSCLK=32.768kHz) can be generated and output outside of the LSI.
- The output logic of the PWM signal can be switched to the positive or negative logic.
- At the coincidence of PWM signal period, duties, and period & duty, a PWM interrupt (PWnINT) occurs.
- The repeat mode/one-shot mode cab be switched.
- For the PWM clock, a low-speed clock (LSCLK), a high-speed time base clock (HTBCLK), and an external clock are available.
- PWM4 and PWM5 can cooperate.
- The dead time can be set for the PWM4 and PWM5 cooperation.
- An external input can control start/stop/clear.
- An external input can generate an emergency stop and emergency stop interrupt.

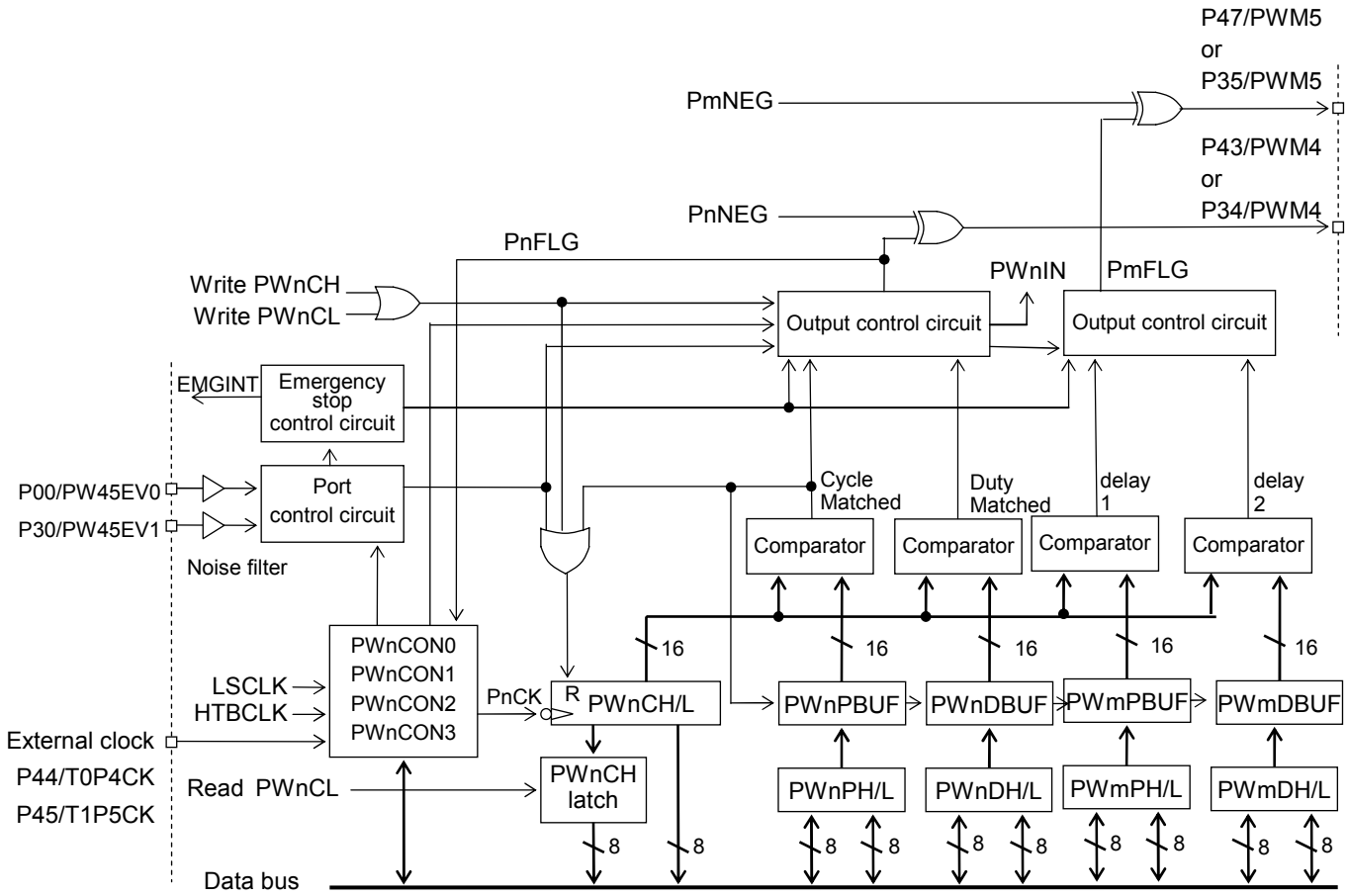
10.1.2 Configuration

Figure 10-1 shows the configuration of the PWM circuit.



PWnPL	: PWMn period register L	PWnPH	: PWMn period register H
PWnPBUF	: PWMn period buffer		
PWnDL	: PWMn duty register L	PWnDH	: PWMn duty register H
PWnDBUF	: PWMn duty buffer		
PWnCL	: PWMn counter register L	PWnCH	: PWMn counter register H
PWnCON0	: PWMn control register 0	PWnCON1	: PWMn control register 1
PWnCON2	: PWMn control register 2	PW4CON3	: PWMn control register 3

(a) In standalone mode (PWM4 to 5) n=4 to 5



(b) In cooperation mode (PWM4 to 5) n=4, m=5

Figure 10-1 Configuration of PWM Circuit

10.1.3 List of Pins

Pin name	Input/output	Function
P34/PWM4	O	PWM4 output pin Used for the tertiary function of the P34 pin.
P43/PWM4	O	PWM4 output pin Used for the tertiary function of the P43 pin.
P35/PWM5	O	PWM5 output pin Used for the tertiary function of the P35 pin.
P47/PWM5	O	PWM5 output pin Used for the tertiary function of the P47 pin.

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial Value
0F8A0H	PWM4 period register L	PW4PL	PW4P	R/W	8/16	0FFH
0F8A1H	PWM4 period register H	PW4PH		R/W	8	0FFH
0F8A2H	PWM4 duty register L	PW4DL	PW4D	R/W	8/16	00H
0F8A3H	PWM4 duty register H	PW4DH		R/W	8	00H
0F8A4H	PWM4 counter register L	PW4CL	PW4C	R/W	8/16	00H
0F8A5H	PWM4 counter register H	PW4CH		R/W	8	00H
0F8A6H	PWM4 control register 0	PW4CON0	PW4CON	R/W	8/16	00H
0F8A7H	PWM4 control register 1	PW4CON1		R/W	8	40H
0F8A8H	PWM4 control register 2	PW4CON2	–	R/W	8	00H
0F8A9H	PWM4 control register 3	PW4CON3		R/W	8	10H
0F8B0H	PWM5 period register L	PW5PL	PW5P	R/W	8/16	0FFH
0F8B1H	PWM5 period register H	PW5PH		R/W	8	0FFH
0F8B2H	PWM5 duty register L	PW5DL	PW5D	R/W	8/16	00H
0F8B3H	PWM5 duty register H	PW5DH		R/W	8	00H
0F8B4H	PWM5 counter register L	PW5CL	PW5C	R/W	8/16	00H
0F8B5H	PWM5 counter register H	PW5CH		R/W	8	00H
0F8B6H	PWM5 control register 0	PW5CON0	PW5CON	R/W	8/16	00H
0F8B7H	PWM5 control register 1	PW5CON1		R/W	8	40H
0F8B8H	PWM5 control register 2	PW5CON2	–	R/W	8	00H

10.2.2 PWM4 Period Registers (PW4PL, PW4PH)

Address: 0F8A0H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW4PL	P4P7	P4P6	P4P5	P4P4	P4P3	P4P2	P4P1	P4P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

Address: 0F8A1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW4PH	P4P15	P4P14	P4P13	P4P12	P4P11	P4P10	P4P9	P4P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

PW4PH and PW4PL are special function registers (SFRs) to set the PWM4 periods.

Note:
When PW4PH or PW4PL is set to “0000H”, the PWM4 period buffer (PW4PBUF) is set to “0001H”.
A word type transfer instruction should be used for register setting.

10.2.3 PWM4 Duty Registers (PW4DL, PW4DH)

	7	6	5	4	3	2	1	0
PW4DL	P4D7	P4D6	P4D5	P4D4	P4D3	P4D2	P4D1	P4D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4DH	P4D15	P4D14	P4D13	P4D12	P4D11	P4D10	P4D9	P4D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW4DH and PW4DL are special function registers (SFRs) to set the duties of PWM4.
If the dead time is set (P4DTMD=1) in the cooperation mode (P45MD=1), the duty of PWM4 is the sum of the setting values for PW4D and PW5D, and the setting value for PW4D is set to the PWM5 period.

Note:
For the PW4DH and PW4DL, set data smaller than for PW4PH and PW4PL.
A word type transfer instruction should be used for register setting.

10.2.4 PWM4 Counter Registers (PW4CH, PW4CL)

	7	6	5	4	3	2	1	0
PW4CL	P4C7	P4C6	P4C5	P4C4	P4C3	P4C2	P4C1	P4C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CH	P4C15	P4C14	P4C13	P4C12	P4C11	P4C10	P4C9	P4C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A5H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW4CL and PW4CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW4CL or PW4CH, it is set to “0000H”. The data that is written is meaningless.
When data is read from PW4CL, the value of PW4CH is latched. When reading PW4CH and PW4CL, use a word type instruction or read PW4CL first.

The contents of PW4CH and PW4CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock.
Table 10-1 shows PW4CH and PW4CL read enable/disable for each combination of the PWM clock and system clock.

Table 10-1 PW4CH and PW4CL Read Enable/Disable during PWM Operation

PWM clock P4CK	System clock SYSCLK	PW4CH and PW4CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW4CH or PW4CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.5 PWM4 Control Register 0 (PW4CON0)

	7	6	5	4	3	2	1	0
PW4CON0	P4CLIG	P4STPSEL	P4INI	P4NEG	P4IS1	P4IS0	P4CS1	P4CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A6H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW4CON0 is a special function register (SFR) to control PWM.

Description of Bits

- **P4CS1, P4CS0** (bits 1, 0)
  The P4CS1 and P4CS0 bits are used to select the PWM4 operation clocks. LSCLK, HTBCLK, or the external clock (P44/T0P4CK) can be selected by these bits. The sampling clock of the external input is OSCLK when HTBCLK is selected, or LSCLK otherwise. This setting is also applied to PWM5 in the cooperation mode (P45MD=1).

P4CS1	P4CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	External clock (P44/T0P4CK)
1	1	Prohibited (the PWM circuit does not operate)

- **P4IS1, P4IS0** (bits 3, 2)
  The P4IS1 and P4IS0 bits are used to select the point at which the PWM4 interrupt occurs. “When the periods coincide”, “when the duties coincide”, or “when the periods and duties coincide” can be selected.

P4IS1	P4IS0	Description
0	0	When the periods coincide (Initial value)
0	1	When the duties coincide
1	*	When the periods and duties coincide

- **P4NEG** (bit 4)
  The P4NEG bit is used to select the output logic of PWM4. The initial value of PWM4 output is “1” for the positive logic and “0” for the negative logic.

P4NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P4INI** (bit 5)
  The P4INI bit is used to select the initial value level of the PWM4 output. When P4NEG="1", the initial value level of the PWM4 is also inverted.

P4INI	Description
0	Initial value level of PWM4 output is "H". (initial value)
1	Initial value level of PWM4 output is "L".

- **P4STPSEL** (bit 6)
  The P4STPSEL bit is used to select whether or not to set the PWM4 output level back to its initial level when the PWM4 output is paused by P4RUN="0". The initial value level is selected by P4INI and inverted when P4NEG="1".

P4STPSEL	Description
0	Holds the PWM4 output level when PWM4 is paused. (initial value)
1	Initializes the PWM4 output level when PWM4 is paused.

- **P4CLIG** (bit 7)
  The P4CLIG signal is used to select whether or not to enable the external clear input when the PWM4 output flag (P4FLG) is at the "H" level in the software start or external input clear mode. This setting is also applied to PWM5 in the cooperation mode (P45MD="H").

P4CLIG	Description
0	Enables the external clear input to PWM4 in the software start or external input clear mode. (initial value)
1	Disables the external clear input when the PWM4 output flag ="H" in the software start or external input clear mode.

10.2.6 PWM4 Control Register 1 (PW4CON1)

	7	6	5	4	3	2	1	0
PW4CON1	P4STAT	P4FLG	—	—	—	—	—	P4RUN
R/W	R	R	R	R	R	R	R	R/W
At reset	0	1	0	0	0	0	0	0

Address: 0F8A7H
Access: R/W
Access size: 8 bits
Initial value: 40H

PW4CON1 is a special function register (SFR) to control PWM4.

Description of Bits

- **P4RUN** (bit 0)
  The P4RUN bit is used to control count stop/start of PWM4.

P4RUN	Description
0	Stops counting (Initial value)
1	Starts counting

- **P4FLG** (bit 6)
  The P4FLG bit is used to read the output flag of PWM4.
  This bit is set to “1” when write operation to PW4CH or PW4CL is performed.

P4FLG	Description
0	PWM4 output flag = "0"
1	PWM4 output flag = "1" (initial value)

- **P4STAT** (bit 7)
  The P4STAT bit indicates “counting stopped or “counting in progress” of PWM4.

P4STAT	Description
0	Counting stopped (Initial value)
1	Counting in progress

10.2.7 PWM4 Control Register 2 (PW4CON2)

	7	6	5	4	3	2	1	0
PW4CON2	P45MD	P4MD	—	P4TGSEL	P4STM1	P4STM0	P4TGE1	P4TGE0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8A8H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW4CON1 is a special function register (SFR) to control PWM4.

- **P4TGE1**, **P4TGE0** (bits 1, 0)
  The P4TGE1 and P4TGE0 bits are used to select disable operation, falling-edge operation, rising-edge operation, or both-edge operation when PWM4 is controlled by the external input. This setting is also applied to PWM5 in the cooperation mode (P45MD=1).

P4TGE1	P4TGE0	Description	
		External input start mode enabled (P4STM1,P4STM0 = "01" or "10")	External input clear mode enabled (P4STM1,P4STM0 = "11")
0	0	Disables external input start (initial value)	Disables external input clear (initial value)
0	1	Rising-edge start Falling-edge stop & clear	Falling edge clear
1	0	Falling-edge start Rising-edge stop & clear	Rising-edge clear
1	1	Disables external input start	Both-edge clear

- **P4STM1**, **P4STM0** (bits 3, 2)
  The P4STM1 and P4STM0 bits are used to select the count start mode of PWM4.
  This setting is also applied to PWM5 in the cooperation mode (P45MD=1).

P4STM1	P4STM0	Description
0	0	Software start mode (initial value)
0	1	Software start or external input start mode
1	0	External input start mode
1	1	Software start or external input clear mode

- **P4TGSEL** (bit 4)
  The P4TGSEL bit is used to select the pin used as the hardware control pin. This setting is also applied to PWM5 in the cooperation mode (P45MD=1).

P4TGSEL	Description	
	External input start/external input clear control	Emergency stop control
0	Uses the P00/PW45EV0 pin (initial value)	Uses the P30/PW45EV1 pin (initial value)
1	Uses the P30/PW45EV1 pin	Uses the P00/PW45EV0 pin

- **P4MD** (bit 6)
  The P4MD bit is used to select the one-shot mode or repeat mode for PWM4. When the P4MD bit is set to "1", PWM4 operates in the one-shot mode. This setting is also applied to PWM5 in the cooperation mode (P45MD=1).

P4MD	Description
0	PWM4 repeat mode (initial value)
1	PWM4 one-shot mode

- **P45MD** (bit 7)
  The P45MD bit is used to select the standalone mode or cooperation mode for PWM4 and PWM5. When the P45MD bit is set to "1", PWM4 and PWM5 work together.

P45MD	Description
0	PWM4 and PWM5 standalone mode (initial value)
1	PWM4 and PWM5 cooperation mode

10.2.8 PWM4 Control Register 3 (PW4CON3)

	7	6	5	4	3	2	1	0
PW4CON3	P4SDST	—	—	P4DTMD	—	—	P4SDE1	P4SDE0
R/W	R/W	R	R	R/W	R	R	R/W	R/W
At reset	0	0	0	1	0	0	0	0

Address: 0F8A9H
Access: R/W
Access size: 8 bits
Initial value: 10H

PW4CON1 is a special function register (SFR) to control PWM4.

- **P4SDE1**, **P4SDE0** (bits 1, 0)
  The P4SDE1 and P4SDE0 bits are used to select enable/disable of the emergency stop function and which edge activates the emergency stop.
  The emergency stop function is valid in the cooperation mode (P45MD=1).

P4SDE1	P4SDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

- **P4DTMD** (bit 4)
  The P4DTMD bit is used to select whether or not to use the dead time setting in the cooperation mode (P45MD=1). When the dead time setting is used, it is set in the duty register (PW5D) of PWM5. This function is valid in the cooperation mode (P45MD=1).

P4DTMD	Description
0	Does not use the dead time setting.
1	Uses the dead time setting. (initial value)

- **P4SDST** (bit 7)
  The P4SDST bit indicates that an emergency stop interrupt has occurred.
  Write “1” to this bit to clear it.
  The emergency stop function is valid in the cooperation mode (P45MD=1).

P4SDST	Description
0	No emergency stop interrupt has occurred. (initial value)
1	An emergency stop interrupt has occurred.

10.2.9 PWM5 Period Registers (PW5PL, PW5PH)

Address: 0F8B0H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW5PL	P5P7	P5P6	P5P5	P5P4	P5P3	P5P2	P5P1	P5P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

Address: 0F8B1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW5PH	P5P15	P5P14	P5P13	P5P12	P5P11	P5P10	P5P9	P5P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

PW5PH and PW5PL are special function registers (SFRs) to set the PWM5 periods.
When the dead time setting is used (P4DTMD=1) in the cooperation mode (P45MD=1), the value of the PW5P setting is invalid because the value of the PWM5 period is set in PW4D.

Note:
When PW5PH or PW5PL is set to “0000H”, the PWM5 period buffer (PW5PBUF) is set to “0001H”.
A word type transfer instruction should be used for register setting.

10.2.10 PWM5 Duty Registers (PW5DL, PW5DH)

	7	6	5	4	3	2	1	0
PW5DL	P5D7	P5D6	P5D5	P5D4	P5D3	P5D2	P5D1	P5D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5DH	P5D15	P5D14	P5D13	P5D12	P5D11	P5D10	P5D9	P5D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B3H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW5DH and PW5DL are special function registers (SFRs) to set the duties of PWM5.
When the dead time setting is used (P4DTMD=1) in the cooperation mode (P45MD=1), the PW5D value is used for the dead time setting.

Note:
For PW5DH and PW5DL, set data smaller than for PW5PH and PW5PL.
A word type transfer instruction should be used for register setting.

10.2.11 PWM5 Counter Registers (PW5CH, PW5CL)

	7	6	5	4	3	2	1	0
PW5CL	P5C7	P5C6	P5C5	P5C4	P5C3	P5C2	P5C1	P5C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CH	P5C15	P5C14	P5C13	P5C12	P5C11	P5C10	P5C9	P5C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B5H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW5CL and PW5CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW5CL or PW5CH, it is set to “0000H”. The data that is written is meaningless.
When data is read from PW5CL, the value of PW5CH is latched. When reading PW5CH and PW5CL, use a word type instruction or read PW5CL first.

The contents of PW5CH and PW5CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock.
Table 10-2 shows PW5CH and PW5CL read enable/disable for each combination of the PWM clock and system clock.

Table 10-2 PW5CH and PW5CL Read Enable/Disable during PWM0 Operation

PWM clock P5CK	System clock SYSCLK	PW5CH and PW5CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW5CH or PW5CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.12 PWM5 Control Register 0 (PW5CON0)

	7	6	5	4	3	2	1	0
PW5CON0	P5CLIG	P5STPSEL	P5INI	P5NEG	P5IS1	P5IS0	P5CS1	P5CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B6H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW5CON0 is a special function register (SFR) to control PWM5.

Description of Bits

- **P5CS1, P5CS0** (bits 1, 0)
  The P5CS1 and P5CS0 bits are used to select the PWM5 operation clocks. LSCLK, HTBCLK, or the external clock (P45/T1P5CK) can be selected by these bits. The sampling clock of the external input is OSCLK when HTBCLK is selected, or LSCLK otherwise.

P5CS1	P5CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	External clock (P45/T1P5CK)
1	1	Prohibited (the PWM circuit does not operate)

- **P5IS1, P1IS0** (bits 3, 2)
  The P5IS1 and P5IS0 bits are used to select the point at which the PWM5 interrupt occurs. “When the periods coincide”, “when the duties coincide”, or “when the periods and duties coincide” can be selected.

P5IS1	P5IS0	Description
0	0	When the periods coincide (Initial value)
0	1	When the duties coincide
1	*	When the periods and duties coincide

- **P5NEG** (bit 4)
  The P5NEG bit is used to select the output logic of PWM5. The initial value of PWM5 output is “1” for the positive logic and “0” for the negative logic.

P5NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P5INI** (bit 5)
  The P5INI bit is used to select the initial value level of the PWM5 output. When P5NEG="1", the initial value level of the PWM5 is also inverted.

P5INI	Description
0	Initial value level of PWM5 output is "H". (initial value)
1	Initial value level of PWM5 output is "L".

- **P5STPSEL** (bit 6)
  The P5STPSEL bit is used to select whether or not to set the PWM5 output level back to its initial level when the PWM5 output is paused by P5RUN="0". The initial value level is selected by P5INI and inverted when P5NEG="1". In the cooperation mode, this setting is applied when P4RUN="0".

P5STPSEL	Description
0	Holds the PWM5 output level when PWM5 is paused. (initial value)
1	Initializes the PWM5 output level when PWM5 is paused.

- **P5CLIG** (bit 7)
  The P5CLIG signal is used to select whether or not to enable the external clear input when the PWM5 output flag (P5FLG) is at the "H" level in the software start or external input clear mode. In the cooperation mode (P45MD="H"), this setting is invalid, and the P4CLIG setting is applied.

P5CLIG	Description
0	Enables the external clear input to PWM5 in the software start or external input clear mode. (initial value)
1	Disables the external clear input when the PWM5 output flag = "H" in the software start or external input clear mode.

10.2.13 PWM5 Control Register 1 (PW5CON1)

	7	6	5	4	3	2	1	0
PW5CON1	P5STAT	P5FLG	—	—	—	—	—	P5RUN
R/W	R	R	R	R	R	R	R	R/W
At reset	0	1	0	0	0	0	0	0

Address: 0F8B7H
Access: R/W
Access size: 8 bits
Initial value: 40H

PW5CON1 is a special function register (SFR) to control PWM5.

Description of Bits

- **P5RUN** (bit 0)
  The P5RUN bit is used to control count stop/start of PWM5.

P5RUN	Description
0	Stops counting (Initial value)
1	Starts counting

- **P5FLG** (bit 6)
  The P5FLG bit is used to read the output flag of PWM5.
  This bit is set to “1” when write operation to PW5CH or PW5CL is performed.

P5FLG	Description
0	PWM5 output flag = “0”
1	PWM5 output flag = “1” (initial value)

- **P5STAT** (bit 7)
  The P5STAT bit indicates “counting stopped” or “counting in progress” of PWM5.

P5STAT	Description
0	Counting stopped (Initial value)
1	Counting in progress

10.2.14 PWM5 Control Register 2 (PW5CON2)

	7	6	5	4	3	2	1	0
PW5CON2	—	P5MD	—	P5TGSEL	P5STM1	P5STM0	P5TGE1	P5TGE0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F8B8H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW5CON2 is a special function register (SFR) to control PWM5.

Description of Bits

- **P5TGE1, P5TGE0** (bits 1, 0)
  The P5TGE1 and P5TGE0 bits are used to select disable operation, falling-edge operation, rising-edge operation, or both-edge operation when PWM5 is controlled by the external input. In the cooperation mode (P45MD=1), this setting is invalid.

P5TGE1	P5TGE0	Description	
		External input start mode enabled (P5STM1,P5STM0 = "01" or "10")	External input clear mode enabled (P5STM1,P5STM0 = "11")
0	0	Disables external input start (initial value)	Disables external input clear (initial value)
0	1	Rising-edge start Falling-edge stop & clear	Falling edge clear
1	0	Falling-edge start Rising-edge stop & clear	Rising-edge clear
1	1	Disables external input start	Both-edge clear

- **P5STM1**, **P5STM0** (bits 3, 2)
  The P5STM1 and P5STM0 bits are used to select the count start mode of PWM5.
  In the cooperation mode (P45MD=1), this setting is invalid.

P5STM1	P5STM0	Description
0	0	Software start mode (initial value)
0	1	Software start or external input start mode
1	0	External input start mode
1	1	Software start or external input clear mode

- **P5TGSEL** (bit 4)
  The P5TGSEL bit is used to select the pin used as the external input control pin. In the cooperation mode (P45MD=1), this setting is invalid, and the P4TGSEL setting is applied.

P5TGSEL	Description
	External input start/external input clear control
0	Uses the P00/PW45EV0 pin (initial value)
1	Uses the P30/PW45EV1 pin

- **P5MD** (bit 6)
  The P5MD bit is used to select the one-shot mode or repeat mode for PWM5. When the P5MD bit is set to “1”, PWM5 operates in the one-shot mode. In the cooperation mode (P45MD=1), this setting is invalid, and the P4MD setting is applied.

P5MD	Description
0	PWM5 repeat mode (initial value)
1	PWM5 one-shot mode

10.3 Description of Operation

PWM has the six different operation modes described below.
For details of each operation mode, see Sections 10.3.1 to 10.3.6.

P45MD	**P4DTMD**	**PnMD**	Operation mode	Description
0	—	0	In standalone mode and repeat mode	PWM4 and PWM5 independently and repeatedly work.
	—	1	In standalone mode and one-shot mode	PWM4 and PWM5 independently work and automatically stop after one cycle.
1	0	0	In cooperation mode and repeat mode Does not use the dead time setting	PWM4 and PWM5 repeatedly work together. The duty can be set for PWM4 and PWM5 independently.
		1	In cooperation mode and one-shot mode Does not use the dead time setting	PWM4 and PWM5 work together and automatically stop after one cycle. The duty can be set for PWM4 and PWM5 independently.
	1	0	In cooperation mode and repeat mode Uses the dead time setting	PWM4 and PWM5 repeatedly work together. The dead time is set, and the timing when PWM4 and PWM5 simultaneously turn off can be generated.
		1	In cooperation mode and one-shot mode Uses the dead time setting	PWM4 and PWM5 work together and automatically stop after one cycle. The dead time is set, and the timing when PWM4 and PWM5 simultaneously turn off can be generated.

n=4, 5

There are the following 11 modes for start/stop/clear control of PWM.
For hardware control, the PnTGSEL bit allows selection of the external input for control from P00/PW45EV0 and P30/PW45EV1.
For details of each operation mode, see Section 10.3.7.

PnSTM1	PnSTM0	PnTGE1	PnTGE0	Operation mode	Description
0	0	—	—	Software start mode	The PnRUN bit control is used for start/stop.
0	1	0	1	Software start or External input start mode	The PnRUN bit control is used for start/stop. In addition, the "H" level of the selected external input can be used for start, and "L" level stop or counter clear.
		1	0		The PnRUN bit control is used for start/stop. In addition, the "L" level of the selected external input can be used for start, and "H" level stop or counter clear.
		0	0		The PnRUN bit control is used for start/stop. The external input control is invalid.
		1	1		
1	0	0	1	External input start mode	Rising edge of the selected external input can be used for start, and falling edge for stop and counter clear.
		1	0		Falling edge of the selected external input can be used for start, and rising edge for stop and counter clear.
		0	0		The external input control is invalid and PWM does not operate.
		1	1		
1	1	0	0	Software start or External input clear mode	The PnRUN bit control is used for start/stop. The external input control is invalid.
		0	1		The PnRUN bit control is used for start/stop. In addition, falling edge of the selected external input can be used for counter clear.
		1	0		The PnRUN bit control is used for start/stop. In addition, rising edge of the selected external input can be used for counter clear.
		1	1		The PnRUN bit control is used for start/stop. In addition, rising or falling edge of the selected external input can be used for counter clear.

n=4, 5

10.3.1 Repeat Mode with PWM4 and PWM5 Standalone Mode (P45MD="0", PnMD="0")

When the PnRUN bit of the PWMn control register 1 (PWnCON1) is set to "1", the PWM counters (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that is selected by the PWMn control register 0 (PWnCON0) and increment the count value on the second falling edge.

When the count value of the PWnCH and PWnCL counter registers coincides the value of the PWMn duty buffer (PWnDBUF), the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of the PWnCH and PWnCL counter registers and the value of the PWMn period buffer (PWnPBUF) coincide, the PnFLG becomes "1" at the next PnCK falling edge, and the PWnCH and PWnCL are reset to "0000H" to continue counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the PnRUN bit is set to "0", the PWnCH and PWnCL counter registers stop counting after counting once the falling of the PWM clock (PnCK). To confirm that PWnCH and PWnCL are stopped, check that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, the PWnCH and PWnCL counter registers restart incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWnCH and PWnCL counter registers to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWMn occurs, and the logic of the PWM output are selected by the PWMn control register 0 (PWnCON0).

When the external input control is enabled by PnSTM1 and PnSTM0 of the PWMn control register 2 (PWnCON2), the PWnCH, PWnCL, and PWMn outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the PnTGE0 and PnTGE1 bits of the PWMn control register 2 (PWnCON2), and the pin for the external input control is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency selected by the PWMn control register 0 (PWnCON0)

n=4, 5

After the PnRUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. Subsequent PWM interrupt periods are constant.
Figure 10-2 shows the operation timing diagram of PWMn in the repeat mode with the PWM4 and PWM5 standalone mode (P45MD=“0”, PnMD=“0”).

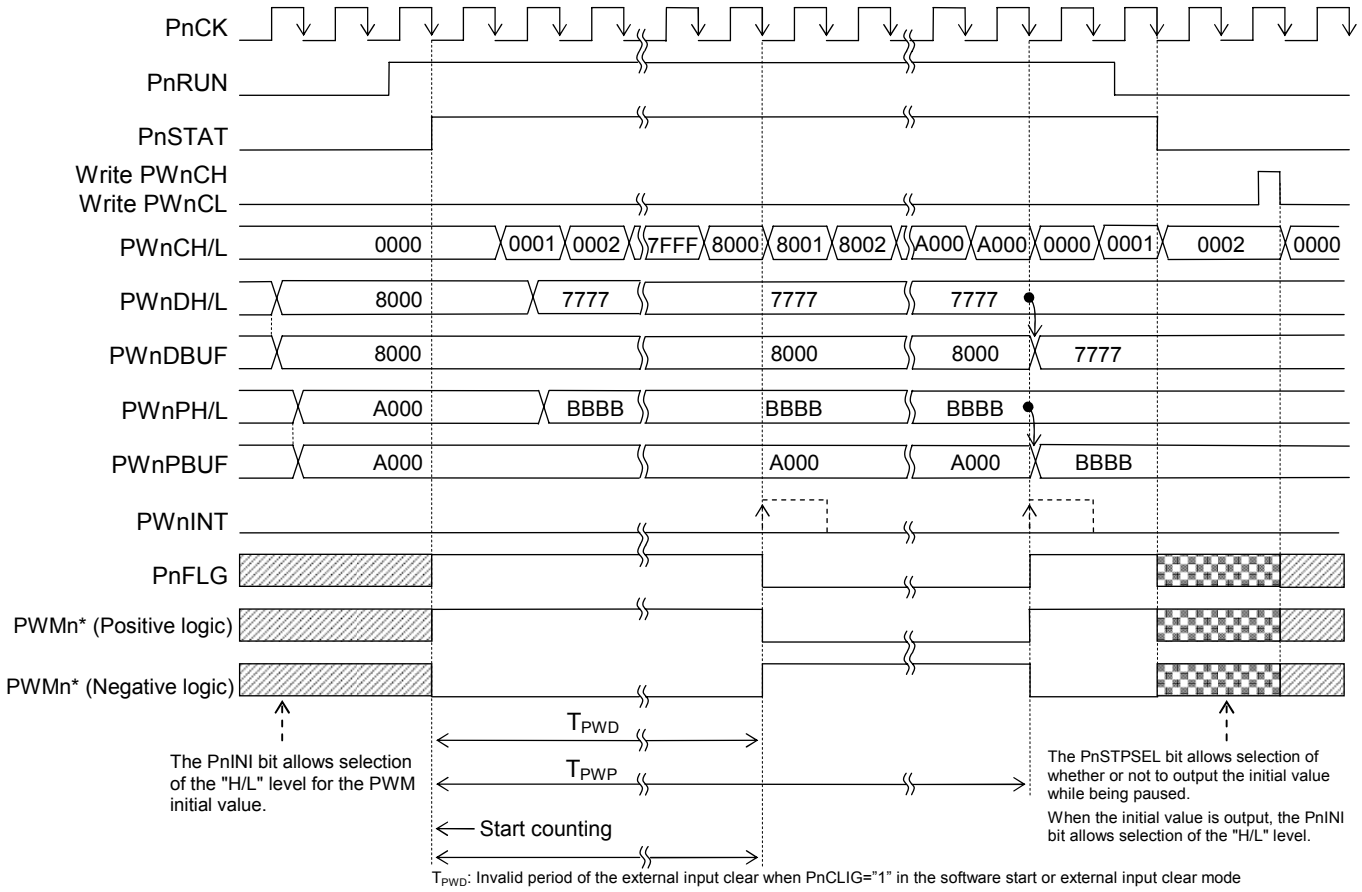


Figure 10-2 (1/2) Operation Timing Diagram of PWM4 (PnMD=“0”, P45MD=“0”)

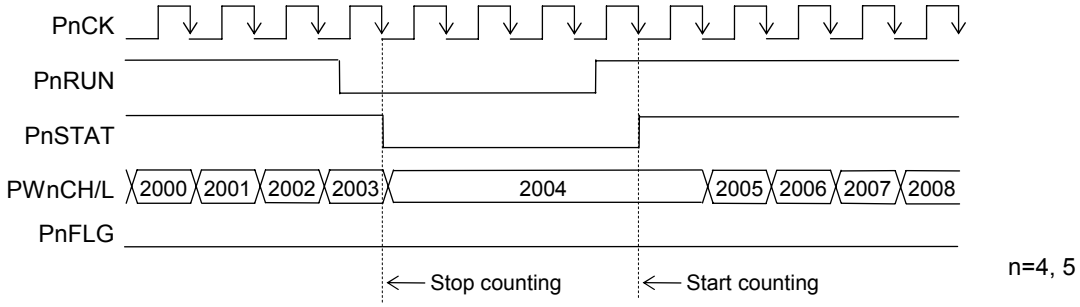


Figure 10-2 (2/2) Operation Timing Diagram of PWMn

Note:
Even if “0” is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a “1” state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

10.3.2 One-shot Mode with PWM4 and PWM5 Standalone Mode (P45MD="0", PnMD="1")

When the PnRUN bit of the PWMn control register 1 (PWnCON1) is set to "1", the PWM counters (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that is selected by the PWMn control register 0 (PWnCON0) and increment the count value on the second falling edge.

When the count value of the PWnCH and PWnCL counter registers coincides the value of the PWMn duty buffer (PWnDBUF), the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of the PWnCH and PWnCL counter registers and the value of the PWMn period buffer (PWnPBUF) coincide, the PnFLG becomes "1" at the next PnCK falling edge, and the PWnCH and PWnCL are reset to "0000H" to stop counting and the PnRUN bit is cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).
When the PnRUN bit is set to "1" again, the PWM counter is resumed.

When the PnRUN bit is set to "0" during counter operation, the PWnCH and PWnCL counter registers stop counting after counting once the falling of the PWM clock (PnCK). To confirm that PWnCH and PWnCL are stopped, check that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, the PWnCH and PWnCL counter registers restart incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWnCH and PWnCL counter registers to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWMn occurs, and the logic of the PWM output are selected by the PWMn control register 0 (PWnCON0).

When the external input control is enabled by PnSTM1 and PnSTM0 of the PWMn control register 2 (PWnCON2), the PWnCH, PWnCL, and PWMn outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the PnTGE0 and PnTGE1 bits of the PWMn control register 2 (PWnCON2), and the pin for the external input control is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency selected by the PWMn control register 0 (PWnCON0)

n=4, 5

After the PnRUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued.
Figure 10-3 shows the operation timing diagram of PWMn in the one-shot mode with the PWM4 and PWM5 standalone mode (P45MD=“0”, PnMD=”1”).

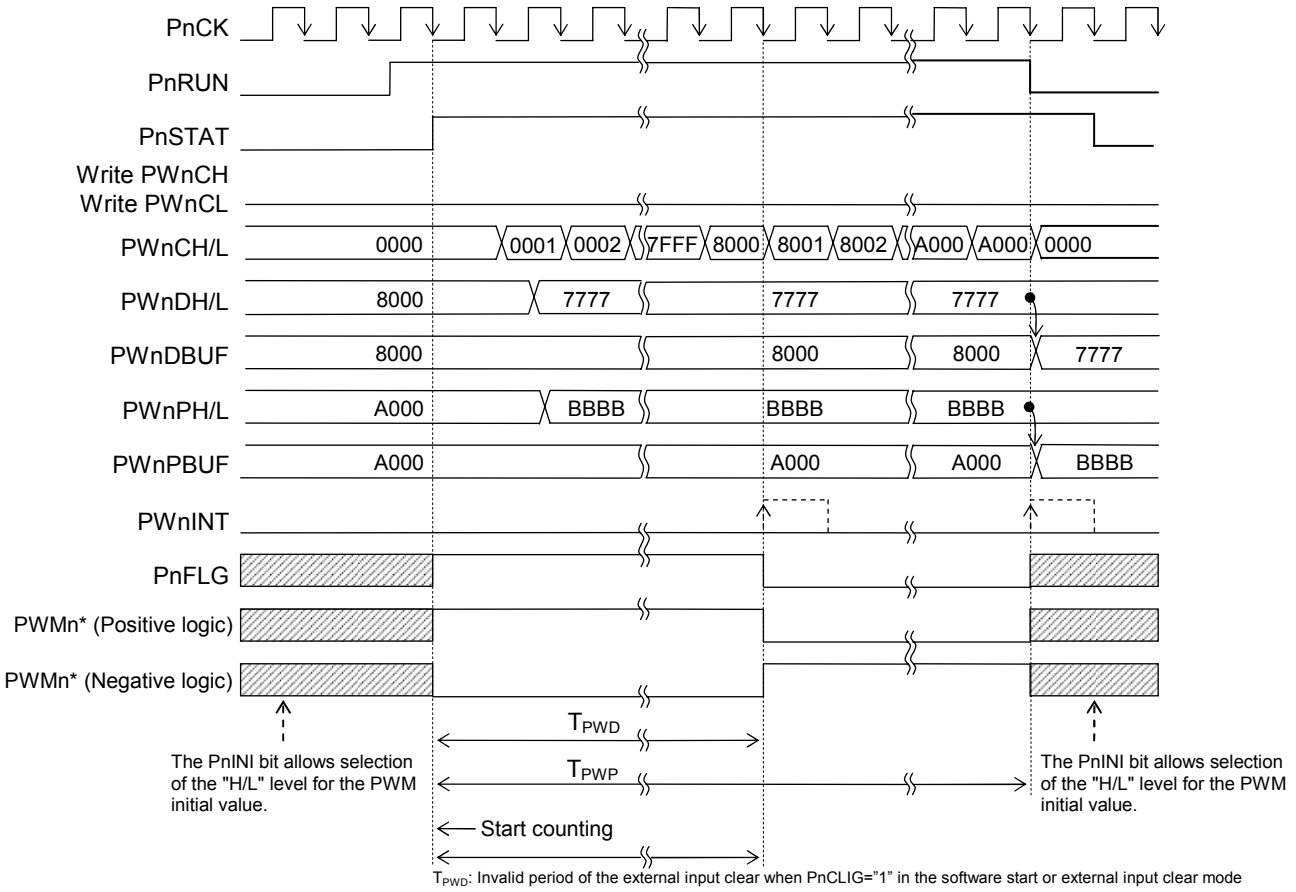


Figure 10-3 (1/2) Operation Timing Diagram of PWM4 (PnMD=“1”, P45MD=“0”)

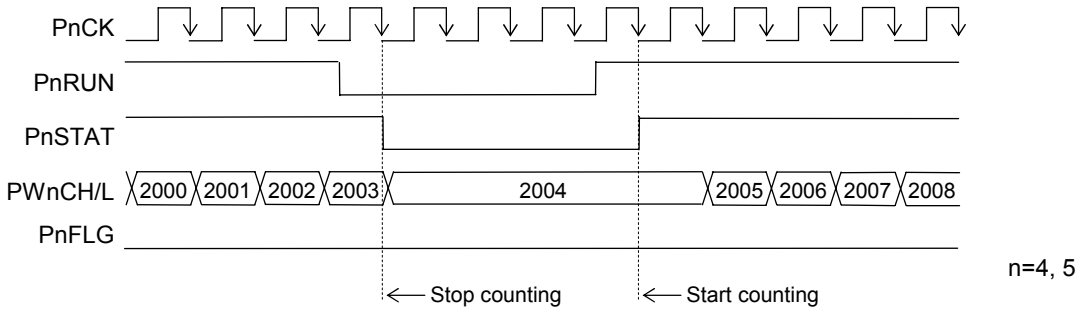


Figure 10-3 (2/2) Operation Timing Diagram of PWMn

Note:
Even if “0” is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a “1” state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

10.3.3 Repeat Mode with PWM4 and PWM5 Cooperation Mode (Dead Time Setting Is Not Used) (P45MD="1", P4DTMD="0", P4MD="0")

When the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1", the PWM counters (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that is selected by the PWM4 control register 0 (PW4CON0) and increment the count value on the second falling edge.

When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next falling edge of P4CK. When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 period buffer (PW5PBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 period buffer (PW4PBUF) coincide, P4FLG is set to "1" on the next falling edge of P4CK, and the PW4CH and PW4CL are reset to "0000H" to continue counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P4RUN bit is set to "0", the PW4CH and PW4CL counter registers stop counting after counting once the falling of the PWM clock (P4CK). To confirm that PW4CH and PW4CL are stopped, check that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, the PW4CH and PW4CL counter registers restart incremental counting from the previous value on the falling edge of P4CK.

To initialize the PW4CH and PW4CL counter registers to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWM4 occurs, and the logic of the PWM4 output are selected by the PWM4 control register 0 (PW4CON0). The logic of the PWM5 output is selected by the PWM5 control register 0 (PW5CON0).

When the external input control is enabled by P4STM1 and P4STM0 of the PWM4 control register 2 (PW4CON2), the PW4CH, PW4CL, PWM4, and PWM5 outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the P4TGE0 and P4TGE1 bits of the PWM4 control register 2 (PW4CON2), and the pin for the external input control is selected by the P4TGSEL bit of the PWM4 control register 2 (PW4CON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWM4 signal (T_{PWP}), the first half duration of the duty (T_{PWD}), the delay1 period (T_{PWD1}), and delay2 period (T_{PWD2}) of the PWM5 signal are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW5P + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency selected by the PWM4 control register 0 (PW4CON0)
PW5P: PWM5 period registers (PW5PH, PW5PL) setting value (0001H to 0FFFFH)
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. Subsequent PWM interrupt periods are constant.
Figure 10-4 shows the operation timing diagram of PWM4 and PWM5 in the repeat mode with the PWM4 and PWM5 cooperation mode (P45MD=“1”) and without the dead time setting (P4DTMD=“0”).

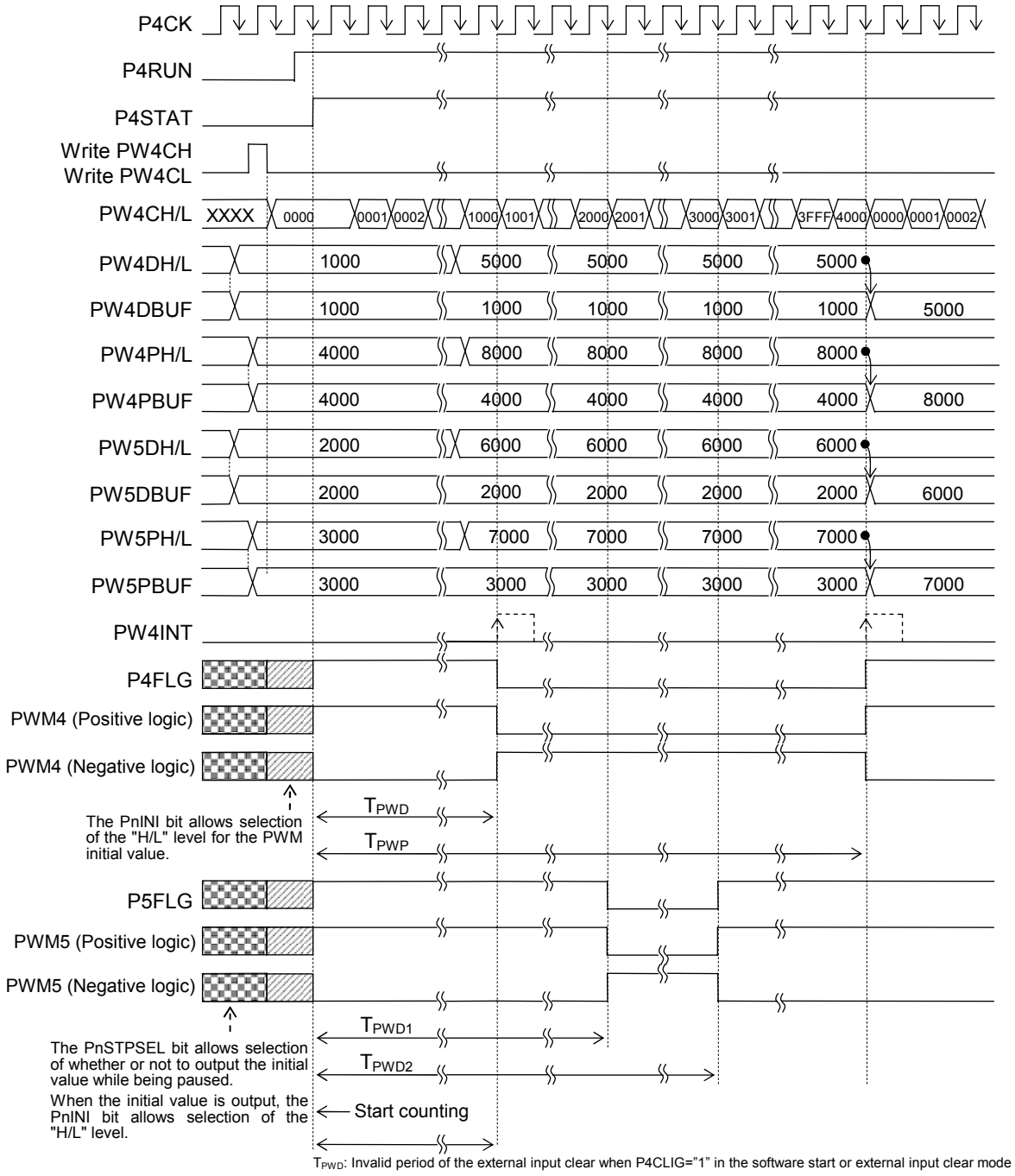


Figure 10-4 Operation Timing Diagram of PWM4 and PWM5 (P4MD=“0”, P45MD=“1”, P4DTMD=“0”)

10.3.4 One-shot Mode with PWM4 and PWM5 Cooperation Mode (Dead Time Setting Is Not Used) (P45MD="1", P4DTMD="0", P4MD="1")

When the P0RUN bit of PWM4 control register 1 (PW4CON1) is set to "1", the PWM counters (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that is selected by the PWM4 control register 0 (PW4CON0) and increment the count value on the second falling edge.

When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next falling edge of P4CK. When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 period buffer (PW5PBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 period buffer (PW4PBUF) coincide, the P4FLG becomes "1" at the next P4CK falling edge, and the PW4CH and PW4CL are reset to "0000H" to stop counting and the P4RUN bit is cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).
When the P4RUN bit is set to "1" again, the PWM counter is resumed.

When the P4RUN bit is set to "0" during counter operation, the PW4CH and PW4CL counter registers stop counting after counting once the falling of the PWM clock (P4CK). To confirm that PW4CH and PW4CL are stopped, check that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, the PW4CH and PW4CL counter registers restart incremental counting from the previous value on the falling edge of P4CK.

To initialize the PW4CH and PW4CL counter registers to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWM4 occurs, and the logic of the PWM output are selected by the PWM4 control register 0 (PW4CON0).

When the external input control is enabled by P4STM1 and P4STM0 of the PWM4 control register 2 (PW4CON2), the PW4CH, PW4CL, PWM4, and PWM5 outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the P4TGE0 and P4TGE1 bits of the PWM4 control register 2 (PW4CON2), and the pin for the external input control is selected by the P4TGSEL bit of the PWM4 control register 2 (PW4CON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWM4 signal (T_{PWP}), the first half duration of the duty (T_{PWD}), the delay1 period (T_{PWD1}), and delay2 period (T_{PWD2}) of the PWM5 signal are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW5P + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency selected by the PWM4 control register 0 (PW4CON0)
PW5P: PWM5 period registers (PW5PH, PW5PL) setting value (0001H to 0FFFFH)
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. Subsequent PWM interrupt periods are constant.
Figure 10-5 shows the operation timing diagram of PWM4 and PWM5 in the one-shot mode with the PWM4 and PWM5 cooperation mode (P45MD=“1”) and without the dead time setting (P4DTMD=“0”).

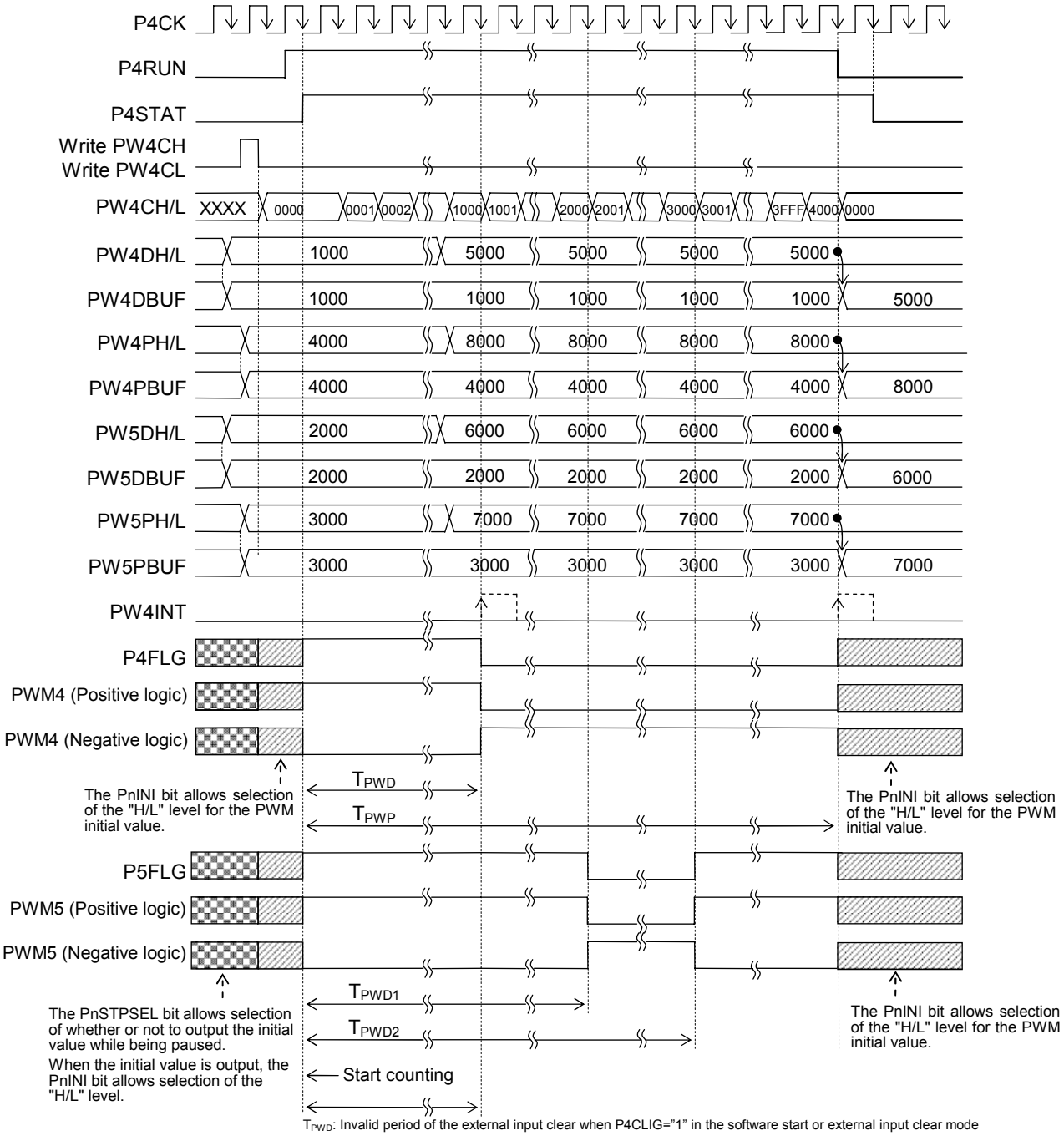


Figure 10-5 Operation Timing Diagram of PWM4 and PWM5 (P4MD=“1”, P45MD=“1”, P4DTMD=“0”)

10.3.5 Repeat Mode with PWM4 and PWM5 Cooperation Mode (Dead Time Setting Is Used) (P45MD="1", P4DTMD="1", P4MD="0")

When the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1", the PWM counters (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that is selected by the PWM4 control register 0 (PW4CON0) and increment the count value on the second falling edge.

When the P4DTMD bit is set to "1", the dead time setting is enabled to forcibly generate the timing when PWM4 and PWM5 simultaneously turn off. The dead time value is set by PW5DH and PW5DL.

When the count value of the PW4CH and PW4CL counter registers and the value of [PWM4 duty buffer]+[Dead time value] (PW4DBUF+PW5DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next falling edge of P4CK. When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 period buffer (PW4PBUF) coincide, P4FLG is set to "1" on the next falling edge of P4CK, and the PW4CH and PW4CL are reset to "0000H" to continue counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P4RUN bit is set to "0", the PW4CH and PW4CL counter registers stop counting after counting once the falling of the PWM clock (P4CK). To confirm that PW4CH and PW4CL are stopped, check that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, the PW4CH and PW4CL counter registers restart incremental counting from the previous value on the falling edge of P4CK.

To initialize the PW4CH and PW4CL counter registers to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWM4 occurs, and the logic of the PWM4 output are selected by the PWM4 control register 0 (PW4CON0). The logic of the PWM5 output is selected by the PWM5 control register 0 (PW5CON0).

When the external input control is enabled by P4STM1 and P4STM0 of the PWM4 control register 2 (PW4CON2), the PW4CH, PW4CL, PWM4, and PWM5 outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the P4TGE0 and P4TGE1 bits of the PWM4 control register 2 (PW4CON2), and the pin for the external input control is selected by the P4TGSEL bit of the PWM4 control register 2 (PW4CON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWM4 signal (T_{PWP}), the first half duration of the duty (T_{PWD}), the dead time (T_{DTM}), and delay2 period (T_{PWD2}) of the PWM5 signal are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D+PW5D + 2}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{DTM} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency selected by the PWM4 control register 0 (PW4CON0)
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. Subsequent PWM interrupt periods are constant.
Figure 10-6 shows the operation timing diagram of PWM4 and PWM5 in the repeat mode with the PWM4 and PWM5 cooperation mode (P45MD=“1”) and the dead time setting (P4DTMD=“1”).

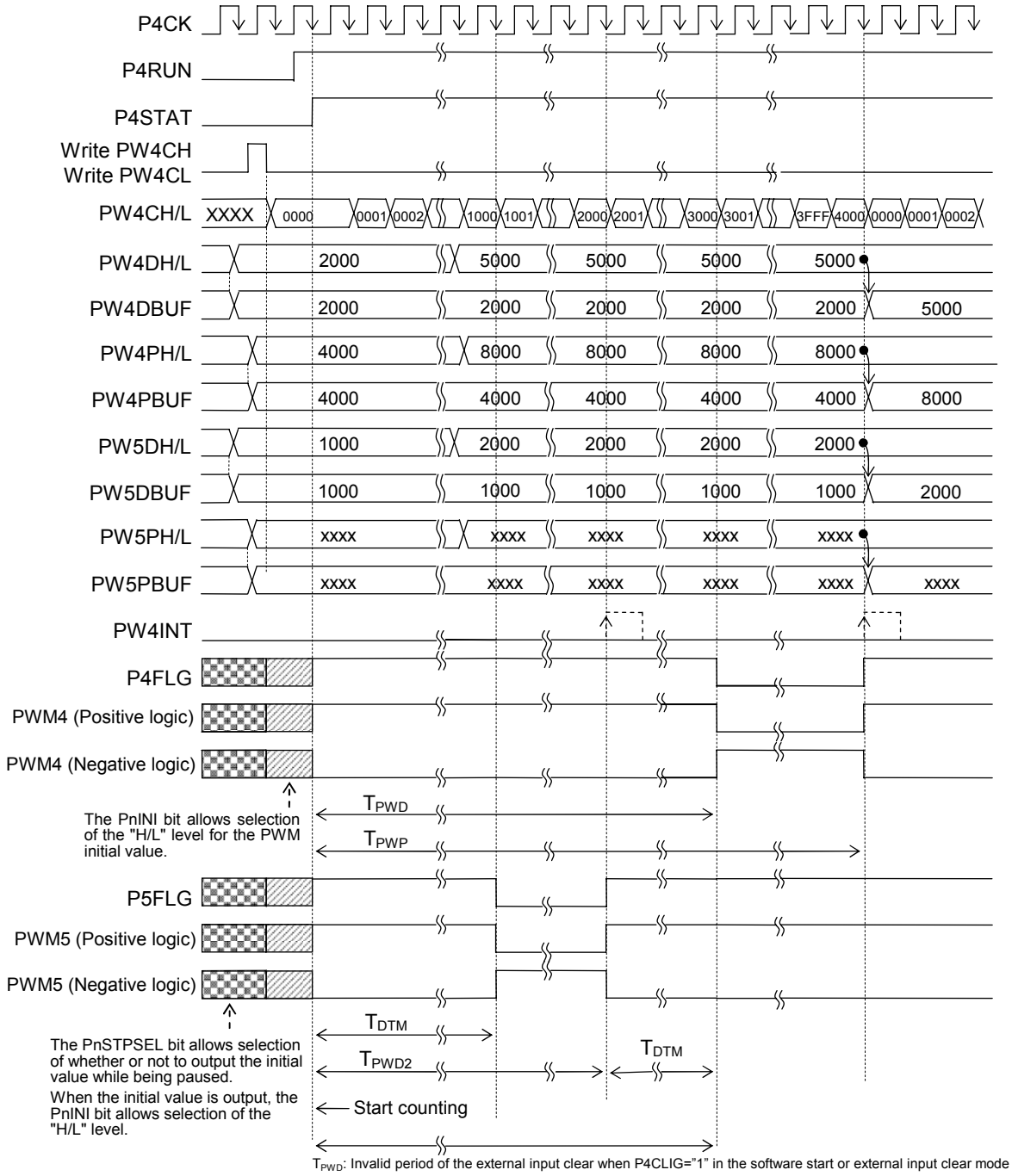


Figure 10-6 Operation Timing Diagram of PWM4 and PWM5 (P4MD=“0”, P45MD=“1”, P4DTMD=“1”)

Note:
When the PWM4 output is assigned to P34 (Port 3) or P43 (Port 4) as the tertiary function or the PWM5 output (PWM5) is assigned to P35 (Port 3) or P47 (Port 4) as the tertiary function, it is a high-impedance output until the output state is set by the port n control registers 0, 1 (PnCON0, PnCON1). When it is necessary to fix in the initial state, use a pull-up or pull-down resistor outside of the LSI.

10.3.6 One-shot Mode with PWM4 and PWM5 Cooperation Mode (Dead Time Setting Is Used) (P45MD="1", P4DTMD="1", P4MD="1")

When the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1", the PWM counters (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that is selected by the PWM4 control register 0 (PW4CON0) and increment the count value on the second falling edge.

When the P4DTMD bit is set to "1", the dead time setting is enabled to forcibly generate the timing when PWM4 and PWM5 simultaneously turn off. The dead time value is set by PW5DH and PW5DL.

When the count value of the PW4CH and PW4CL counter registers and the value of [PWM4 duty buffer]+[Dead time value] (PW4DBUF+PW5DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next falling edge of P4CK. When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 period buffer (PW4DBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of the PW4CH and PW4CL counter registers and the value of the PWM4 period buffer (PW4PBUF) coincide, the P4FLG becomes "1" at the next P4CK falling edge, and the PW4CH and PW4CL are reset to "0000H" to stop counting and the P4RUN bit is cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).
When the P4RUN bit is set to "1" again, the PWM counter is resumed.

When the P4RUN bit is set to "0" during counter operation, the PW4CH and PW4CL counter registers stop counting after counting once the falling of the PWM clock (P4CK). To confirm that PW4CH and PW4CL are stopped, check that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, the PW4CH and PW4CL counter registers restart incremental counting from the previous value on the falling edge of P4CK.

To initialize the PW4CH and PW4CL counter registers to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock, the point at which an interrupt of PWM4 occurs, and the logic of the PWM4 output are selected by the PWM4 control register 0 (PW4CON0). The logic of the PWM5 output is selected by the PWM5 control register 0 (PW5CON0).

When the external input control is enabled by P4STM1 and P4STM0 of the PWM4 control register 2 (PW4CON2), the PW4CH, PW4CL, PWM4, and PWM5 outputs can be started, stopped, and cleared. The edge and level for the external input control are selected by the P4TGE0 and P4TGE1 bits of the PWM4 control register 2 (PW4CON2), and the pin for the external input control is selected by the P4TGSEL bit of the PWM4 control register 2 (PW4CON2).
For transfer timing from the PWMn duty registers (PWnDH, PWnDL) to the PWMn duty buffer (PWnDBUF) and from the PWMn period registers (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF) during the external input control, see Section 10.3.7, "Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control". It also describes the restrictions for each mode.

The period of the PWM4 signal (T_{PWP}), the first half duration of the duty (T_{PWD}), the dead time (T_{DTM}), and delay2 period (T_{PWD2}) of the PWM5 signal are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D+PW5D + 2}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{DTM} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency selected by the PWM4 control register 0 (PW4CON0)
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to “1”, counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. Subsequent PWM interrupt periods are constant.
Figure 10-7 shows the operation timing diagram of PWM4 and PWM5 in the one-shot mode with the PWM4 and PWM5 cooperation mode (P45MD=“1”) and the dead time setting (P4DTMD=“1”).

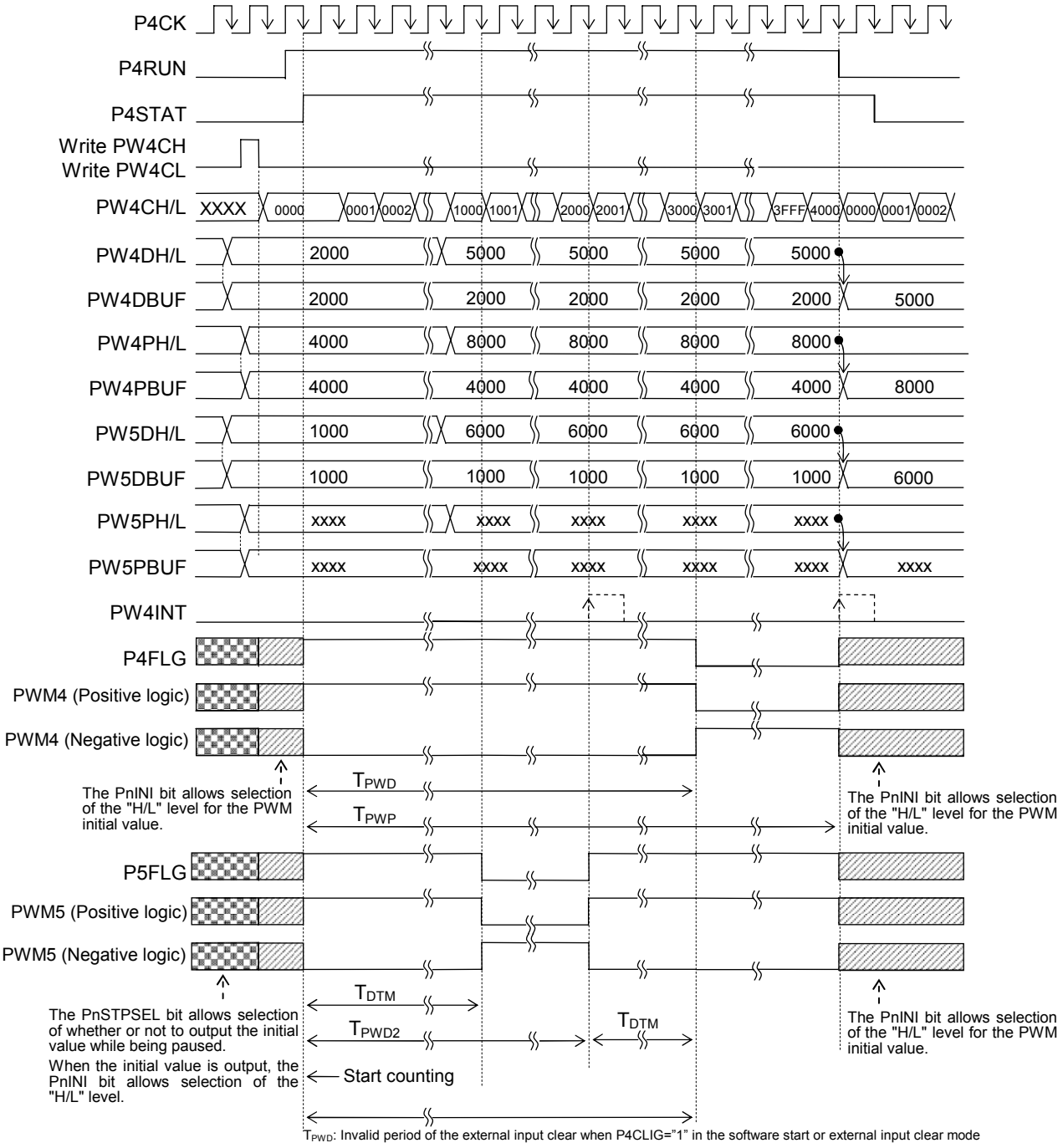
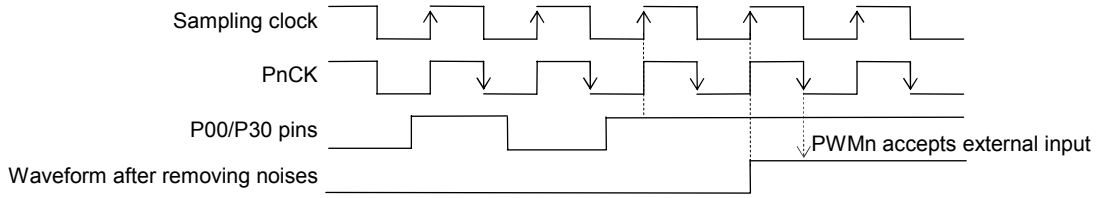


Figure 10-7 Operation Timing Diagram of PWM4 and PWM5 (P4MD=“1”, P45MD=“1”, P4DTMD=“1”)

Note:
When the PWM4 output is assigned to P34 (Port 3) or P43 (Port 4) as the tertiary function or the PWM5 output (PWM5) is assigned to P35 (Port 3) or P47 (Port 4) as the tertiary function, it is a high-impedance output until the output state is set by the port n control registers 0, 1 (PnCON0, PnCON1). When it is necessary to fix in the initial state, use a pull-up or pull-down resistor outside of the LSI.

10.3.7 Start, Stop, and Clear Operations of PWM4 and PWM5 by External Input Control

Setting the PnSTM1 and PnSTM0 bits of the PWMn control register 2 (PWnCON2) enables the start/stop/clear control of the PWM counters (PWnCH and PWnCL) using the external input (P00/PW45EV0 or P30/PW45EV1 port) that is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2). From the external input, pulses shorter than one sampling clock are removed as noises. The sampling clock is OSCLK (approx. 125 ns) when HTBCLK is selected by the PnCS1 and PnCS0 bits, or LSCLK (approx. 32 kHz) otherwise.



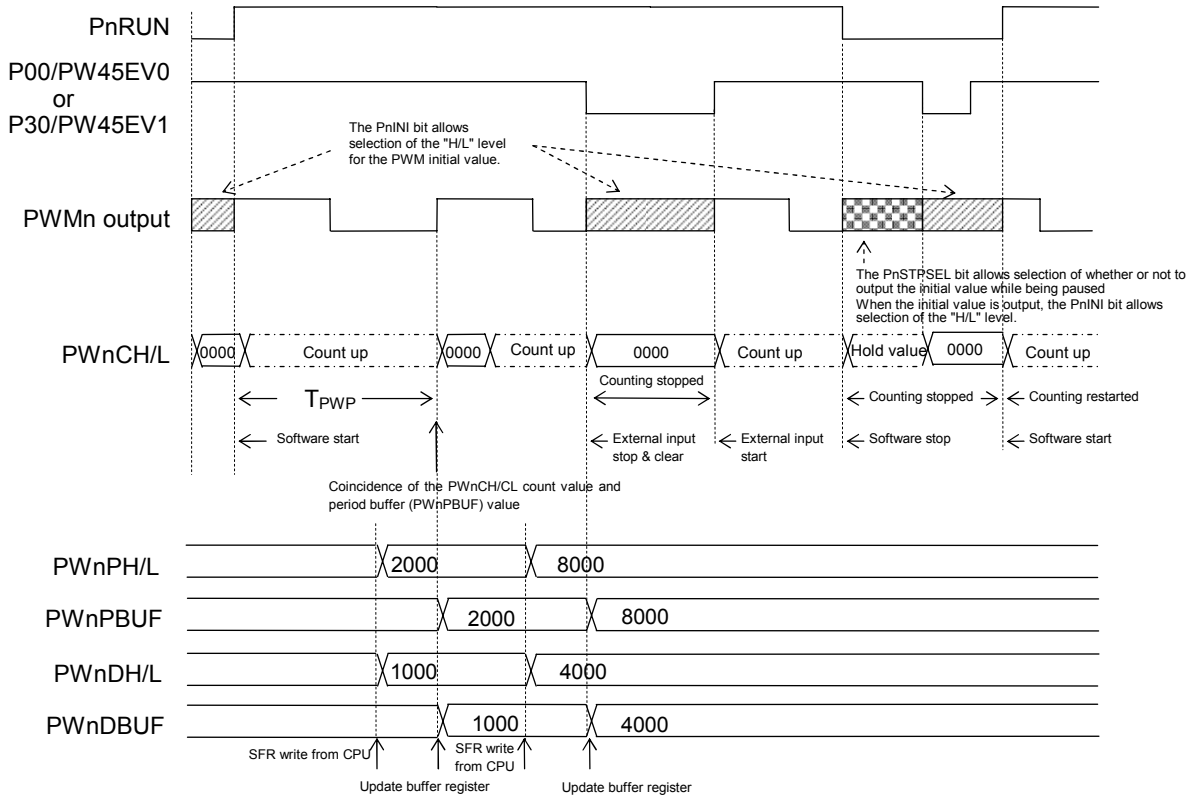
10.3.7.1 Software Start Mode

With the setting of PnSTM1="0" and PnSTM0="0", the PWM counter operates being controlled by the PnRUN bit only. The operation timing is similar to the ones shown in 10.3.1 to 10.3.6.

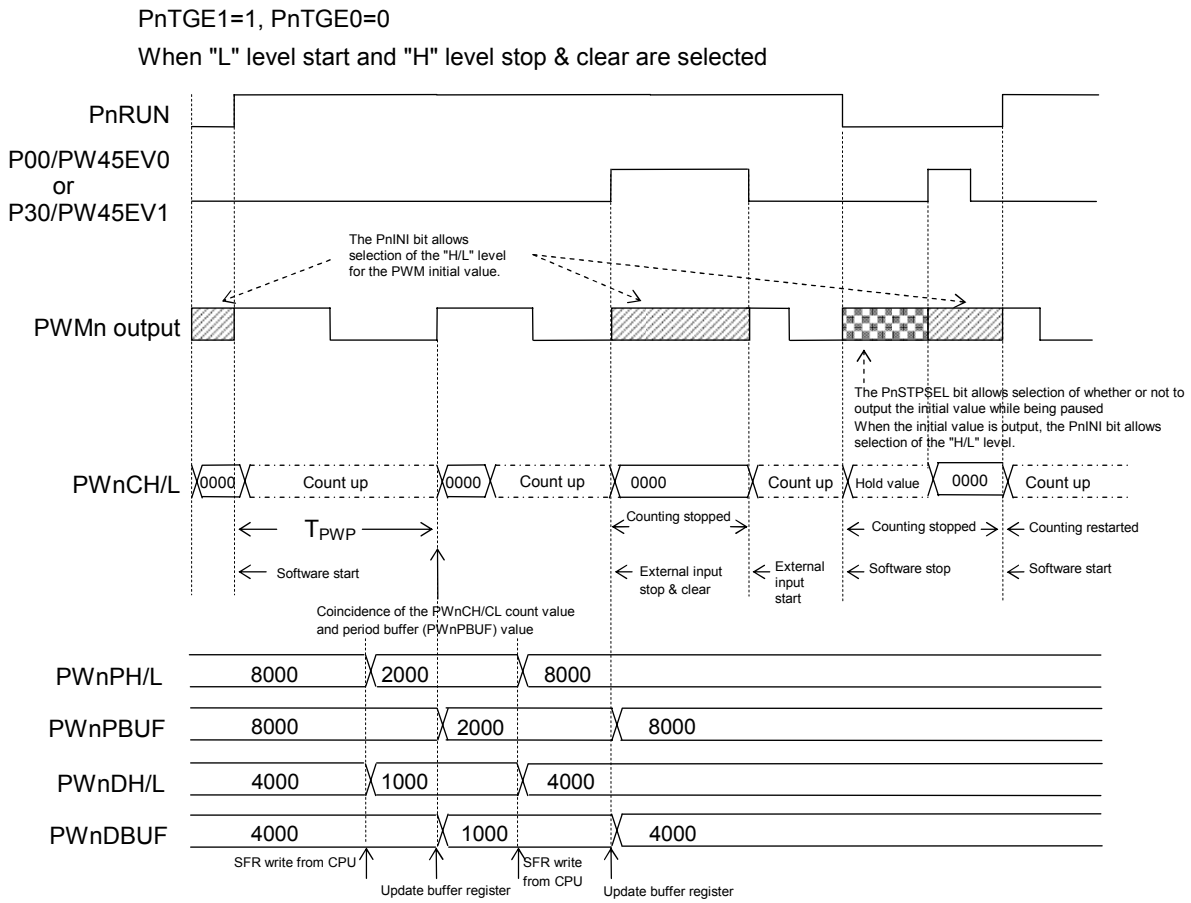
10.3.7.2 Software Start or External Input Start Mode

With the setting of PnSTM1="0" and PnSTM0="1", the PWM counter operates being controlled by the level of the external input (P00/PW45EV0 or P30/PW45EV1 pin) that is selected by the PnRUN and PnTGSEL bits.
When the selected external input gets an external input specified by PnTGE1 and PnTGE0, the PWM counter is started, stopped, or cleared. When the selected external input is fixed at the start level, the counter operates in the same way as the software start.
However, when the selected external input is at the count stop level on the software start, the counter does not start, and it starts counting when the selected external input becomes the start level.
Figure 10-8 shows the operation timing.

PnTGE1=0, PnTGE0=1
When "H" level start and "L" level stop & clear are selected



(a) Operation Timing Diagram with Software Start or External Input Start



(b) Operation Timing Diagram with Software Start or External Input Start

Figure 10-8 Operation Timing Diagram with Software Start or External Input Start (PnSTM1="0", PnSTM0="1")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

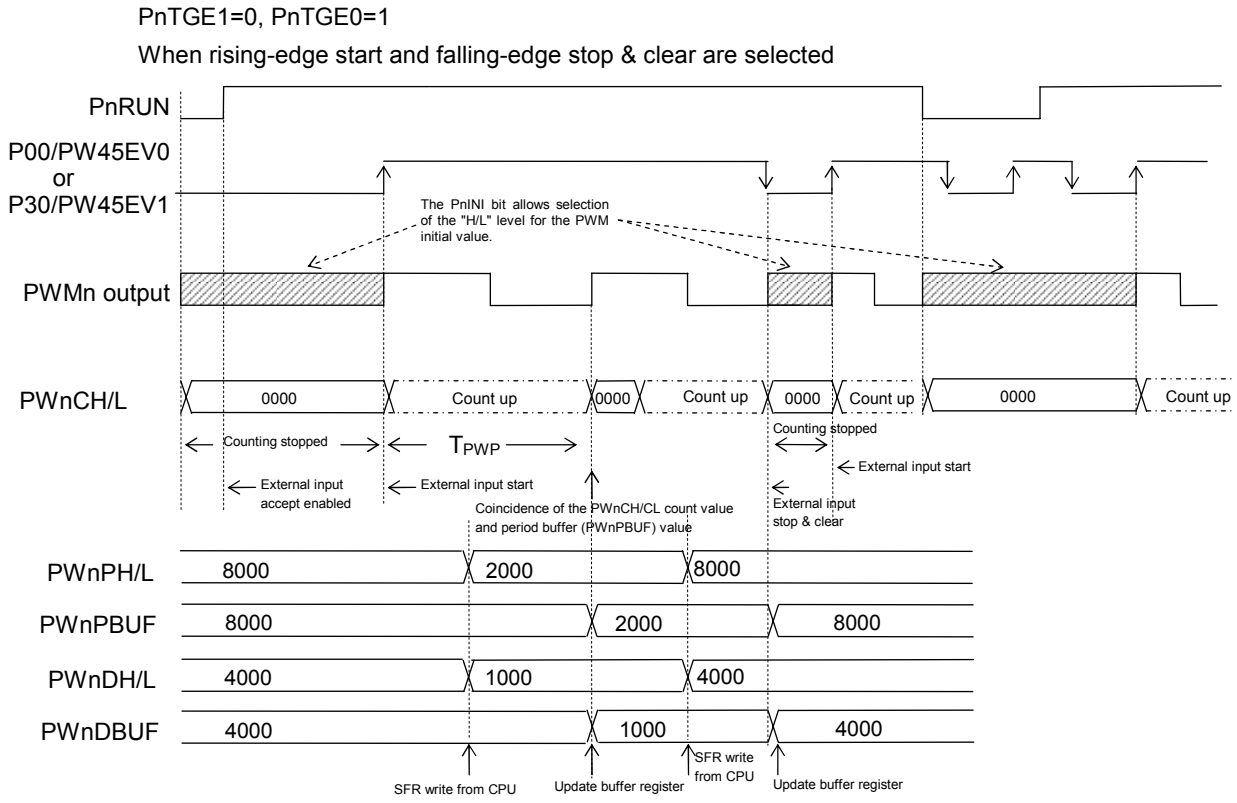
PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

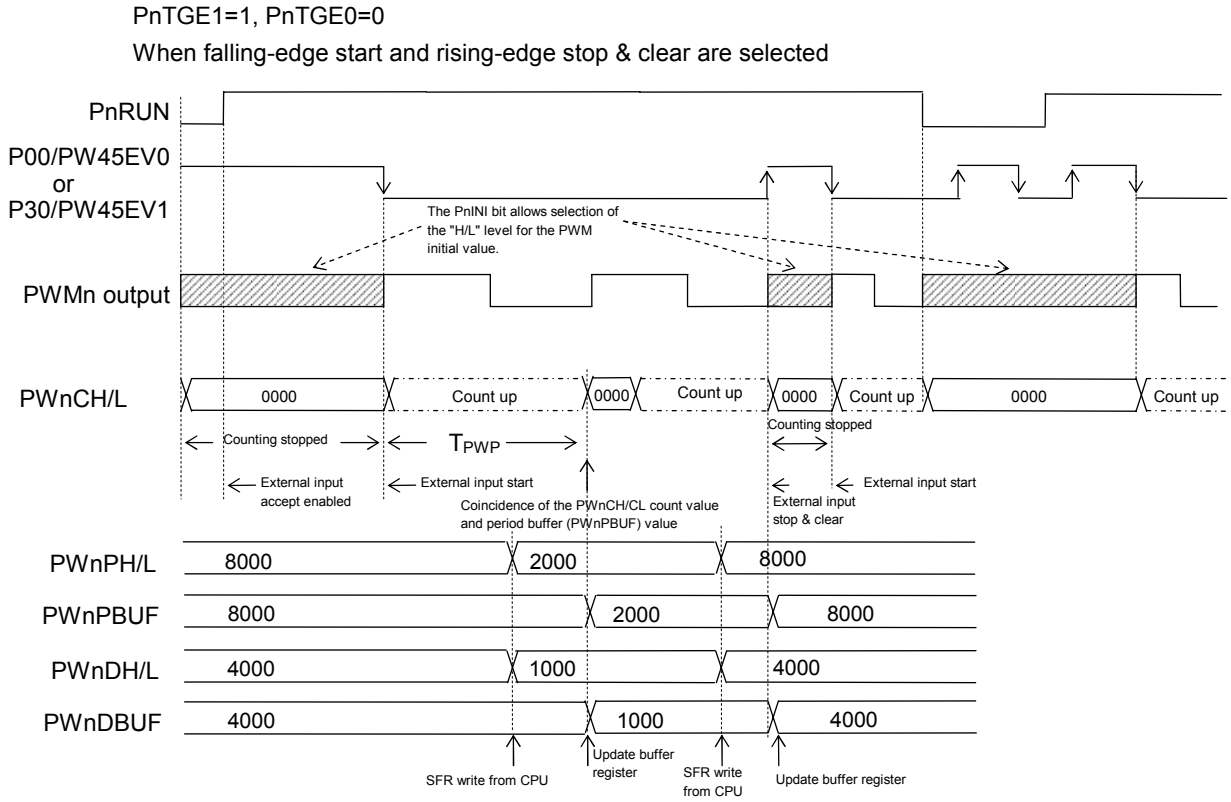
③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

10.3.7.3 External Input Start Mode

With the setting of PnSTM1="1" and PnSTM0="0" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the edge of the external input (P00/PW45EV0 or P30/PW45EV1 port) that is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2).
Note that the PnRUN bit is set to "1" in advance. If the PnRUN bit is "0", PWM will not operates even when the edge input occurs on the selected external input.
Figure 10-9 shows the operation timing.



(a) Operation Timing Diagram with External Input Start



(b) Operation Timing Diagram with External Input Start

Figure 10-9 Operation Timing Diagram with External Input Start (PnSTM1="1", PnSTM0="0")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

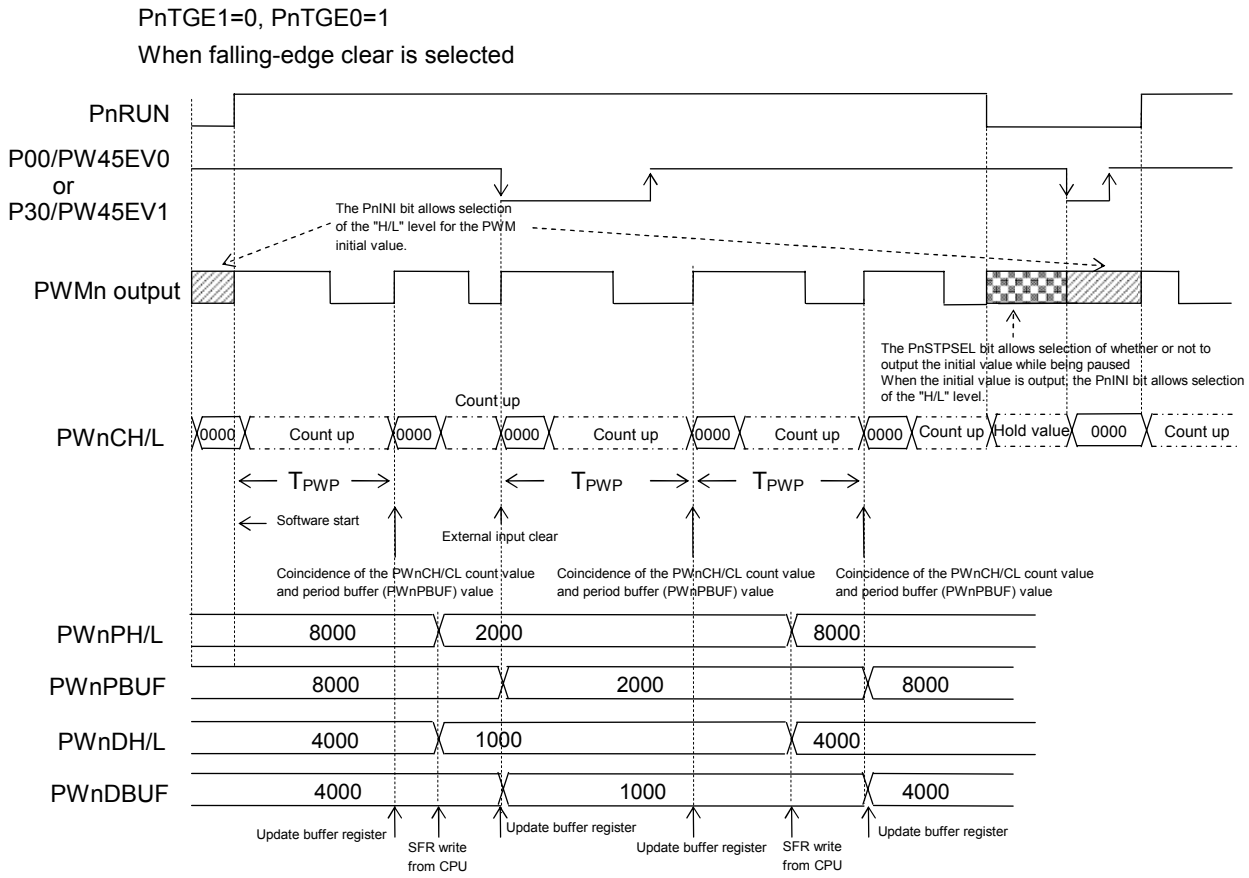
PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

10.3.7.4 Software Start or External Input Clear Mode

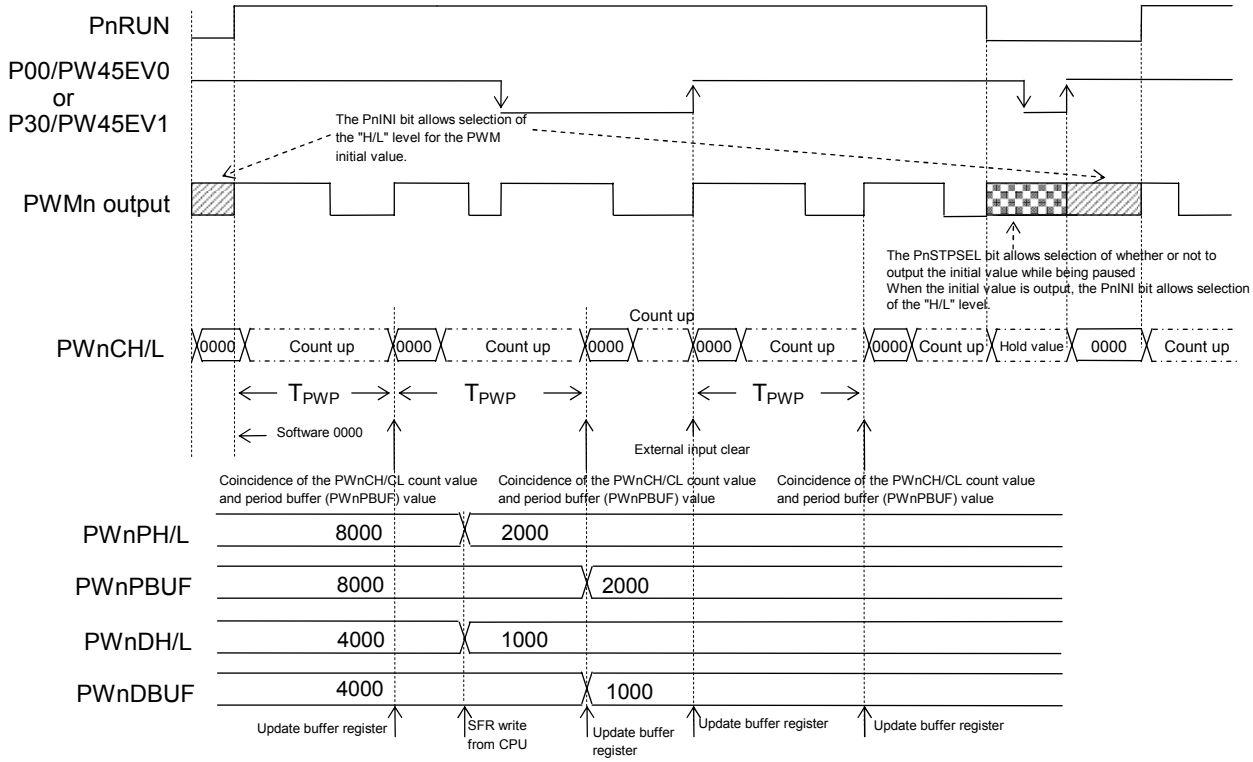
With the setting of PnSTM1="1" and PnSTM0="1" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the PnRUN bit.
When there is no edge input on the external input (P00/PW45EV0 or P30/PW45EV1 pin) selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2), the counter operates in the same way as the software start. When the selected external input (P00/PW45EV0 or P30/PW45EV1 pin) gets an edge input specified by PnTGE1 and PnTGE0, the PWM counter is cleared. The PnCLIG bit of the PWMn control register 0 (PWnCON0) allows enable/disable of the external clear input at the "H" level of the PWMn output flag (PnFLG).
Figure 10-10 shows the operation timing.



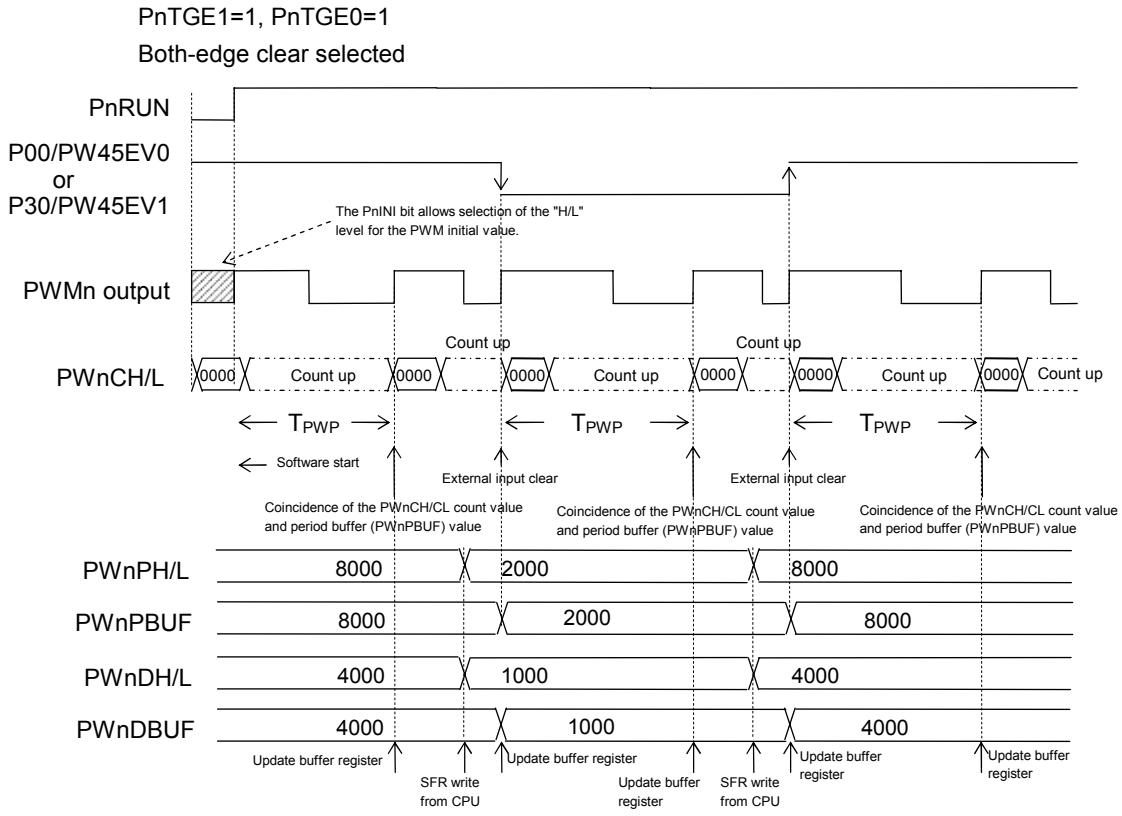
(a) Operation Timing Diagram with Software Start and External Input Clear

PnTGE1=1, PnTGE0=0

When rising-edge clear is selected



(b) Operation Timing Diagram with Software Start and External Input Clear



(c) Operation Timing Diagram with Software Start and External Input Clear

Figure 10-10 Operation Timing Diagram with Software Start and External Input Clear

For clear control by the external input, the values of the PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) are transferred to the PWMn duty buffer (PWnDBUF) and PWMn period buffer (PWnPBUF) respectively at the timing of the external input pins and edges specified by PnTGSEL, PnTGE1, and PnTGE0.

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the software start or external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

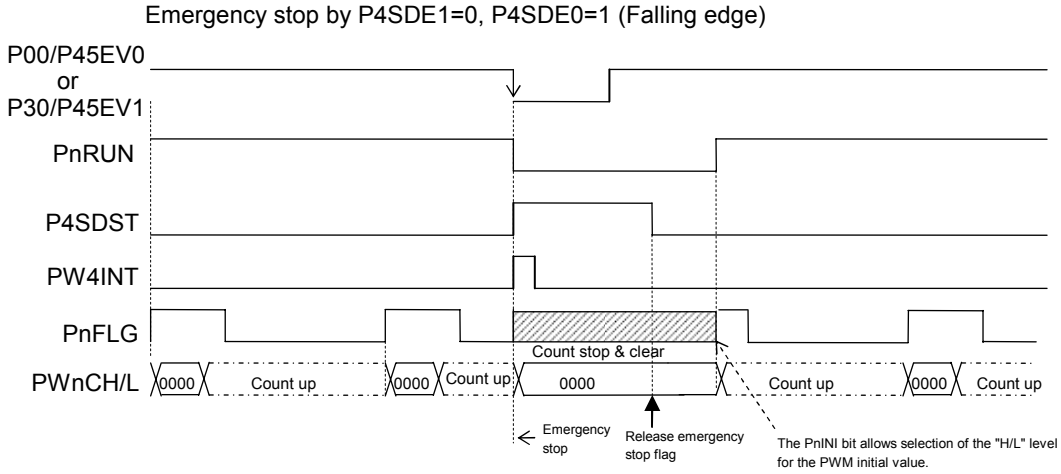
② When the external input clear control is done at a timing when PWMnPH/L or PWMnDH/L is changed while the PWM count is being paused, transfer to the PWMn duty buffer (PWnDBUF) or PWMn period buffer (PWnPBUF) may delay for one PWM clock.

10.3.8 Emergency Stop Operation

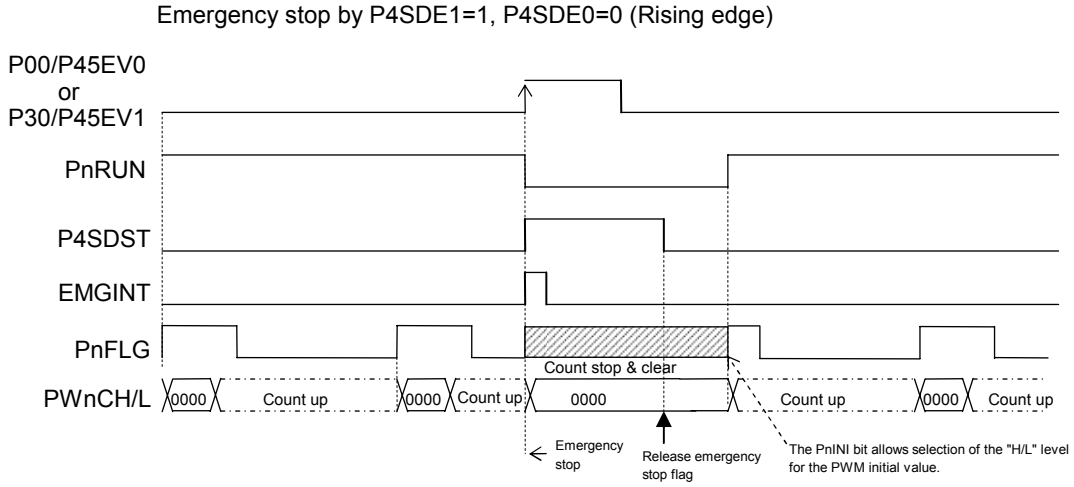
Setting the P4SDE1 and P4SDE0 bits of the PWM4 control register 3 (PW4CON3) enables the emergency stop function with the external input (P00/PW45EV0 or P30/PW45EV1 pin) that is selected by P4TGSEL. Note that the emergency stop function is valid only in the cooperation mode (P45MD="1").

When the external input that is selected by the P4TGSEL bit gets an edge input specified by P4SDE1 an P4SDE0, the emergency stop flag (P4SDST) is set to "1", an emergency stop interrupt (PW4INT) is generated, and the PWM counter is stopped/cleared. Because the PWM flag output (PnFLG) is cleared, the PWM4 and PWM5 outputs are turned off simultaneously.

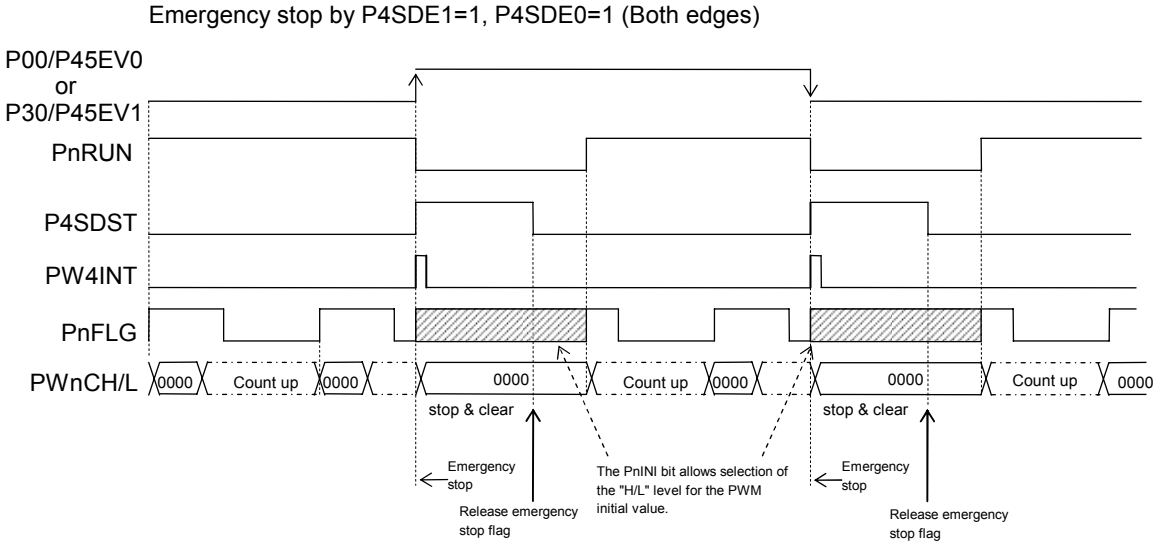
To release the emergency stop flag, write "1" to P4SDST of the PWM4 control register 3 (PW4CON3).
Figure 10-11 shows the operation timing.



(a) Timing with Falling-edge operation



(b) Timing with Rising-edge operation



(c) Timing with Both-edge operation

Figure 10-11 Operation Timing Diagram at Emergency Stop

10.4 Specifying Port Registers

To output the PWM waveform, the applicable bit of each related port register needs to be set. See Chapter 18, “Port 3” and Chapter 19, “Port 4” for details about the port registers.

10.4.1 Functioning P34 Pin (PWM4) as PWM Output

Set the P34MD1 bit (bit 4 of P3MOD1 register) to "1" and the P34MD0 bit (bit 4 of P3MOD0 register) to "0" to specify PWM4 as the tertiary function of P34.

Register name	P3MOD1 register (Address: 0F21DH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36MD1	P35MD1	**P34MD1**	P33MD1	P32MD1	P31MD1	P30MD1
Setting value	-	*	*	**1**	*	*	*	*

Register name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36MD0	P35MD0	**P34MD0**	P33MD0	P32MD0	P31MD0	P30MD0
Setting value	-	*	*	**0**	*	*	*	*

Set the P34C1 bit (bit 4 of P3CON1 register) to “1”, the P34C0 bit (bit 4 of P3CON0 register) to “1”, and the P34DIR bit (bit 4 of P3DIR register) to “0” to specify the state mode of the P34 pin used for PWM4 as the CMOS output.

Register name	P3CON1 register (Address: 0F21BH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36C1	P35C1	**P34C1**	P33C1	P32C1	P31C1	P30C1
Setting value	-	*	*	**1**	*	*	*	*

Register name	P3CON0 register (Address: 0F21AH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36C0	P35C0	**P34C0**	P33C0	P32C0	P31C0	P30C0
Setting value	-	*	*	**1**	*	*	*	*

Register name	P3DIR register (Address: 0F219H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36DIR	P35DIR	**P34DIR**	P33DIR	P32DIR	P31DIR	P30DIR
Setting value	-	*	*	**0**	*	*	*	*

Data of P34D bit (bit 4 of P3D register) does not affect to the PWM output function, so don’t care the data for the function.

Register name	P3D register (Address: 0F218H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	P36D	P35D	**P34D**	P33D	P32D	P31D	P30D
Setting value	-	*	*	******	*	*	*	*

- : Bit that does not exist
* : Bit not related to the PWM function
** : Don’t care

10.4.2 Functioning P43 Pin (PWM4) as PWM Output

Set the P43MD1 bit (bit 3 of P4MOD1 register) to "1" and the P43MD0 bit (bit 3 of P4MOD0 register) to "0" to specify PWM4 as the tertiary function of P43.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P46MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	*	**0**	*	*	*

Set the P43C1 bit (P4CON1 register bit 3) to "1", the P43C0 bit (P4CON0 register bit 3) to "1", and the P43DIR bit (P4DIR register bit 3) to "0" to specify the state mode of the P43 pin used for PWM4 as the CMOS output.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	*	**0**	*	*	*

The P43D bit (P4D register bit 3) data can either be "0" or "1".

Register name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Setting value	*	*	*	*	******	*	*	*

* : Bit not related to the PWM function
** : Don’t care

10.4.3 Functioning P35 Pin (PWM5) as PWM Output

Set the P35MD1 bit (bit 5 of P3MOD1 register) to "1" and the P35MD0 bit (bit 5 of P3MOD0 register) to "0" to specify PWM5 as the tertiary function of P35.

Register name	P3MOD1 register (Address: 0F21DH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36MD1	**P35MD1**	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
Setting value	-	*	**1**	*	*	*	*	*

Register name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36MD0	**P35MD0**	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
Setting value	-	*	**0**	*	*	*	*	*

Set the P35C1 bit (bit 5 of P3CON1 register) to “1”, the P35C0 bit (bit 5 of P3CON0 register) to “1”, and the P35DIR bit (bit 5 of P3DIR register) to “0” to specify the state mode of the P35 pin used for PWM5 as the CMOS output.

Register name	P3CON1 register (Address: 0F21BH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36C1	**P35C1**	P34C1	P33C1	P32C1	P31C1	P30C1
Setting value	-	*	**1**	*	*	*	*	*

Register name	P3CON0 register (Address: 0F21AH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36C0	**P35C0**	P34C0	P33C0	P32C0	P31C0	P30C0
Setting value	-	*	**1**	*	*	*	*	*

Register name	P3DIR register (Address: 0F219H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36DIR	**P35DIR**	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
Setting value	-	*	**0**	*	*	*	*	*

Data of P35D bit (bit 5 of P3D register) does not affect to the PWM output function, so don’t care the data for the function.

Register name	P3D register (Address: 0F218H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	-	P36D	**P35D**	P34D	P33D	P32D	P31D	P30D
Setting value	-	*	******	*	*	*	*	*

- : Bit that does not exist
* : Bit not related to the PWM function
** : Don’t care

10.4.4 Functioning P47 Pin (PWM5) as PWM Output

Set the P47MD1 bit (bit 7 of P4MOD1 register) to "1" and the P47MD0 bit (bit 7 of P4MOD0 register) to "0" to specify PWM5 as the tertiary function of P47.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47MD1**	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
Setting value	**1**	*	*	*	*	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47MD0**	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
Setting value	**0**	*	*	*	*	*	*	*

Set the P47C1 bit (P4CON1 register bit 7) to "1", the P47C0 bit (P4CON0 register bit 7) to "1", and the P47DIR bit (P4DIR register bit 7) to "0" to specify the state mode of the P47 pin used for PWM5 as the CMOS output.

Register name	P4CON1 register (Address: 0F223H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47C1**	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
Setting value	**1**	*	*	*	*	*	*	*

Register name	P4CON0 register (Address: 0F222H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47C0**	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
Setting value	**1**	*	*	*	*	*	*	*

Register name	P4DIR register (Address: 0F221H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47DIR**	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
Setting value	**0**	*	*	*	*	*	*	*

The P47D bit (P4D register bit 7) data can either be "0" or "1".

Register name	P4D register (Address: 0F220H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**P47D**	P46D	P45D	P44D	P43D	P42D	P41D	P40D
Setting value	******	*	*	*	*	*	*	*

* : Bit not related to the PWM function
** : Don’t care

Chapter 11

Synchronous Serial Port

11. Synchronous Serial Port

11.1 Overview

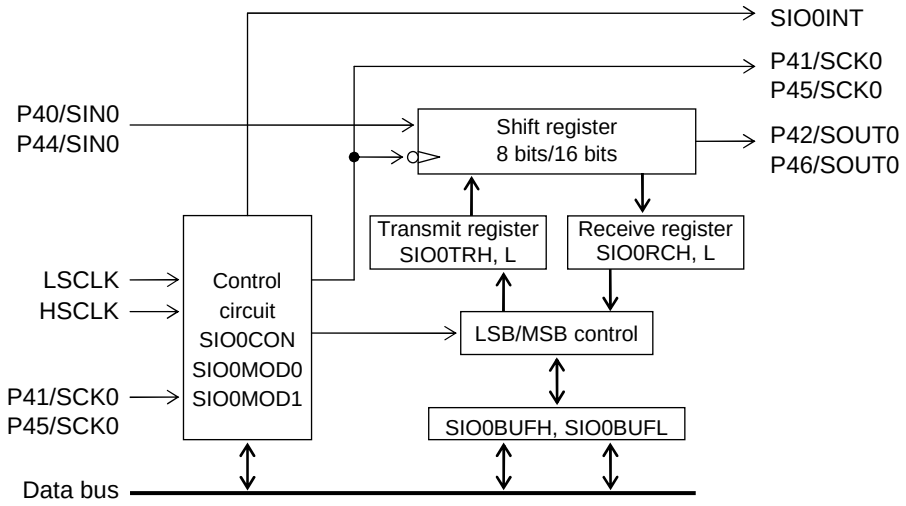
This LSI includes two channels of the 8/16-bit synchronous serial port (SSIO) and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
For the input clock, see Chapter 6, "Clock Generation Circuit".
When the synchronous serial port is used, the tertiary functions of port 4 or the tertiary functions of port 5 must be set. For the tertiary functions of port 4, see Chapter 19, "Port 4". For the tertiary functions of port 5, see Chapter 20, "Port 5".
The synchronous serial port (SSIO0) operates only when the DSIO0 bit of the block control register 2 (BLKCON2) is "0". When the DSIO0 bit is "1", every function of SSIO0 is in a reset state
The synchronous serial port (SSIO1) operates only when the DSIO1 bit of the block control register 2 (BLKCON2) is "0". When the DSIO1 bit is "1", every function of SSIO1 is in a reset state
For the block control registers, see Chapter 4, "MCU Control Function".

11.1.1 Features

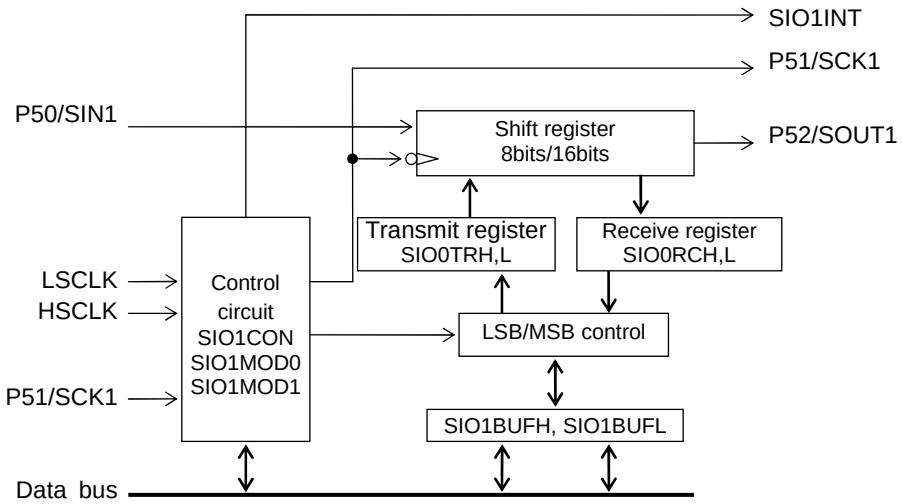
- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable fro the data length

11.1.2 Configuration

Figure 11-1 shows the configuration of the synchronous serial port.



SIO0BUFL: Serial port transmit/receive buffer L
SIO0BUFH: Serial port transmit/receive buffer H
SIO0CON: Serial port control register
SIO0MOD0: Serial port mode register 0
SIO0MOD1: Serial port mode register 1



SIO1BUFL: Serial port transmit/receive buffer L
SIO1BUFH: Serial port transmit/receive buffer H
SIO1CON: Serial port control register
SIO1MOD0: Serial port mode register 0
SIO1MOD1: Serial port mode register 1

Figure 11-1 Configuration of Synchronous Serial Port

11.1.3 List of Pins

Pin name	I/O	Description
P40/SIN0	I	Receive data input. Used for the tertiary function of the P40 pin.
P41/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P41 pin.
P42/SOUT0	O	Transmit data output. Used for the tertiary function of the P42 pin.
P44/SIN0	I	Receive data input. Used for the tertiary function of the P44 pin.
P45/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P45 pin.
P46/SOUT0	O	Transmit data output. Used for the tertiary function of the P46 pin.
P50/SIN1	I	Receive data input. Used for the tertiary function of the P50 pin.
P51/SCK1	I/O	Synchronous clock input/output. Used for the tertiary function of the P51 pin.
P52/SOUT1	O	Transmit data output. Used for the tertiary function of the P52 pin.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	—	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F288H	Serial port 1 transmit/receive buffer L	SIO1BUFL	SIO1BUF	R/W	8/16	00H
0F289H	Serial port 1 transmit/receive buffer H	SIO1BUFH		R/W	8	00H
0F28AH	Serial port 1 control register	SIO1CON	—	R/W	8	00H
0F28CH	Serial port 1 mode register 0	SIO1MOD0	SIO1MOD	R/W	8/16	00H
0F28DH	Serial port 1 mode register 1	SIO1MOD1		R/W	8	00H

11.2.2 Serial Port Transmit/Receive Buffers (SIO0BUFL, SIO0BUFH)

Address: 0F280H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F281H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUFL and SIO0BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port.
When data is written in SIO0BUFL and SIO0BUFH, the data is written in the transmit registers (SIO0TRL and SIO0TRH) and when data is read from SIO0BUFL and SIO0BUFH, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

11.2.3 Serial Port Transmit/Receive Buffers (SIO1BUFL, SIO1BUFH)

Address: 0F288H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1BUFL	S1B7	S1B6	S1B5	S1B4	S1B3	S1B2	S1B1	S1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F289H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1BUFH	S1B15	S1B14	S1B13	S1B12	S1B11	S1B10	S1B9	S1B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1BUFL and SIO1BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port.
When data is written in SIO1BUFL and SIO1BUFH, the data is written in the transmit registers (SIO1TRL and SIO1TRH) and when data is read from SIO1BUFL and SIO1BUFH, the contents of the receive registers (SIO1RCL and SIO1RCH) are read.

11.2.4 Serial Port Control Register (SIO0CON)

Address: 0F282H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0CON	—	—	—	—	—	—	—	S0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port.

[Description of Bits]

- **S0EN** (bit 0)
  The S0EN bit is used to specify start of synchronous serial communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated.
  The S0EN bit is set to "0" at a system reset.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

11.2.5 Serial Port Control Register (SIO1CON)

Address: 0F28AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1CON	—	—	—	—	—	—	—	S1EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1CON is a special function register (SFR) to control the synchronous serial port.

[Description of Bits]

- **S1EN** (bit 0)
  The S1EN bit is used to specify start of synchronous serial communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated.
  The S1EN bit is set to "0" at a system reset.

S1EN	Description
0	Stops communication. (Initial value)
1	Starts communication

11.2.6 Serial Port Mode Register 0 (SIO0MOD0)

Address: 0F284H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	—	—	—	—	S0LG	S0MD1	S0MD0	S0DIR
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD0 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S0DIR** (bit 0)
  The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

- **S0MD1, S0MD0** (bits 2, 1)
  The S0MD1 and S0MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S0LG** (bit 3)
  The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
  The S0LG bit is set to "0" at a system reset.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

Note:

- Do not change any of the SIO0MOD0 register settings during transmission/reception.
- When the synchronous serial port is used, the tertiary functions of SSIO must be set. For the tertiary functions of Port 4, see Chapter 19, "Port 4".

11.2.7 Serial Port Mode Register 0 (SIO1MOD0)

Address: 0F28CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	—	—	—	—	S1LG	S1MD1	S1MD0	S1DIR
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1MOD0 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S1DIR** (bit 0)
  The S1DIR is used to select LSB first or MSB first.

S1DIR	Description
0	LSB first (initial value)
1	MSB first

- **S1MD1, S1MD0** (bits 2, 1)
  The S1MD1 and S1MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S1MD1	S1MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S1LG** (bit 3)
  The S1LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
  The S1LG bit is set to "0" at a system reset.

S1LG	Description
0	8-bit length (initial value)
1	16-bit length

Note:

- Do not change any of the SIO1MOD0 register settings during transmission/reception.
- When the synchronous serial port is used, the tertiary functions of SSIO must be set. For the tertiary functions of Port 5, see Chapter 20, "Port 5".

11.2.8 Serial Port Mode Register 1 (SIO0MOD1)

Address: 0F285H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD1	—	—	—	S0CKT	S0CK3	S0CK2	S0CK1	S0CK0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD1 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S0CK2 to S0CK0** (bits 2 to 0)
  The S0CK2 to S0CK0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK3	S0CK2	S0CK1	S0CK0	Description
0	0	0	0	1/1 LSCLK (initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	External clock 0 (P41/SCK0)
0	1	1	1	External clock 0 (P45/SCK0)
1	0	0	0	1/1 HSCLK
1	0	0	1	1/2 HSCLK
1	0	1	∗	Prohibited
1	1	∗	∗	Prohibited

- **S0CKT** (bit 4)
  The S0CKT bit is used to select a tansfer clock output phase.

S0CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

Note:
- Do not change the value of the SIO0MOD1 register during transmission or reception.
- Set the S0CK3-S0CK0 bit not to exceed 4.2MHz.

11.2.9 Serial Port Mode Register 1 (SIO1MOD1)

Address: 0F28DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1MOD1	—	—	—	S1CKT	S1CK3	S1CK2	S1CK1	S1CK0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1MOD1 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S1CK2 to S1CK0** (bits 2 to 0)
  The S1CK2 to S1CK0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S1CK3	S1CK2	S1CK1	S1CK0	Description
0	0	0	0	1/1 LSCLK (initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	External clock 0 (P51/SCK1)
0	1	1	1	Prohibited
1	0	0	0	1/1 HSCLK
1	0	0	1	1/2 HSCLK
1	0	1	∗	Prohibited
1	1	∗	∗	Prohibited

- **S1CKT** (bit 4)
  The S1CKT bit is used to select a tansfer clock output phase.

S1CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

Note:

- Do not change the value of the SIO1MOD1 register during transmission or reception.
- Set the S1CK3-S1CK0 bit not to exceed 4.2MHz.

11.3 Description of Operation

11.3.1 Transmit Operation

When "1" is written to the SnMD1 bit and "0" is written to the SnMD0 bit of the serial mode register (SIOnMOD0), this LSI is set to a transmit mode.
When transmit data is written to the serial port transmit /receive buffer (SIOnBUFL and H) and the SnEN bit of the serial port control register (SIOnCON) is set to "1", transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Transmit data is output from the tertiary function pins (P42/SOUT0 or P46/SOUT0 or P52/SOUT1) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0 or P51/SCK1) is selected, the LSI is set to a slave mode.
The serial port mode register (SIOnMOD0) enables selection of MSB first/LSB first.
The transmit data output pin (P42/SOUT0 or P46/SOUT0 or P52/SOUT1) and transfer clock input/output pin (P41/SCK0 or P45/SCK0 or P51/SCK1) must be set to the tertiary functions.
Figures 11-2 and 11-3 show the transmit operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, LSB first, clock types 0 and 1).

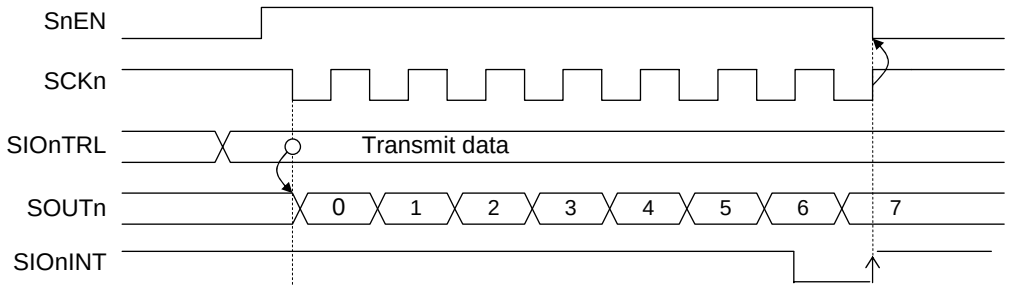


Figure 11-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first)

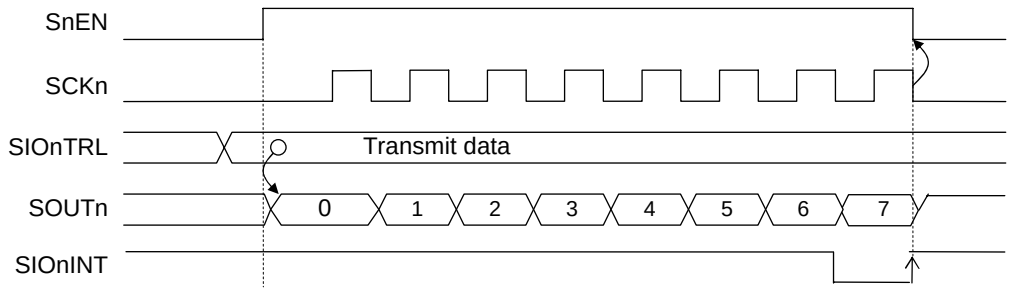


Figure 11-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first)

11.3.2 Receive Operation

When "0" is written to the SnMD1 bit and "1" is written to the SnMD0 bit of the serial mode register (SIOnMOD0), this LSI is set to a receive mode.
When the SnEN bit of the serial port control register (SIOnCON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Receive data is input from the tertiary function pins (P40/SIN0 or P44/SIN0 or P50/SIN1) of GPIO.
When an internal clock is selected in the serial port mode register (SIOnMD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0 or P51/SCK1) is selected, the LSI is set to a slave mode.
The serial port mode register (SIOnMOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0 or P44/SIN0 or P50/SIN1) and transfer clock input/output pin (P41/SCK0 or P45/SCK0 or P21/SCK1) must be set to the tertiary function.
Figures 11-4 and 11-5 show the receive operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, MSB first, clock types 0 and 1).

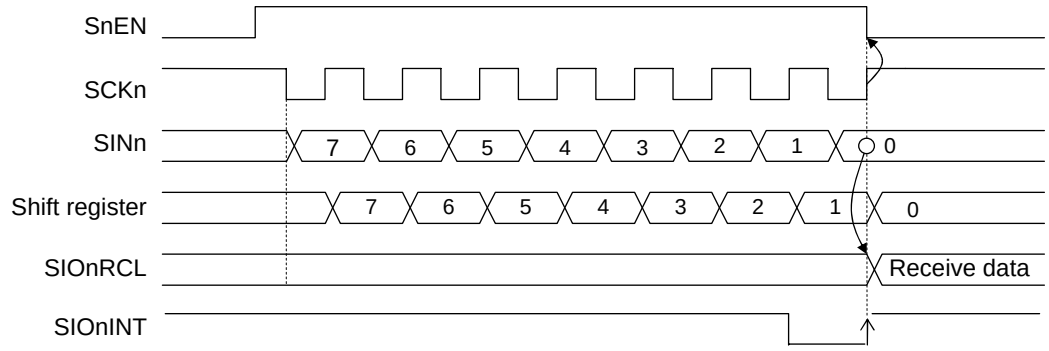


Figure 11-4 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first)

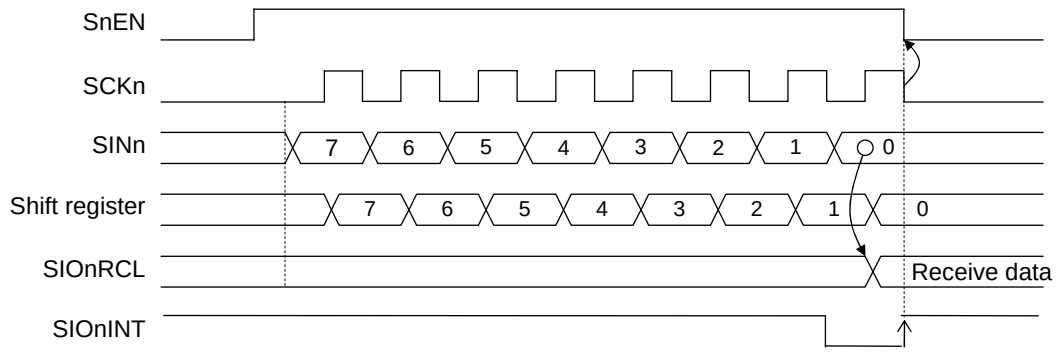


Figure 11-5 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first)

Note:
When the SOUTn pin is set to the tertiary function output in receive mode, a "H" level is output from the SOUTn output pin.

11.3.3 Transmit/Receive Operation

When "1" is written to the SnMD1 bit and "1" is written to the SnMD0 bit of the serial mode register (SIOnMOD0), this LSI is set to a transmit/receive mode.
When the S0EN bit of the serial port control register (SIOnCON) is set to "1", transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Receive data is input from the tertiary function pins (P40/SIN0 or P44/SIN0 or P50/SIN1) of GPIO, and transmit data is output from the tertiary function pins (P42/SOUT0 or P46/SOUT0 or P52/SOUT1) of GPIO
When an internal clock is selected in the serial port mode register (SIOnMD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0 or P51/SCK1) is selected, the LSI is set ot a slave mode.
The serial port mode register (SIOnMOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0 or P44/SIN0 or P50/SIN1), the transmit data output pin (P42/SOUT0 or P46/SOUT0 or P52/SOUT1), and transfer clock input/output pin (P41/SCK0 or P45/SCK0 or P51/SCK1) must be set to the tertiary function.
Figure 11-6 shows the transmit/receive operation waveforms of the synchronous serial port (16-bit length, LSB first, clock types 0).

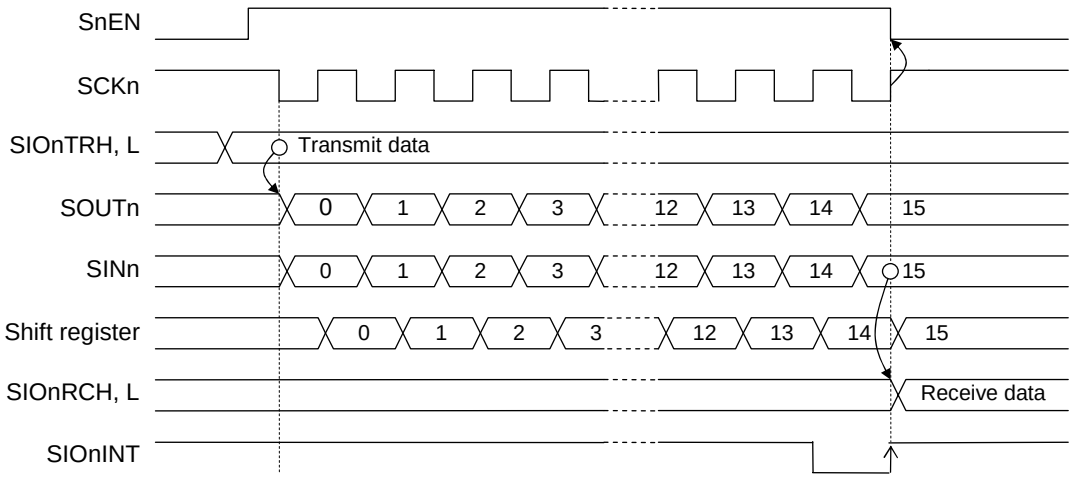


Figure 11-6 Transmit/Receive Operation Waveforms of Synchronous Serial Port (16-bit Length, LSB first, Clock Type 0)

11.4 Register setup of the port

For enable the SSIO function, each related port register needs to be set up. Refer to the Chapter 16, "Port 4" for details of each register.

11.4.1 When operating the SSIO0 function in master mode using P42 pin (SOUT0:output), P41 pin (SCK0:input/output), and P40 pin (SIN0:input).

SSIO is selected as the secondary function of P42, P41, and P40 by setting P42MD1-P40MD1 bit (P4MOD1 register: bit2-0) to "1" and setting P42MD0-P40MD0 bit (P4MOD0 register: bit2-0) to "0".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
value	*	*	*	*	*	**1**	**1**	**1**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
value	*	*	*	*	*	**0**	**0**	**0**

The state of the P42 and P41 pin is selected as CMOS output mode by setting P42C1-P41C1 bit (P4CON1 register:bit2-1) to "1" , setting P42C0-P41C0 bit (P4CON0 register:bit2-1) to "1" and setting P42DIR-P41DIR bit (P4DIR register:bit2-1) to "0". Additionally, the P40 pin is selected as input pin by setting P40DIR bit (P4DIR register: bit0) to "1"
The setting value of P40C1 bit and P40C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
value	*	*	*	*	*	**1**	**1**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
value	*	*	*	*	*	**1**	**1**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	*	*	*	*	*	**0**	**0**	**1**

As for P42D-P40D bit (P4D register:bit2-0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47 D	P46 D	P45 D	P44 D	P43D	**P42D**	**P41D**	**P40D**
value	*	*	*	*	*	******	******	******

* : no relation to the SSIO function **: Don't care $: Optional

11.4.2 When operating the SSIO0 function in slave mode using P42 pin (SOUT0:output), P41 pin (SCK0:input/output), and P40 pin (SIN0:input).

SSIO is selected as the secondary function of P42, P41, and P40 by setting P42MD1-P40MD1 bit (P4MOD1 register: bit2-0) to "1" and setting P42MD0-P40MD0 bit (P4MOD0 register: bit2-0) to "0". It is the same setup as the case of master mode.

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
value	*	*	*	*	*	**1**	**1**	**1**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
value	*	*	*	*	*	**0**	**0**	**0**

The state of the P42 pin is selected as CMOS output mode by setting P42C1 bit (P4CON1 register:bit2) to "1" , setting P42C0 bit (P4CON0 register:bit2) to "1" and setting P42DIR bit (P4DIR register:bit2) to "0". Additionally, the P41 and P40 pin is selected as input pin by setting P41DIR-P40DIR bit (P4DIR register: bit1-0) to "1"
The setting value of P41C1-P40C1 bit and P41C0-P40C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P41 and P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
value	*	*	*	*	*	**1**	**$**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
value	*	*	*	*	*	**1**	**$**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	*	*	*	*	*	**0**	**1**	**1**

As for P42D-P40D bit (P4D register:bit2-0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P47 D	P46 D	P45 D	P44 D	P43D	**P42D**	**P41D**	**P40D**
value	*	*	*	*	*	******	******	******

* : no relation to the SSIO function **: Don't care $: Optional

11.4.3 When operating the SSIO function in master mode using P52 pin (SOUT1:output), P51 pin (SCK1:input/output), and P50 pin (SIN1:input).

SSIO is selected as the secondary function of P52, P51, and P50 by setting P52MD1-P50MD1 bit (P5MOD1 register: bit2-0) to "1" and setting P52MD0-P50MD0 bit (P5MOD0 register: bit2-0) to "0".

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53MD1	**P52MD1**	**P51MD1**	**P50MD1**
value	-	-	-	-	*	**1**	**1**	**1**

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53MD0	**P52MD0**	**P51MD0**	**P50MD0**
value	-	-	-	-	*	**0**	**0**	**0**

The state of the P52 and P51 pin is selected as CMOS output mode by setting P52C1-P51C1 bit (P5CON1 register:bit2-1) to "1" , setting P52C0-P51C0 bit (P5CON0 register:bit2-1) to "1" and setting P52DIR-P51DIR bit (P5DIR register:bit2-1) to "0". Additionally, the P50 pin is selected as input pin by setting P50DIR bit (P5DIR register: bit0) to "1"
The setting value of P50C1 bit and P50C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P50 pin is connected.

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53C1	**P52C1**	**P51C1**	**P50C1**
value	-	-	-	-	*	**1**	**1**	**$**

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53C0	**P52C0**	**P51C0**	**P50C0**
value	-	-	-	-	*	**1**	**1**	**$**

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53DIR	**P52DIR**	**P51DIR**	**P50DIR**
value	-	-	-	-	*	**0**	**0**	**1**

As for P52D-P50D bit (P5D register:bit2-0), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53D	**P52D**	**P51D**	**P50D**
value	-	-	-	-	*	******	******	******

* : no relation to the SSIO function **: Don't care $: Optional

11.4.4 When operating the SSIO1 function in slave mode using P52 pin (SOUT1:output), P51 pin (SCK1:input/output), and P50 pin (SIN1:input).

SSIO is selected as the secondary function of P52, P51, and P50 by setting P52MD1-P50MD1 bit (P5MOD1 register: bit2-0) to "1" and setting P52MD0-P50MD0 bit (P5MOD0 register: bit2-0) to "0". It is the same setup as the case of master mode.

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53MD1	**P52MD1**	**P51MD1**	**P50MD1**
value	-	-	-	-	*	**1**	**1**	**1**

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53MD0	**P52MD0**	**P51MD0**	**P50MD0**
value	-	-	-	-	*	**0**	**0**	**0**

The state of the P52 pin is selected as CMOS output mode by setting P52C1 bit (P5CON1 register:bit2) to "1" , setting P52C0 bit (P5CON0 register:bit2) to "1" and setting P52DIR bit (P5DIR register:bit2) to "0". Additionally, the P51 and P50 pin is selected as input pin by setting P51DIR-P50DIR bit (P5DIR register: bit1-0) to "1"
The setting value of P51C1-P50C1 bit and P51C0-P50C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P51 and P50 pin is connected.

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53C1	**P52C1**	**P51C1**	**P50C1**
value	-	-	-	-	*	**1**	**$**	**$**

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53C0	**P52C0**	**P51C0**	**P50C0**
value	-	-	-	-	*	**1**	**$**	**$**

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53DIR	**P52DIR**	**P51DIR**	**P50DIR**
value	-	-	-	-	*	**0**	**1**	**1**

As for P52D-P50D bit (P5D register:bit2-0), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P53D	**P52D**	**P51D**	**P50D**
value	-	-	-	-	*	******	******	******

* : no relation to the SSIO function **: Don't care $: Optional

Chapter 12

UART

12. UART

12.1 Overview

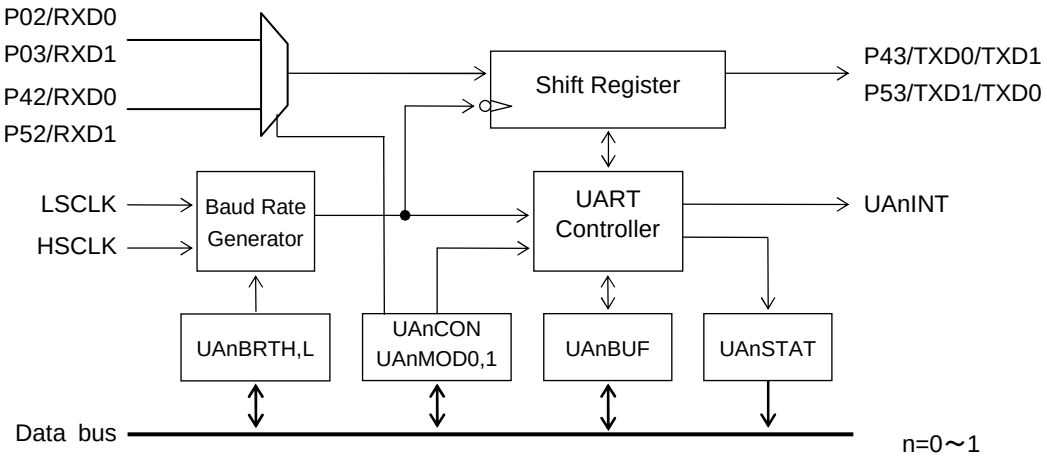
This LSI includes UART (Universal Asynchronous Receiver Transmitter) which is an asynchronous serial interface of half-duplex communication.（A full-duplex is also possible by using 2 channels.）
For the input clock, see Chapter 6, "Clock Generation Circuit".
The use of UART requires setting of the secondary/fourthly functions of Port 4 or Port5. For setting of the secondary/fourthly functions of Port 4, see Chapter 19, "Port 4". For setting of the secondary/fourthly functions of Port 5, see Chapter 20, "Port 5".
The UART operates only when the DUA0 and DUA1 bits of the block control register 2 (BLKCON2) is "0". When the DUA0 and DUA1 bits are "1", every function of the UART is in a reset state.
For the block control registers, see Chapter 4, "MCU Control Function".

12.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable
- Odd parity, even parity, or no parity selectable
- 1 stop bit or 2 stop bits selectable
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic
- LSB first or MSB first selectable as a communication direction
- Communication speed: Settable within the range of 2400 bps to 115200 bps
- Built-in baud rate generator

12.1.2 Configuration

Figure 12-1 shows the configuration of the UART.



UAnBUF: UARTn transmit/receive buffer
UAnBRTH, L: UARTn baud rate registers H, L
UAnCON: UARTn control register
UAnMOD0, 1: UARTn mode registers 0, 1
UAnSTAT: UARTn status register

Figure 12-1 Configuration of UART

12.1.3 List of Pins

Pin name	I/O	Description
P02 / RXD0	I	UART0, UART2 data input pin Used for the primary function of the P02 pin.
P42 / RXD0	I	UART0, UART2 data input pin Used for the secondary / fourthly function of the P42 pin.
P43 / TXD0 / TXD1	O	UART0, UART2 data output pin Used for the secondary / fourthly function of the P43 pin.
P03 / RXD1	I	UART1 data input pin Used for the primary function of the P03 pin.
P52 / RXD1	I	UART1 data input pin Used for the secondary function of the P52 pin.
P53 / TXD1 / TXD0	O	UART1, UART2 data output pin Used for the secondary / fourthly function of the P53 pin.

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F298H	UART1 transmit/receive buffer	UA1BUF	—	R/W	8	00H
0F299H	UART1 control register	UA1CON	—	R/W	8	00H
0F29AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F29BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F29CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F29DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F29EH	UART1 status register	UA1STAT	—	R/W	8	00H

12.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmit/receive data of the UART.
In transmit mode, write transmission data to UA0BUF. To transmit data continuously, write the next data to UA0BUF after making sure that the U0FUL flag of the UART0 status register (UA0STAT) is "0". Any value written to UA0BUF can be read.
In receive mode, since data received at termination of reception is stored in UA0BUF, read the contents of UABUF using the UART0 interrupt at termination of reception. At continuous reception, UA0BUF is updated whenever reception terminates. Any write to UA0BUF is disabled in receive mode.
The bits not required when 5-bit, 6-bit, 7-bit, or 8-bit data length is selected become invalid in transmit mode and are set to "0" in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting transmit data in UA0BUF.

12.2.3 UART1 Transmit/Receive Buffer (UA1BUF)

Address: 0F298H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1BUF	U1B7	U1B6	U1B5	U1B4	U1B3	U1B2	U1B1	U1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1BUF is a special function register (SFR) to store the transmit/receive data of the UART.
In transmit mode, write transmission data to UA1BUF. To transmit data continuously, write the next data to UA1BUF after making sure that the U1FUL flag of the UART1 status register (UA1STAT) is "0". Any value written to UA1BUF can be read.
In receive mode, since data received at termination of reception is stored in UA1BUF, read the contents of UABUF using the UART1 interrupt at termination of reception. At continuous reception, UA1BUF is updated whenever reception terminates. Any write to UA1BUF is disabled in receive mode.
The bits not required when 5-bit, 6-bit, 7-bit, or 8-bit data length is selected become invalid in transmit mode and are set to "0" in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA1MOD0 and UA1MOD1) before setting transmit data in UA1BUF.

12.2.4 UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Starts communication.

12.2.5 UART1 Control Register (UA1CON)

Address: 0F299H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1CON	—	—	—	—	—	—	—	U1EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA1CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U1EN** (bit 0)
  The U1EN bit is used to specify the UART communication operation start. When U1EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U1EN	Description
0	Stops communication. (Initial value)
1	Starts communication.

12.2.6 UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bits
Initial value: 06H

	7	6	5	4	3	2	1	0
UA0MOD0	—	—	U0RSS	U0RSEL	—	U0CK1	U0CK0	U0IO
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U0CK1, U0CK0** (bits 2, 1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited (UART0 does not operate)
1	*	HSCLK

- **U0RSEL** (bit 4)
  The U0RSEL bit is used to select the receive data input pin for the UART0.

U0RSEL	Description
0	Selects the P02 pin. (Initial value)
1	Selects the P42 pin.

- **U0RSS** (bit 5)
  The U0RSS bit is used to select the receive data input sampling timing for the UART0.

U0RSS	Description
0	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 (Initial value)
1	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 – 1

Note:

- Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.
- When selecting the P42 pin as the receive data input pin and P43 pin as the transfer data output pin, it is necessary to set settings for the Port 4 secondary functions. For the details of the Port 4 secondary function settings, see Chapter 19, "Port 4".

12.2.7 UART1 Mode Register 0 (UA1MOD0)

Address: 0F29AH
Access: R/W
Access size: 8/16 bits
Initial value: 06H

	7	6	5	4	3	2	1	0
UA1MOD0	—	—	U1RSS	U1RSEL	—	U1CK1	U1CK0	U1IO
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U1IO** (bit 0)
  The U1IO bit is used to select transmit or receive mode.

U1IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U1CK1, U1CK0** (bits 2, 1)
  The U1CK1 and U1CK0 bits are used to select the clock to be input to the baud rate generator of the UART1.

U1CK1	U1CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited (UART1 does not operate)
1	*	HSCLK

- **U1RSEL** (bit 4)
  The U1RSEL bit is used to select the receive data input pin for the UART1.

U1RSEL	Description
0	Selects the P03 pin. (Initial value)
1	Selects the P52 pin.

- **U1RSS** (bit 5)
  The U1RSS bit is used to select the receive data input sampling timing for the UART1.

U1RSS	Description
0	Values-set-in-the-UA1BRTH-and-UA1BRTL-registers/2 (Initial value)
1	Values-set-in-the-UA1BRTH-and-UA1BRTL-registers/2 – 1

Note:

- Always set the UA1MOD0 register while communication is stopped, and do not rewrite it during communication.
- When selecting the P52 pin as the receive data input pin and the P53 pin as the transfer data output pin, it is necessary to set settings for the Port 5 secondary functions. For the details of the Port 5 secondary function settings, see Chapter 20, "Port 5".

12.2.8 UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	—	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0LG1, U0LG0** (bits 1, 0)
  The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1, U0PT0** (bits 3, 2)
  The U0PT1 and U0PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 4)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U0NEG** (bit 5)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 6)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

12.2.9 UART1 Mode Register 1 (UA1MOD1)

Address: 0F29BH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1MOD1	—	U1DIR	U1NEG	U1STP	U1PT1	U1PT0	U1LG1	U1LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U1LG1, U1LG0** (bits 1, 0)
  The U1LG1 and U1LG0 bits are used to specify the data length in the communication of the UART.

U1LG1	U1LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U1PT1, U1PT0** (bits 3, 2)
  The U1PT1 and U1PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART.

U1PT1	U1PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U1STP** (bit 4)
  The U1STP bit is used to select the stop bit length in the communication of the UART.

U1STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U1NEG** (bit 5)
  The U1NEG bit is used to select positive logic or negative logic in the communication of the UART.

U1NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U1DIR** (bit 6)
  The U1DIR bit is used to select LSB first or MSB first in the communication of the UART.

U1DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA1MOD1 register while communication is stopped, and do not rewrite it during communication.

12.2.10 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 12.3.2, "Baud Rate".

Note:
Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

12.2.11 UART1 Baud Rate Registers L, H (UA1BRTL, UA1BRTH)

Address: 0F29CH
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA1BRTL	U1BR7	U1BR6	U1BR5	U1BR4	U1BR3	U1BR2	U1BR1	U1BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F29DH
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA1BRTH	—	—	—	—	U1BR11	U1BR10	U1BR9	U1BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA1BRTL and UA1BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 12.3.2, "Baud Rate".

Note:
Always set the UA1BRTL and UA1BRTH registers while communication is stopped, and do not rewrite them during communication.

12.2.12 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	—	—	—	—	U0FUL	U0PER	U0OER	U0FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	Framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previous receive data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

- **U0FUL** (bit 3)
  The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When transmit data is written in UA0BUF in transmit mode, this bit is set to "1" and when transmit data is transferred to the shift register, this bit is set to "0". To transmit data consecutively, write the next transmit data to UA0BUF after checking that the U0FUL flag has been set to "0".
  The U0FUL bit is fixed to "0" in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

12.2.13 UART1 Status Register (UA1STAT)

Address: 0F29EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1STAT	—	—	—	—	U1FUL	U1PER	U1OER	U1FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA1STAT, all the flags are initialized to "0".

[Description of Bits]

- **U1FER** (bit 0)
  The U1FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U1FER bit is set to "1". This bit is updated each time reception is completed.
  The U1FER bit is fixed to "0" in transmit mode.

U1FER	Description
0	No framing error (initial value)
1	Framing error

- **U1OER** (bit 1)
  The U1OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA1BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U1EN bit and then reception is restarted, this bit is set to "1" unless the previous receive data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U1OER bit is fixed to "0" in transmit mode.

U1OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U1PER** (bit 2)
  The U1PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U1PER is updated whenever data is received.
  The U1PER bit is fixed to "0" in transmit mode.

U1PER	Description
0	No parity error (initial value)
1	Parity error

- **U1FUL** (bit 3)
  The U1FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When transmit data is written in UA1BUF in transmit mode, this bit is set to "1" and when transmit data is transferred to the shift register, this bit is set to "0". To transmit data consecutively, write the next transmit data to UA1BUF after checking that the U1FUL flag has been set to "0".
  The U1FUL bit is fixed to "0" in receive mode.

U1FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

12.3 Description of Operation

12.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected. All these options are set with the UARTn mode register (UAnMOD1).
Figure 12-2 and Figure 12-3 show the positive logic input/output format and negative logic input/output format, respectively.

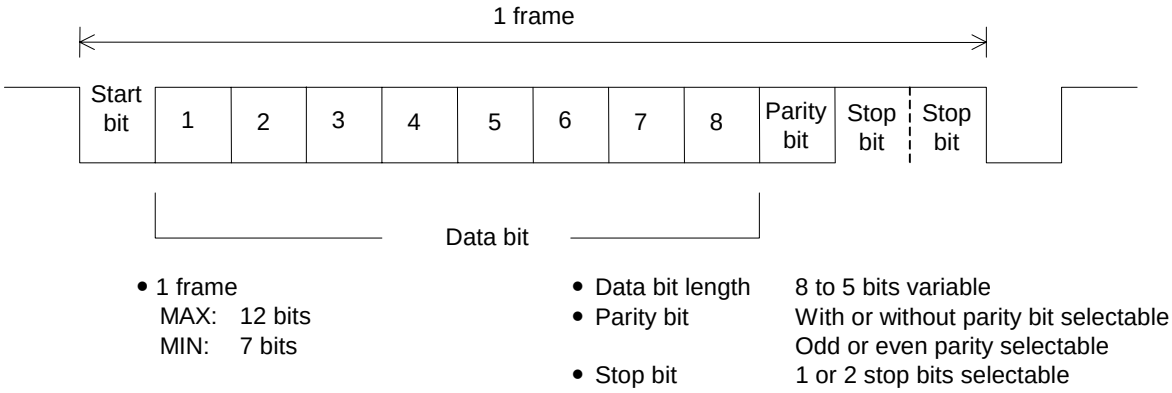


Figure 12-2 Positive Logic Input/Output Format

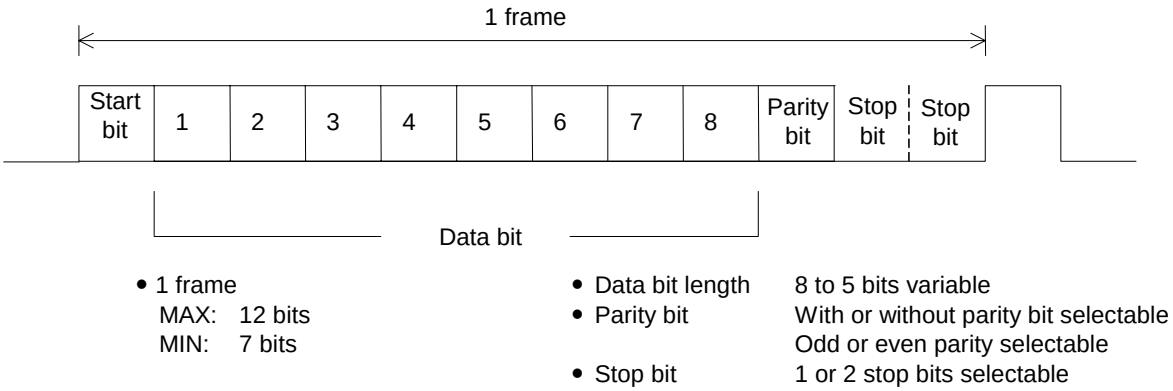


Figure 12-3 Negative Logic Input/Output Format

12.3.2 Baud Rate

Baud rates are generated by the baud generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (UnCK1, UnCK0) of the UARTn mode register 0 (UAnMOD0). The count value of the baud rate generator can be set by writing it in the UARTn baud rate register H or L (UAnBRTH, UAnBRTL). The maximum count is 4096.
The setting values of UAnBRTH and UAnBRTL are expressed by the following equation.

$$\text{UAnBRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 12-1 lists the count values for typical baud rates.

Table 12-1 Count Values for Typical Baud Rates

Baud rate	Baud rate generator clock selection			Count value of the baud rate generator				Error
	Baud rate clock	UnCK1	UnCK0	Count value	Period of 1 bit	UAnBRTH	UAnBRTL	
2400 bps	8.192MHz	1	∗	3413	Approx. 417 μs	0DH	054H	0.01%
4800 bps		1	∗	1707	Approx. 208 μs	06H	0AAH	-0.02%
9600 bps		1	∗	853	Approx. 104 μs	03H	054H	0.04%
19200 bps		1	∗	427	Approx. 52 μs	01H	0AAH	-0.08%
38400 bps		1	∗	213	Approx. 26 μs	00H	0D4H	0.16%
57600 bps		1	∗	142	Approx. 17.4 μs	00H	08DH	0.16%
115200 bps		1	∗	71	Approx. 8.7 μs	00H	046H	0.16%

12.3.3 Transmit Data Direction

Figure 12-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

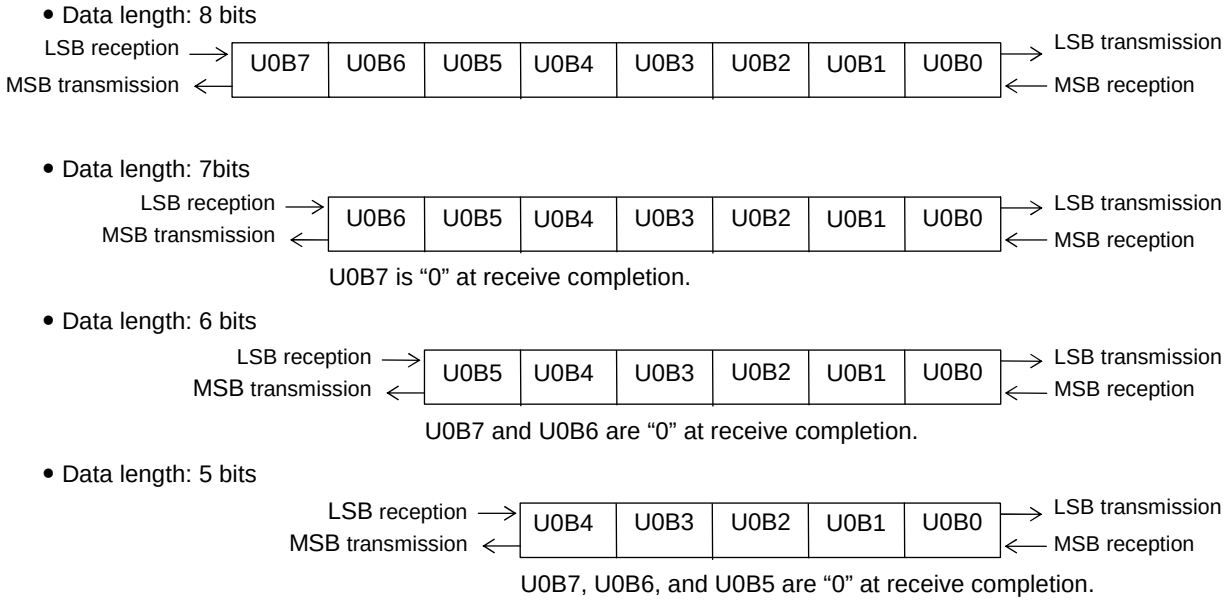


Figure 12-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

Note:
When the TXDn pin is set to serve the secondary function output in receive mode, "H" level is output from the TXDn pin.

12.3.4 Transmit Operation

Transmission is started by setting the UnIO bit of the UARTn mode register 0 (UAnMOD0) to "0" to select transmit mode and setting the UnEN bit of the UARTn control register (UAnCON) to "1".
Figure 12-5 shows the operation timing for transmission.

When the UnEN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmission.
The start bit is output to the TXDn pin by the falling edge of the internal transfer clock (②). Subsequently, transmit data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UARTn interrupt is requested. In the UARTn interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UAnBUF).
When the next data to be transmitted is written to the transmit/receive buffer (UAnOBUF), the transmit buffer status flag (UnFUL) is set to "1" (③) and a UARTn interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. If the UARTn interrupt routine is terminated without writing the next data to the transmit/receive buffer, the UnFUL bit is not set to "1" (⑤) and transmission continues up to the transmission of the stop bit, then the UnEN bit is reset to "0" and a UARTn interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

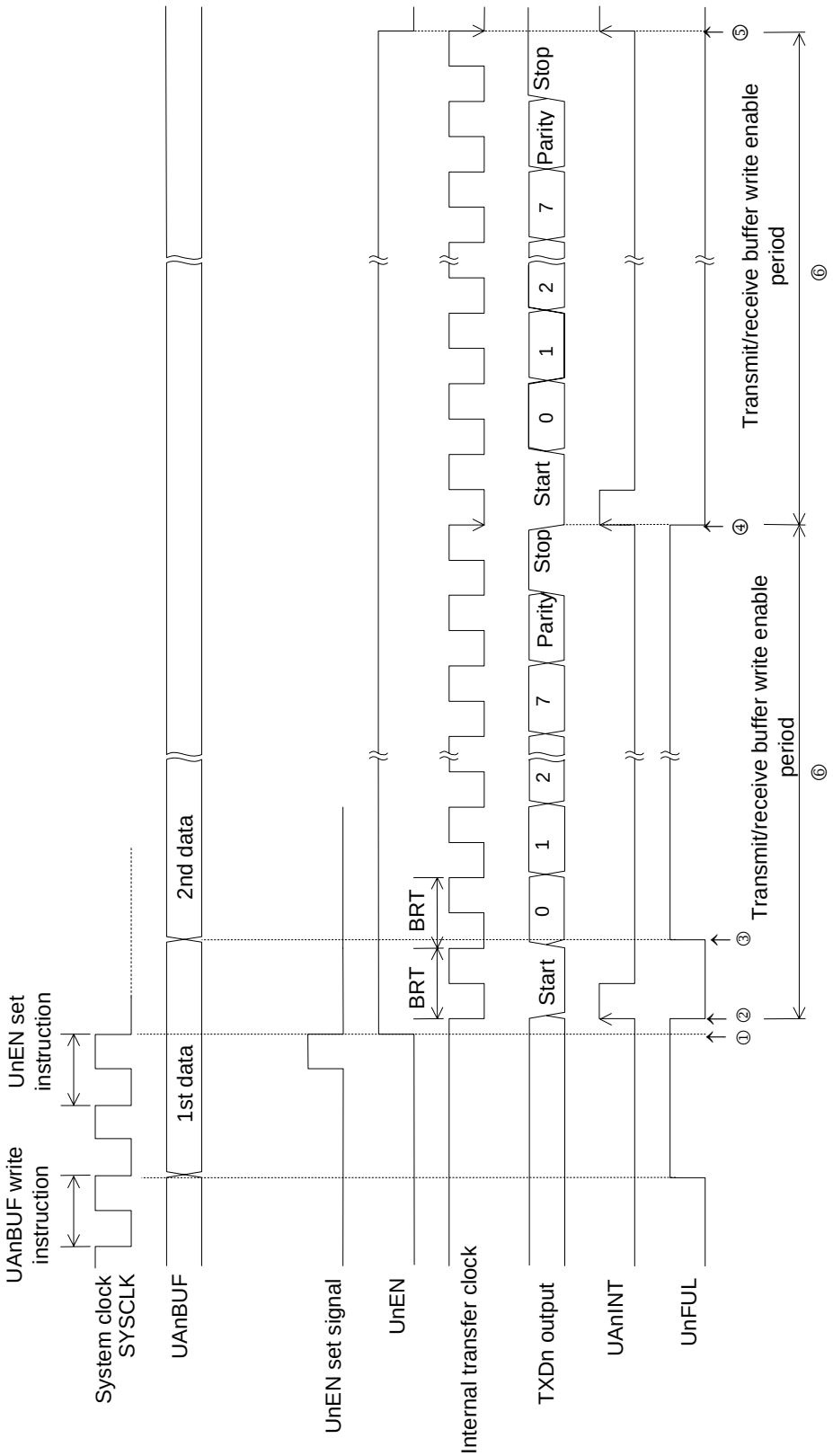


Figure 12-5 Operation Timing in Transmission

12.3.5 Receive Operation

Reception is started by selecting a receive data input pin using the UnRSEL bit of the UARTn mode register 0 (UAnMOD0), then setting the UnIO bit of UAnMOD0 to "0" to select receive mode, and then setting the UnEN bit of the UARTn control register (UAnCON) to "1".
Figure 12-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXDn and waits for the arrival of a start bit.
When detecting a start bit (②), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit receive data is transferred to the transmit/receive buffer (UAnBUF) concurrently with the fall of the internal transfer clock of ③.
The LSI requests a UARTn interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the receive data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UARTn status register (UAnSTAT) to "1".

Parity error : SnPER = "1"
Overrun error : SnOER = "1"
Framing error : SnFER = "1"

As shown in Figure 12-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the receive data.
Reception continues until the UnEN bit is reset to "0" by the program. When the UnEN bit is reset to "0" during reception, the data received may be destroyed. When the UnEN bit is reset to "0" during the "UnEN reset enable period" in Figure 12.6, the data received is protected.

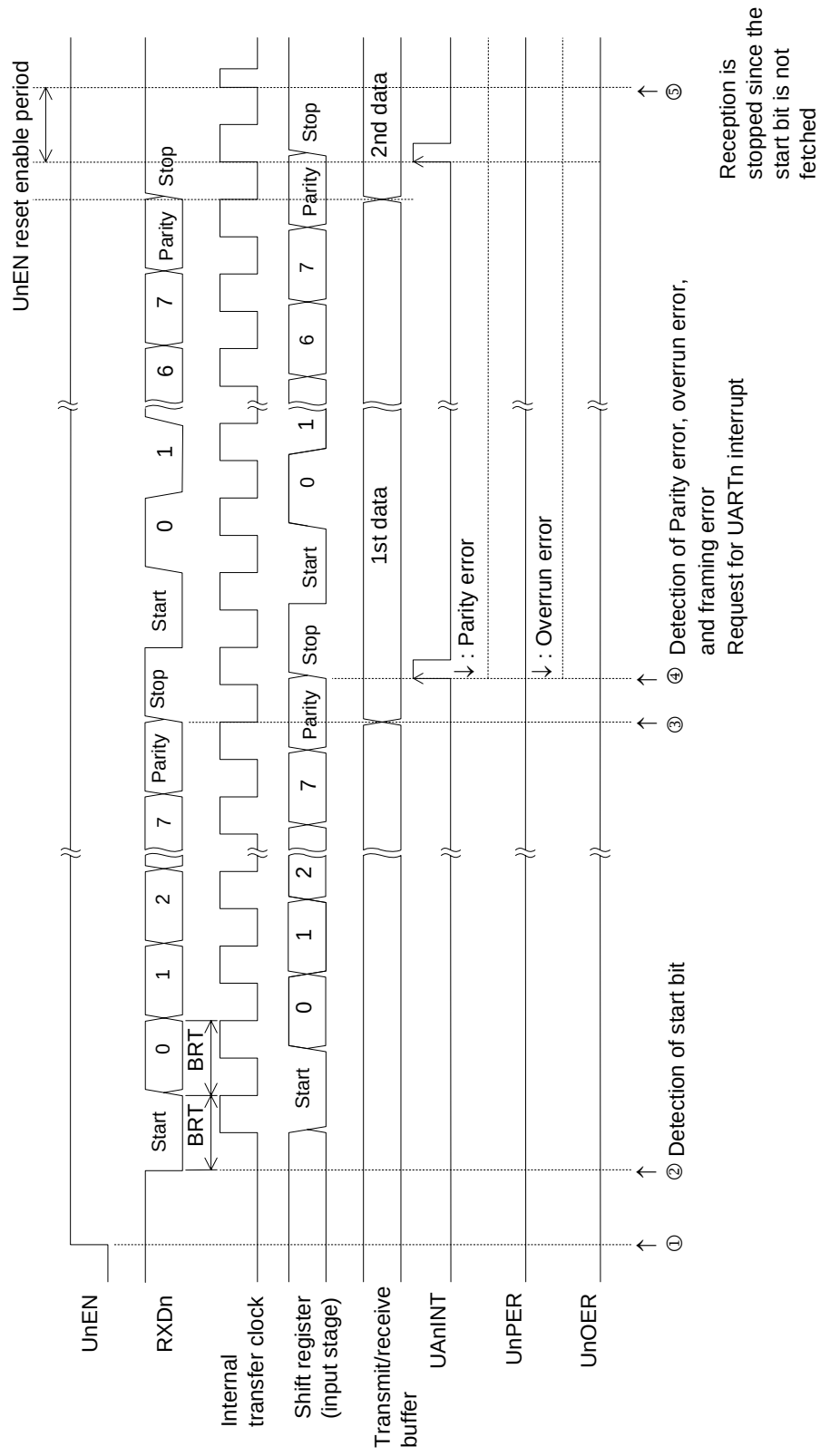


Figure 12-6 Operation Timing in Reception

12.3.5.1 Detection of Start bit

The start bit is sampled by the baud rate generator clock (HSCLK). Therefore, there is a possibility that the start bit will be detected with a delay of a maximum of one cycle of the baud rate generator clock.
Figure 12-7 shows the start bit detection timing.

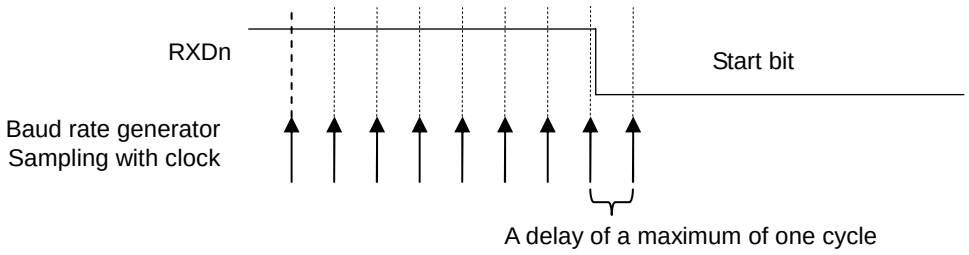
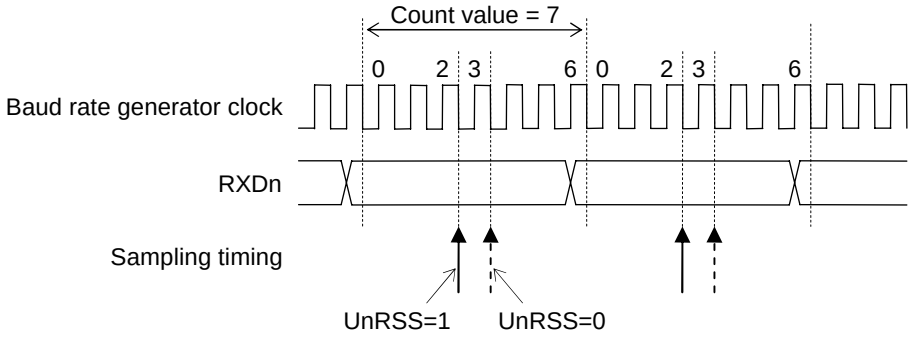


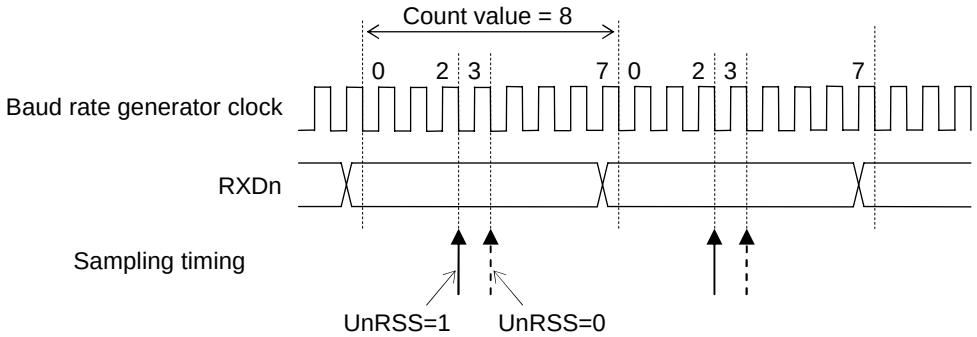
Figure 12-7 Start Bit Detection Timing (Positive Logic)

12.3.5.2 Sampling Timing

When the start bit is detected, the receive data that has been input to RXDn is sampled roughly at the middle of the baud rate and shifted into the shift register.
This sampling timing, where the receive data is sampled to be shifted into the shift register, can be adjusted by one clock pulse of the baud rate generator clock by using the UnRSEL bit of the UARTn mode register 0 (UAnMOD0). Figure 12-8 shows the relationship between the UnRSEL bit and sampling timing.



(1) When the baud rate generator count value is "7" (odd number)



(2) When the baud rate generator count value is "8" (even number)

Figure 12-8 Relationship between UnRSS Bit and Sampling Timing

12.3.5.3 Reception Margin

If there are any errors between the baud rate on the transmitter side and the baud rate to be generated by the baud rate generator of the LSI, those errors will be accumulated until the last stop bit in one frame is shifted in, causing the reception margin to be reduced.
Figure 12-9 shows the waveform indicating baud rate errors and reception margin.

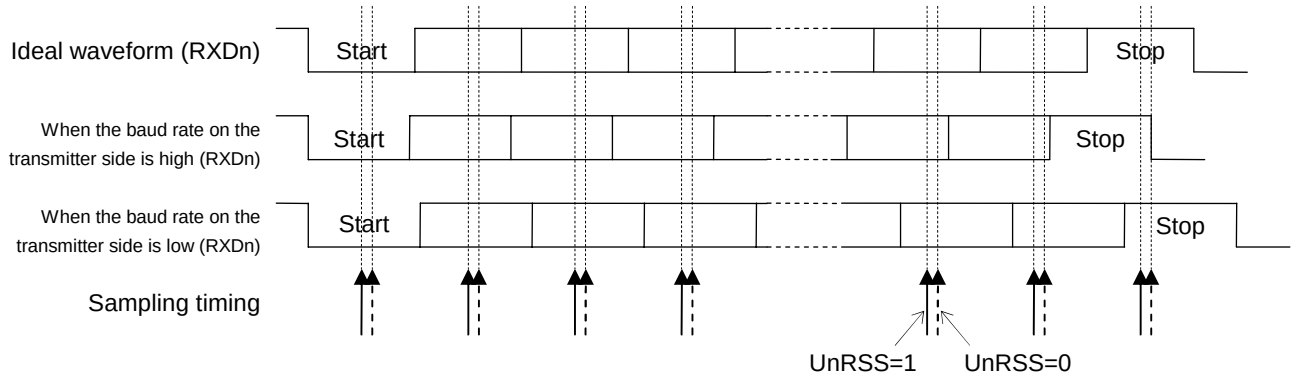


Figure 12-9 Baud Rate Errors and Reception Margin

Note:
When doing system design, ensure enough reception margin taking into account the effects of noise and receive data rounding as well as the difference in baud rate between the transmitter side and receiver side and a delay in the detection of start bit.

12.4 Register setup of the port

For operate the UART function, each related port register needs to be set up. Refer to the Chapter 17, "Port 5", the Chapter 16, "Port 4" and the Chapter 13, "Port 0" for details of each register.

12.4.1 When operating the UART function using P43 pin (TXD0:output) and P42 pin (RDX0:input)

The UART is selected as the secondary function of the P43 pin and the P42 pin by setting P43MD1-P42MD1 bit (P4MOD1 register: bit3-2) to "0" and setting P43MD0-P42MD0 bit (P4MOD0 register: bit3-2) to "1".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	**P42MD1**	P41MD1	P40MD1
value	*	*	*	*	**0**	**0**	*	*

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	**P42MD0**	P41MD0	P40MD0
value	*	*	*	*	**1**	**1**	*	*

The state of the P43 pin is selected as CMOS output mode by setting P43C1 bit (P4CON1 register:bit3) to "1", setting P43C0 bit (P4CON0 register:bit3) to "1" and setting P43DIR bit (P4DIR register:bit3) to "0". The P42 pin is selected as input pin by setting P42DIR bit (P4DIR register: bit2) to "1".
The setting value of P42C1 bit and P42C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P42 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	**P42C1**	P41C1	P40C1
value	*	*	*	*	**1**	**$**	*	*

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	**P42C0**	P41C0	P40C0
value	*	*	*	*	**1**	**$**	*	*

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	**P43 DIR**	**P42 DIR**	P41 DIR	P40 DIR
value	*	*	*	*	**0**	**1**	*	*

As for P43D-P42D bit (P4D register:bit3-2), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	P47 D	P46 D	P45 D	P44 D	**P43 D**	**P42 D**	P41 D	P40 D
value	*	*	*	*	**	**	*	*

* : no relation to the UART function **: Don't care $: Optional
Note:
Receiving pin (RXD) is selected by U0RSEL bit (bit 4) of UA0MOD0 register. The P02 pin is selected by initial value"0" and the P42 pin is selected by "1.". Even if P42 port are chosen RXD0 by P42MD1, P42MD0, P42C1, P42C0, setting of P42DIR, if the U0RSEL bit of the UA0MOD0 register is setting"0", P02 port are chosen by RXD0.

12.4.2 When operating the UART function using P43 pin (TXD0:output) and P02 pin (RDX0:input)

The UART is selected as the secondary function of the P43 pin by setting P43MD1 bit (P4MOD1 register: bit3) to "0" and setting P43MD0 bit (P4MOD0 register: bit3) to "1".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
value	*	*	*	*	**0**	$	*	*

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
value	*	*	*	*	**1**	$	*	*

The state of the P43 pin is selected as CMOS output mode by setting P43C1 bit (P4CON1 register:bit3) to "1", setting P43C0 bit (P4CON0 register:bit3) to "1" and setting P43DIR bit (P4DIR register:bit3) to "0".

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
value	*	*	*	*	**1**	*	*	*

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
value	*	*	*	*	**1**	*	*	*

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	**P43 DIR**	P42 DIR	P41 DIR	P40 DIR
value	*	*	*	*	**0**	*	*	*

As for P43D bit (P4D register:bit3), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 D	P46 D	P45 D	P44 D	**P43 D**	P42 D	P41 D	P40 D
value	*	*	*	*	**	*	*	*

The P02 pin does not require input/output selection by the register, since it is only for an input.
The setting value of P02C1 bit and P02C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P02 pin is connected.

register	P0CON1 register (Address:0F207H)							
bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	P03C1	**P02C1**	P01C1	P00C1
value	-	-	-	-	*	**$**	*	*

register	P0CON0 register (Address:0F206H)							
bit	7	6	5	4	3	**2**	1	0
bit name	-	-	-	-	P03C0	**P02C0**	P01C0	P00C0
value	-	-	-	-	*	**$**	*	*

As for P02D bit (P0D register:bit2), neither "0" nor "1" is problematic.

register	P0D register (Address:0F204H)							
bit	7	6	5	4	3	**2**	1	0
bit name	-	-	-	-	P03D	**P02D**	P01D	P00D
value	-	-	-	-	*	**	*	*

- : not exist
* : no relation to the UART function
**: Don't care
$: Optional

Note:
• The P02 pin has neither the register which selects the input/output direction, nor the register which selects the modes, such as the secondary function.

12.4.3 When operating the UART function using P53 pin (TXD1:output) and P52 pin (RDX1:input)

The UART is selected as the secondary function of the P53 pin and the P52 pin by setting P53MD1-P52MD1 bit (P5MOD1 register: bit3-2) to "0" and setting P53MD0-P52MD0 bit (P5MOD0 register: bit3-2) to "1".

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53MD1**	**P52MD1**	P51MD1	P50MD1
value	-	-	-	-	**0**	**0**	*	*

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53MD0**	**P52MD0**	P51MD0	P50MD0
value	-	-	-	-	**1**	**1**	*	*

The state of the P53 pin is selected as CMOS output mode by setting P53C1 bit (P5CON1 register:bit3) to "1", setting P53C0 bit (P5CON0 register:bit3) to "1" and setting P53DIR bit (P5DIR register:bit3) to "0". The P52 pin is selected as input pin by setting P52DIR bit (P5DIR register: bit2) to "1".
The setting value of P52C1 bit and P52C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P52 pin is connected.

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53C1**	**P52C1**	P51C1	P50C1
value	-	-	-	-	**1**	**$**	*	*

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53C0**	**P52C0**	P51C0	P50C0
value	-	-	-	-	**1**	**$**	*	*

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53DIR**	**P52DIR**	P51DIR	P50DIR
value	-	-	-	-	**0**	**1**	*	*

As for P53D-P52D bit (P5D register:bit3-2), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53D**	**P52D**	P51D	P50D
value	-	-	-	-	******	******	*	*

* : no relation to the UART function **: Don't care $: Optional

Note:
Receiving pin (RXD) is selected by U1RSEL bit (bit 4) of UA1MOD0 register. The P03 pin is selected by initial value"0" and the P53 pin is selected by "1." Even if P52 port are chosen RXD0 by P52MD1, P52MD0, P52C1, P52C0, setting of P52DIR, if the U1RSEL bit of the UA1MOD0 register is setting"0", P03 port are chosen by RXD1.

12.4.4 When operating the UART function using P53 pin (TXD1:output) and P03 pin (RXD1:input)

The UART is selected as the secondary function of the P53 pin by setting P53MD0 bit (P5MOD0 register: bit3) to "0" and setting P53MD0 bit (P5MOD0 register: bit3) to "1".

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53MD1**	P52MD1	P51MD1	P50MD1
value	-	-	-	-	**0**	*	*	*

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53MD0**	P52MD0	P51MD0	P50MD0
value	-	-	-	-	**1**	*	*	*

The state of the P53 pin is selected as CMOS output mode by setting P53C1 bit (P5CON1 register:bit3) to "1", setting P53C0 bit (P5CON0 register:bit3) to "1" and setting P53DIR bit (P5DIR register:bit3) to "0".

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53C1**	P52C1	P51C1	P50C1
value	-	-	-	-	**1**	*	*	*

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53C0**	P52C0	P51C0	P50C0
value	-	-	-	-	**1**	*	*	*

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53DIR**	P52DIR	P51DIR	P50DIR
value	-	-	-	-	**0**	*	*	*

As for P53D bit (P5D register:bit3), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P53D**	P52D	P51D	P50D
value	-	-	-	-	******	*****	*	*

* : no relation to the UART function **: Don't care $: Optional

The P03 pin does not require input/output selection by the register, since it is only for an input.
The setting value of P03C1 bit and P03C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P03 pin is connected.

register	P0CON1 register (Address:0F207H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P03C1**	P02C1	P01C1	P00C1
value	-	-	-	-	**$**	*	*	*

register	P0CON0 register (Address:0F206H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P03C0**	P02C0	P01C1	P00C1
value	-	-	-	-	**$**	*	*	*

As for P02D bit (P0D register:bit2), neither "0" nor "1" is problematic.

register	P0D register (Address:0F204H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	**P03D**	P02D	P01C1	P00C1
value	-	-	-	-	******	*****	*	*

- : not exist
* : no relation to the UART function
**: Don't care
$: Optional

Note:
• The P03 pin has neither the register which selects the input/output direction, nor the register which selects the modes, such as the secondary function.

12.4.5 When operating the UART function using P53 pin (TXD0:output) and P42 pin (RDX0:input)

The UART is selected as the fourthly function of the P53 pin by setting P53MD1 bit (P5MOD1 register: bit3) to "1" and setting P53MD0 (P5MOD0 register: bit3) to "1".

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53MD1**	P52MD1	P51MD1	P50MD1
value	-	-	-	-	**1**	$	*	*

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53MD0**	P52MD0	P51MD0	P50MD0
value	-	-	-	-	**1**	$	*	*

The state of the P53 pin is selected as CMOS output mode by setting P53C1 bit (P5CON1 register:bit3) to "1", setting P53C0 bit (P5CON0 register:bit3) to "1" and setting P53DIR bit (P5DIR register:bit3) to "0".

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53C1**	P52C1	P51C1	P50C1
value	-	-	-	-	**1**	*-	*	*

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53C0**	P52C0	P51C0	P50C0
value	-	-	-	-	**1**	*-	*	*

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53 DIR**	P52 DIR	P51 DIR	P50 DIR
value	-	-	-	-	**0**	*-	*	*

As for P53D bit (P5D register:bit3), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	**3**	**2**	1	0
bit name	-	-	-	-	**P53 D**	P52 D -	P51 D	P50 D
value	-	-	-	-	**	*-	*	*

The UART is selected as the fourthly function of the P42 pin by setting P42MD1 bit (P4MOD1 register: bit2,) to "0" and setting P42MD0 bit (P4MOD0 register: bit2) to "1"

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	P41MD1	P40MD1
value	*	*	*	*	*	**0**	*	*

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	P41MD0	P40MD0
value	*	*	*	*	*	**1**	*	*

The state of the P42 pin is selected as CMOS output mode by setting P42C1 bit (P4CON1 register:bit2) to "1", setting P42C0 bit (P4CON0 register:bit2) to "1" and setting P42DIR bit (P4DIR register:bit2) to "0".

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	P41C1	P40C1
value	*	*	*	*	*	**$**	*	*

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C0	P46C0	P451C0	P44C0	P43C0	**P42C0**	P41C0	P40C0
value	*	*	*	*	*	**$**	*	*

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	P43 DIR	**P42 DIR**	P41 DIR	P40 DIR
value	*	*	*	*	*	**1**	*	*

As for P42D bit (P4D register:bit2), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 D	P46 D	P45 D	P44 D	P43 D	**P42 D**	P41 D	P40 D
value	*	*	*	*	*	**	*	*

* : no relation to the UART function **: Don't care $: Optional

12.4.6 When operating the UART function using P43 pin (TXD1:output) and P52 pin (RDX2:input)

The UART is selected as the fourthly function of the P43 pin by setting P43MD1 bit (P4MOD1 register: bit3) to "1" and setting P43MD0 bit (P4MOD0 register: bit3) to "1".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
value	*	*	*	*	**1**	$	*	*

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
value	*	*	*	*	**1**	$	*	*

The state of the P43 pin is selected as CMOS output mode by setting P43C1 bit (P4CON1 register:bit3) to "1", setting P43C0 bit (P4CON0 register:bit3) to "1" and setting P43DIR bit (P4DIR register:bit3) to "0".

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
value	*	*	*	*	**1**	*	*	*

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47C0	P46C0	P451C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
value	*	*	*	*	**1**	*	*	*

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 DIR	P46 DIR	P45 DIR	P44 DIR	**P43 DIR**	P42 DIR	P41 DIR	P40 DIR
value	*	*	*	*	**0**	*	*	*

As for P43D bit (P4D register:bit3), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	**3**	2	1	0
bit name	P47 D	P46 D	P45 D	P44 D	**P43 D**	P42 D	P41 D	P40 D
value	*	*	*	*	**	*	*	*

- : not exist
* : no relation to the UART function
**: Don't care
$: Optional

The UART is selected as the fourthly function of the P52 pin by setting P52MD1 bit (P5MOD1 register: bit2,) to "0" and setting P52MD0 bit (P5MOD0 register: bit2) to "1"

register	P5MOD1 register (Address:0F22DH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53MD1	**P52MD1**	P51MD1	P50MD1
value	-	-	-	-	*	**0**	*	*

register	P5MOD0 register (Address:0F22CH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53MD0	**P52MD0**	P51MD0	P50MD0
value	-	-	-	-	*	**1**	*	*

The state of the P52 pin is selected as CMOS output mode by setting P52C1 bit (P5CON1 register:bit2) to "1", setting P52C0 bit (P5CON0 register:bit2) to "1" and setting P52DIR bit (P5DIR register:bit2) to "0".

register	P5CON1 register (Address:0F22BH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53C1	**P52C1**	P51C1	P50C1
value	-	-	-	-	*	**$**	*	*

register	P5CON0 register (Address:0F22AH)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53C0	**P52C0**	P51C0	P50C0
value	-	-	-	-	*	**$**	*	*

register	P5DIR register (Address:0F229H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53 DIR	**P52 DIR**	P51 DIR	P50 DIR
value	-	-	-	-	*	**1**	*	*

As for P52D bit (P5D register:bit2), neither "0" nor "1" is problematic.

register	P5D register (Address:0F228H)							
bit	7	6	5	4	**3**	2	1	0
bit name	-	-	-	-	P53 D	**P52 D**	P51 D	P50 D
value	-	-	-	-	*	**	*	*

- : not exist
* : no relation to the UART function
**: Don't care
$: Optional

Chapter 13

I^2C Bus Interface

13. I2C Bus Interface

13.1 Overview

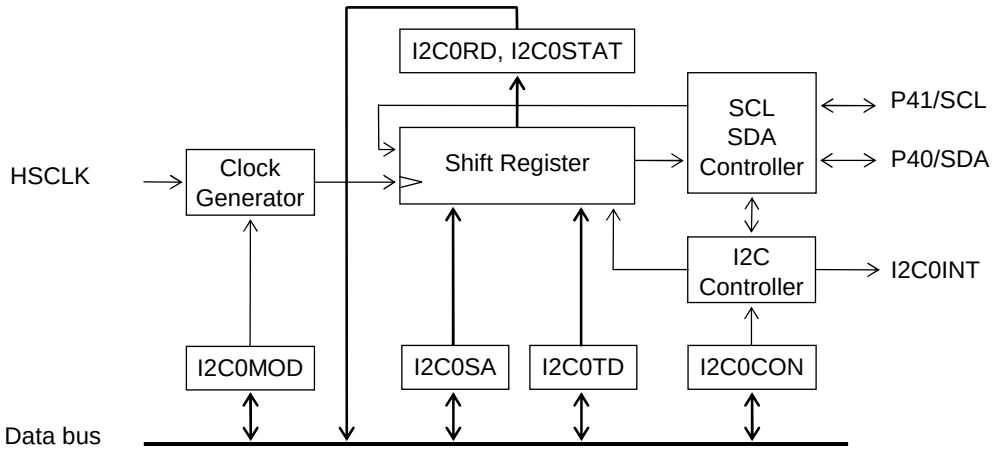
This LSI includes 1 channel of I²C bus interface (master).
The secondary functions of Port 4 are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For Port4, see Chapter 19, "Port 4".

13.1.1 Features

- Master function
- Communication speeds supported include standard mode (100 kbps@4MHz HSCLK) and fast mode (400kbps@4 MHz HSCLK).
- Allows support for arbitration function (multi-master) and clock synchronization (handshake).
- 7-bit address format (10-bit address can be supported)

13.1.2 Configuration

Figure 13-1 shows the configuration of the I²C bus interface.



I2C0RD : I²C bus 0 receive register
I2C0SA : I²C bus 0 slave address register
I2C0TD : I²C bus 0 transmit data register
I2C0CON : I²C bus 0 control register
I2C0MOD : I²C bus 0 mode register
I2C0STAT : I²C bus 0 status register

Figure 13-1 Configuration of I²C Bus Interface

13.1.3 List of Pins

Pin name	I/O	Description
P40/SDA	I/O	I²C bus interface data input/output pin. Used for the secondary function of the P40 pin.
P41/SCL	I/O	I²C bus interface clock input/output pin. Used for the secondary function of the P41 pin.

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A0H	I^2C bus 0 receive register	I2C0RD	—	R	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H

13.2.2 I²C Bus 0 Receive Register (I2C0RD)

Address: 0F2A0H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0RD	I20R7	I20R6	I20R5	I20R4	I20R3	I20R2	I20R1	I20R0
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0RD is a read-only special function register (SFR) to store receive data.
I2C0RD is updated after completion of each reception.

[Description of Bits]

- **I20R7-I20R0** (bits 7-0)
  The I20R7 to I20R0 bits are used to store receive data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

13.2.3 I²C Bus 0 Slave Address Register (I2C0SA)

Address: 0F2A1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0SA	I20A6	I20A5	I20A4	I20A3	I20A2	I20A1	I20A0	I20RW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

- **I20RW** (bit 0)
  The I20RW bit is used to select the data transmit mode (write) or data receive mode (read).

I20RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

- **I20A6-I20A0** (bits 7-1)
  The I20A6 to I20A0 bits are used to set the address of the communication destination.

13.2.4 I²C Bus 0 Transmit Data Register (I2C0TD)

Address: 0F2A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0TD	I20T7	I20T6	I20T5	I20T4	I20T3	I20T2	I20T1	I20T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0TD is a special function register (SFR) to set transmit data.

[Description of Bits]

- **I20T7-0** (bits 7-0)
  The I20T7 to 0 bits are used to set transmit data.

13.2.5 I²C Bus 0 Control Register (I2C0CON)

Address: 0F2A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0CON	I20ACT	—	—	—	—	I20RS	I20SP	I20ST
R/W	R/W	R/W	R/W	R/W	R/W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I20ST** (bit 0)
  The I20ST bit is used to control the communication operation of the I²C bus interface. When the I20ST bit is set to "1", communication starts. When "1" is overwritten to the I20ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication starts again. When the I20ST bit is set to "0", communication is stopped forcibly.
  The I20ST bit can be set to "1" only when the I2C bus interface is in an operation enable state (I20EN = "1").
  When the I20SP bit is set to "1", the I20ST bit is set to "0".

I20ST	Description
0	Stops communication (initial value)
1	Starts communication

- **I20SP** (bit 1)
  The I20SP bit is a write-only bit used to request a stop condition. When the I20SP bit is set to "1", the I²C bus shifts to the stop condition and communication stops. When the I20SP bit is read, "0" is always read.

I20SP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I20RS** (bit 2)
  The I20RS bit is a write-only bit used to request a repeated start. When this bit is set to "1" during data communication, the I²C bus shifts to the repeated start condition and communication restarts from the slave address. I20RS can be set to "1" only while communication is active (I20ST ="1"). When the I20RS bit is read, "0" is always read.

I20RS	Description
0	No repeated start request (initial value)
1	Repeated start request

- **I20ACT** (bit 7)
  The I20ACT bit is used to set the acknowledge signal to be output at completion of reception.

I20ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

[Note]
When another master is connected to the I2C-bus, please check the bus is free with the I20BB flag of I2C0STAT before starting communication.

13.2.6 I²C Bus 0 Mode Register (I2C0MOD)

Address: 0F2A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0MOD	—	—	—	I20SYN	I20DW1	I20DW0	I20MD	I20EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

- **I20EN** (bit 0)
  The I20EN bit is used to enable the operation of the I²C bus interface. Only when the I20EN bit is set to "1", the I20ST bit can be set and the I20BB flag starts operation. When the I20EN bit is set to "0", all the SFRs related to the I²C bus 0 are initialized.

I20EN	Description
0	Stops I²C operation. (Initial value)
1	Enables I²C operation.

- **I20MD** (bit 1)
  The I20MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected.

I20MD	Description
0	Standard mode (initial value)/ 100kbps@4MHz HSCLK
1	Fast mode / Max. 400kbps@4MHz HSCLK

- **I20DW1, I20DW0** (bits 3, 2)
  The I20DW1 and I20DW0 bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kpbs/400kpbs.

I20DW1	I20DW0	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

- **I20SYN** (bit 4)
  The I20SYN bit is used to select whether or not to use the clock synchronization function (handshake function). When using the clock synchronization function or using a multi-master, set this bit to "1"

I20SYN	Description
0	Clock synchronization is not used. (Initial value)
1	Clock synchronization is used.

Note:
The I²C bus is set so that the communication speed may become 100kbps/400kbps when HSCLK is 4 MHz.

13.2.7 I²C Bus 0 Status Register (I2C0STAT)

Address: 0F2A5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0STAT	—	—	—	—	—	I20ER	I20ACR	I20BB
R	R	R	R	R	R	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C0STAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

[Description of Bits]

- I20BB (bit 0)
  The I20BB bit is used to indicate the state of use of the I²C bus interface. When the start condition is generated on the I²C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". In multi-master mode, this bit is set to "1" even if another master device is using the I²C bus. The I20BB bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20BB	Description
0	I²C bus-free state (Initial value)
1	I²C bus-busy state

- **I20ACR** (bit 1)
  The I20ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I20ACR bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

- **I20ER** (bit 2)
  The I20ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". When clock synchronization is used (I20SYN = "1"), if the I20ER bit is set to "1", the SDA pin output is disabled until the subsequent byte data communication terminates. When clock synchronization is not used (I20SYN = "0"), The SDA pin remains the output until the subsequent byte data communication terminates even if I20ER is set to "1".
  The I20ER bit is set to "0" when a write operation to I2C0CON is performed. The I20ER bit is set to "0" when the I20EN bit of I2C0MOD is set to "0".

I20ER	Description
0	No transmit error (initial value)
1	Transmit error

13.3 Description of Operation

13.3.1 Communication Operating Mode

Communication is started when communication mode is selected by using the I²C bus 0 mode register (I2C0MOD), the I²C function is enabled by using the I20EN bit, a slave address and a data communication direction are set in the I²C bus 0 slave address register, and "1" is written to the I20ST bit of the I2C bus 0 control register (I2C0CON).

13.3.1.1 Start Condition

When "1" is written to the I20ST bit of the I²C bus 0 control register ((I2C0CON) while communication is stopped (the I20ST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to slave address transmit mode.

13.3.1.2 Repeated Start Condition

When "1" is written to the I20RS and I20ST bits of the I²C bus 0 control register ((I2C0CON) during communication (the I20ST bit is "0"), the repeated start condition waveform is output to the SDA and SCL pins.
After execution of the repeated start condition, the LSI shifts to slave address transmit mode.

13.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus 0 slave address register (I2C0SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0SA output from the SDA pin is stored in I2C0RD.

13.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C0TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0TD output from the SDA pin is stored in I2C0RD.

13.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I20ACT bit of the I2C bus 0 control register (I2C0CON) is output as an acknowledge signal. At completion of acknowledgment transmission, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The data received is stored in I2C0RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).

13.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I²C bus interface interrupt (I2C0INT) is generated.
In the control register setting wait state, the transmit flag (I20ER) of the I²C bus 0 status register (I2C0STAT) and acknowledgment receive data (I20ACR) are confirmed and at data reception, the contents of I2C0RD are read in the CPU and the next operation mode is selected.
When "1" is written to the I20ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I20SP bit, the LSI shifts to the stop condition. When "1" is written to the I20RS bit and I20ST bit, the operation shifts to the repeated start condition.

13.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I²C bus interface interrupt (I2C0INT) is generated.

13.3.2 Communication Operation Timing

Figures 13-2 to 13-4 show the operation timing and control method for each communication mode.

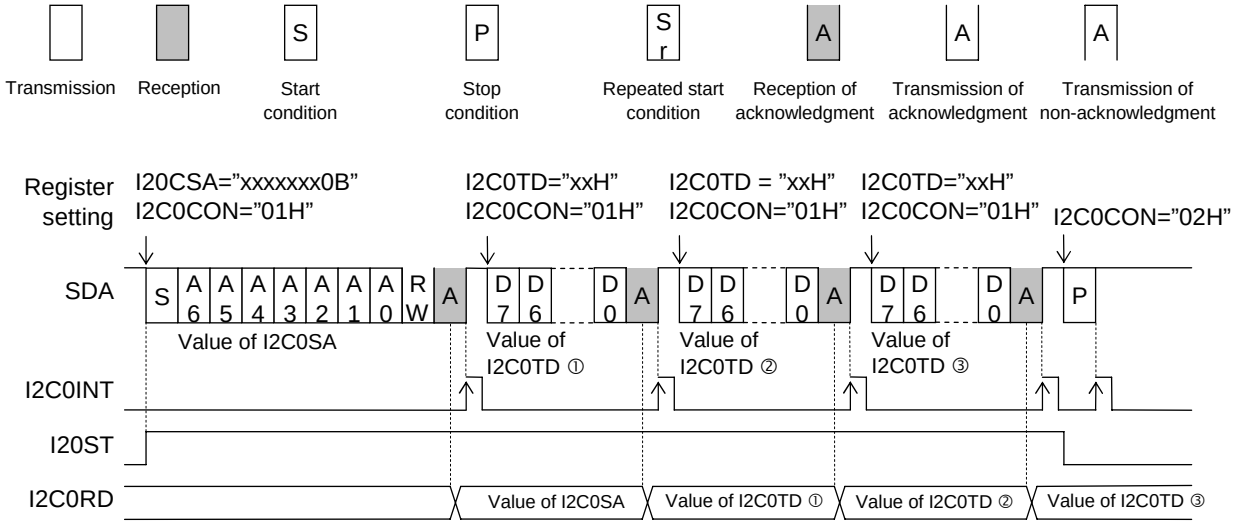


Figure 13-2 Operation Timing in Data Transmit (Write)

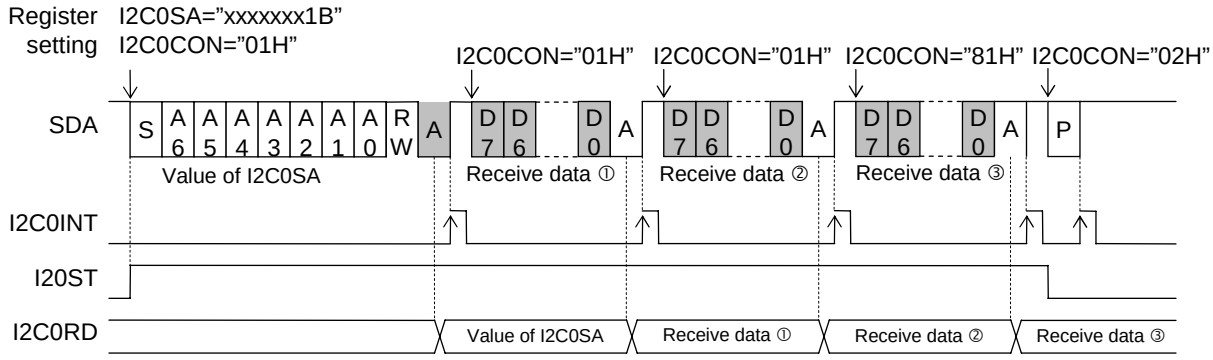


Figure 13-3 Operation Timing in Data Receive (Read)

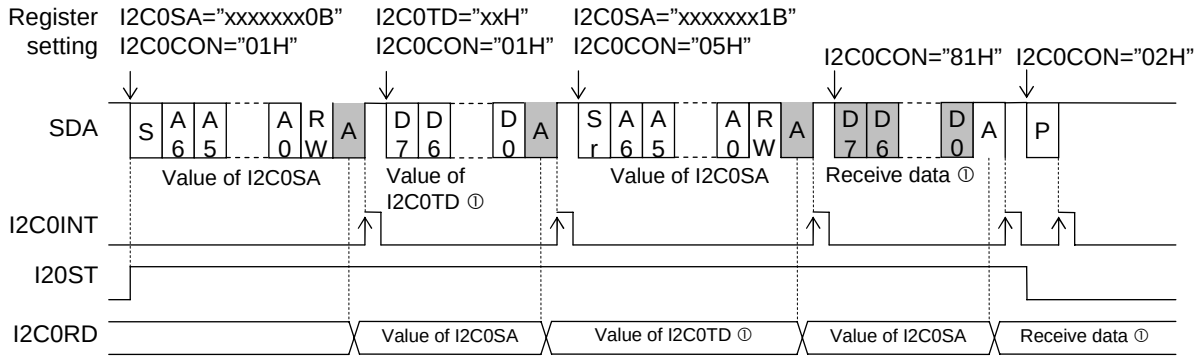


Figure 13-4 Operation Timing at Data Transmit/Receive (Write/Read) Switching

Figure 13-5 shows the operation timing and control method when an acknowledgment error occurs.

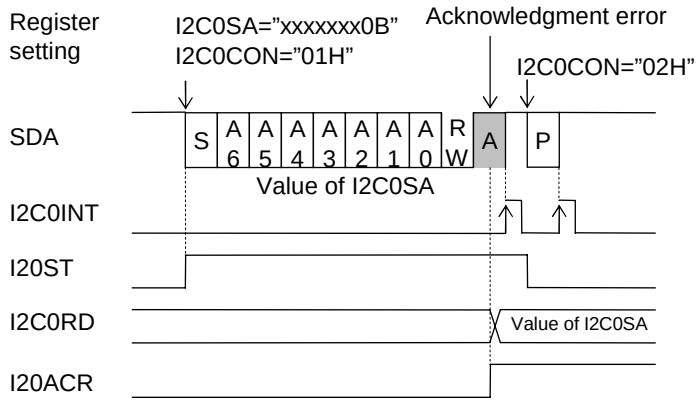


Figure 13-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide (transmit failure due to arbitration when a multi-masters is used), the I20ER bit of the I2C bus 0 status register (I2C0STAT) is set to "1" and SDA pin remains the output until termination of the subsequent byte data communication. I20ER bit is initialized to "0" by writing I²C Bus 0 Control Register (I2C0COCON).
Figure 13-6 shows the operation timing and control method when transmission fails.

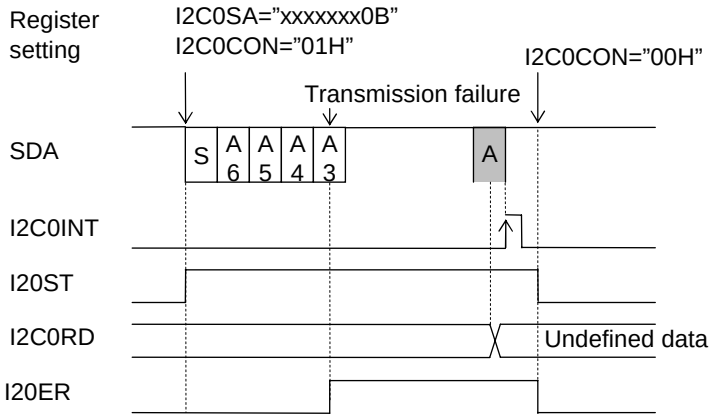


Figure 13-6 Operation Timing When Transmission Fails

13.3.3 Operation Waveforms

Figure 13-7 shows the operation waveforms of the SDA and SCL signals and the I20BB flag. Table 13-1 shows the relationship between communication speeds and HSCLK clock counts.

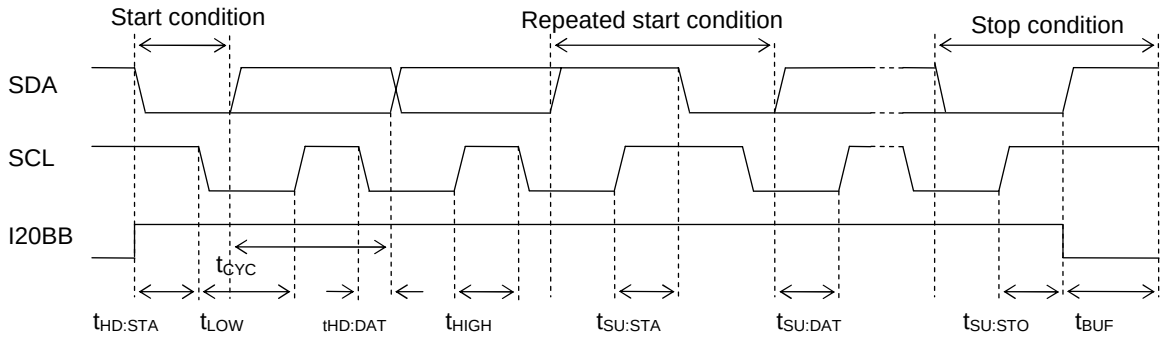


Figure 13-7 Operation Waveforms of SDA and SCL Signals and I20BB Flag

Table 13-1 Relationship between Communication Speeds and HSCLK Clock Counts

Communication speed (I20SP)	Speed reduction (I20DW1, 0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100 kbps	No reduction	80ϕ	36ϕ	44ϕ	8ϕ	36ϕ	44ϕ	36ϕ	36ϕ	44ϕ
	10% reduction	88ϕ	40ϕ	48ϕ	8ϕ	40ϕ	48ϕ	40ϕ	40ϕ	48ϕ
	20% reduction	96ϕ	44ϕ	52ϕ	8ϕ	44ϕ	52ϕ	44ϕ	44ϕ	52ϕ
	30% reduction	104ϕ	48ϕ	56ϕ	8ϕ	48ϕ	56ϕ	48ϕ	48ϕ	56ϕ
Fast mode 400 kbps	No reduction	0ϕ	8ϕ	12ϕ	4ϕ	8ϕ	12ϕ	8ϕ	8ϕ	12ϕ
	10% reduction	22ϕ	8ϕ	14ϕ	4ϕ	8ϕ	14ϕ	10ϕ	8ϕ	14ϕ
	20% reduction	24ϕ	10ϕ	14ϕ	4ϕ	10ϕ	14ϕ	10ϕ	10ϕ	14ϕ
	30% reduction	26ϕ	10ϕ	16ϕ	4ϕ	10ϕ	16ϕ	12ϕ	10ϕ	16ϕ

ϕ: Period of high-speed clock (HSCLK)

Note
The HSCLK clock count is set so that the communication speed may be set to 100kbps/400kbps when HSCLK is 4 MHz. When the high-speed clock frequency is not 4 MHz, select an I2C0MOD communication speed reduction rate and an FCON0 HSCLK frequency so that the communication speed may not exceed 100kbps/400kbps.

13.4 Specifying port registers

To enable the I²C function, the applicable bit of each related port register needs to be set. See Chapter 20, "Port 4" for detail about the port registers.

13.4.1 Functioning P41(SCL) and P40(SDA) as the I2C

Set P41MD1 to P40MD1 bit (bit1-bit0 of P4MOD0 register) to "0", and P41MD0 to P40MD0 bit (bit1-bit0 of P4MOD0 register) to "1", for specifying the I2C as the secondary function of P41 and P40.

Reg. name	P4MOD0 register (Address: 0F225H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	**P41MD1**	**P40MD1**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	**P41MD0**	**P40MD0**
Data	*	*	*	*	*	*	**1**	**1**

Set P41C1-P40C1 bit(bit1-0 of P4CON1 register) to "1", set P41C0-P40C0 bit(bit1-0 of P4CON0 register) to "0", and set P41DIR-P40DIR bit(bit1-0 of P4DIR register) to "0", for specifying the P41 and P40 as Nch open-drain output. The open-drain/open-collector outputs are required on the I2C bus line to avoid collision between H level and L level.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	**P41C1**	**P40C1**
Data	*	*	*	*	*	*	**1**	**1**

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	**P41C0**	**P40C0**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	**P41DIR**	**P40DIR**
Data	*	*	*	*	*	*	**0**	**0**

Data of P41D-P40D bits (bit1-0 of P4D register) do not affect to the I2C function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	P42D	**P41D**	**P40D**
Data	*	*	*	*	*	*	******	******

* : Bit not related to the I2C bus interface function
** : Don't care the data

Chapter 14

NMI Pin

14 NMI Pin

14.1 Overview

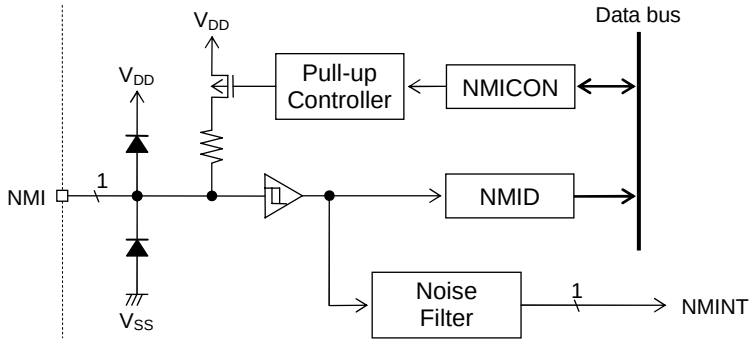
This LSI includes an input port (NMI) which generates a non-maskable interrupt.
For interrupts see Chapter 5, "Interrupts".

14.1.1 Features

- Non-maskable interrupt pin.
- Allows selection of an input with a pull-up resistor or a high-impedance input.
- Applies a noise filter to NMI interrupt (NMINT).

14.1.2 Configuration

Figure 14-1 shows the configuration of the NMI pin.



NMID : NMI data register
NMICON : NMI control register

Figure 14-1 Configuration of NMI Pin

14.1.3 List of Pins

Pin name	Input/output	Description
NMI	I	Non-maskable interrupt input port

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F200H	NMI data register	NMID	–	R	8	Depends on pin state
0F201H	NMI control register	NMICON	–	R/W	8	00H

14.2.2 NMI Data Register (NMID)

Address: 0F200H
Access: R
Access size: 8 bits
Initial value: Depends on the pin state

	7	6	5	4	3	2	1	0
NMID	—	—	—	—	—	—	—	NMI
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	x

NMID is a read-only special function register (SFR) for reading the NMI pin level.

[Description of Bits]

- **NMI**（bit 0）
  The NMI bit is used to read the level of the NMI pin.

NMI	Description
0	"0" level
1	"1" level

14.2.3 NMI Control Register (NMICON)

Address: 0F201H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
NMICON	—	—	—	—	—	—	—	NMIC
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

NMICON is a special function register (SFR) to select the input mode of the NMI pin.

[Description of Bits]

- **NMIC** (bit 0)
  The NMIC bit is used to select the input mode with or without a pull-up resistor.

NMIC	Description
0	Input mode with a pull-up resistor (initial value)
1	High-impedance input mode

Note:
Do not choose high impedance input mode in an open state.

14.3 Description of Operation

The non-maskable NMI interrupt (NMIINT) is assigned to the NMI pin.
The NMI pin allows selection of an input mode with a pull-up resistor or a high-impedance input mode by using the NMI control register (NMICON). At a system reset, the input mode with a pull-up resistor is selected.
The level of the NMI pin can be read by reading the NMI data register (NMID).

14.3.1 Interrupt Request

When a level change occurs at the NMI pin after the duration longer than the minimum NMI interrupt pulse width, a non-maskable interrupt which does not depend on the master interrupt enable flag (MIE) is generated.
Figure 14-2 shows the NMI interrupt generation timing.

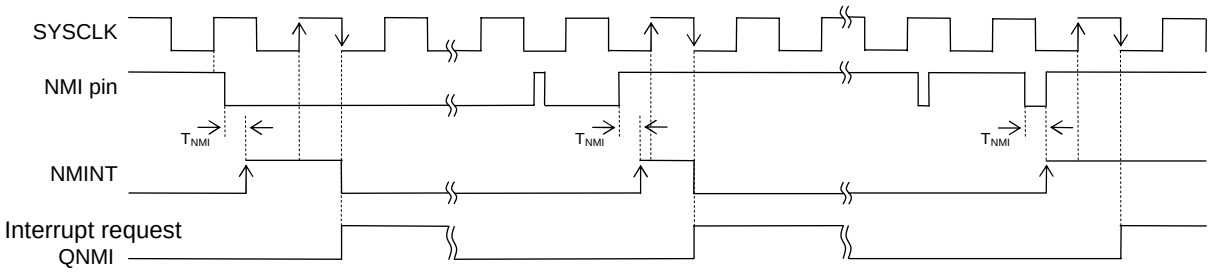


Figure 14-2 NMI Interrupt Generation Timing

Chapter 15

Port 0

15. Port 0

15.1 Overview

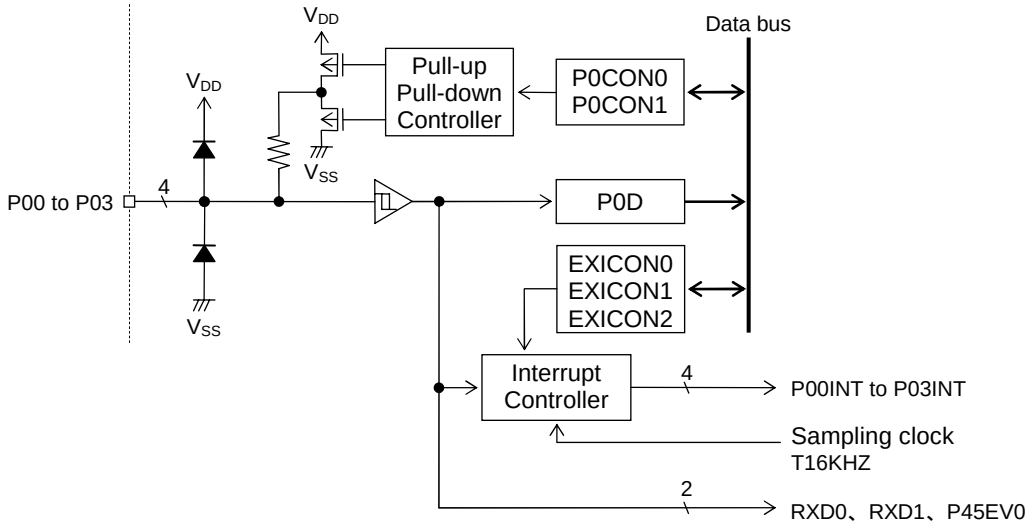
This LSI includes Port 0 (P00 to P03) which is a 4-bit input port.

15.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ)
- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- The P02 pin can be used as the RXD0 input pin of UART0.
- The P03 pin can be used as the RXD1 input pin of UART1
- The P00 pin can be used as the P45EV0 input pin of PWM

15.1.2 Configuration

Figure 15-1 shows the configuration of Port 0.



P0D	: Port 0 data register
P0CON0	: Port 0 control register 0
P0CON1	: Port 0 control register 1
EXICON0	: External interrupt control register 0
EXICON1	: External interrupt control register 1
EXICON2	: External interrupt control register 2

Figure 15-1 Configuration of Port 0

15.1.3 List of Pins

Pin name	I/O	Description
P00/EXI0/ P45EV0	I	Input port, External 0 interrupt, P45EV0 input
P00/EXI1	I	Input port, External 1 interrupt
P02/EXI2/RXD0/	I	Input port, External 2 interrupt, UART0 data input（RXD0）
P03/EXI3/RXD1	I	Input port, External 3 interrupt, UART1 data input (RXD1)

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F204H	Port 0 data register	P0D	—	R	8	Depends on pin status
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	—	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	—	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	—	R/W	8	00H

15.2.2 Port 0 Data Register (P0D)

Address: 0F204H
Access: R
Access size: 8 bits
Initial value: Depends on pin status

	7	6	5	4	3	2	1	0
P0D	—	—	—	—	P03D	P02D	P01D	P00D
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	x	x	x	x

P0D is a special function register (SFR) to only read the pin level of Port 0.

[Description of Bits]

- **P03D to P00D** (bits 3 to 0)
  The P03D to P00D bits are used to read the pin level of Port 0.

P00D	Description
0	P00 pin input: "L" level
1	P00 pin input: "H" level

P01D	Description
0	P01 pin input: "L" level
1	P01 pin input: "H" level

P02D	Description
0	P02 pin input: "L" level
1	P02 pin input: "H" level

P03D	Description
0	P03 pin input: "L" level
1	P03 pin input: "H" level

15.2.3 Port 0 Control Registers 0, 1 (P0CON0, P0CON1)

Address: 0F206H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON0	—	—	—	—	P03C0	P02C0	P01C0	P00C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F207H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	—	P03C1	P02C1	P01C1	P00C1
R/W	R	R	R/	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0CON0 and P0CON1 are special function registers (SFRs) to select the input mode of Port 0.

[Description of Bits]

- **P03C0 to P00C0, P03C1 to P00C1** (bits 3 to 0)
  The P03C0 to P00C0 bits and the P03C1 to P00C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. The P0nC0 bit and the P0nC1 bit determine the input mode of P0n (Example: When P02C0 = "0" and P02C1 = "1", P02 is in input mode with a pull-up resistor).

P03C1 to P00C1	P03C0 to P00C0	Description
0	0	High-impedance input mode (initial value)
0	1	Input mode with a pull-down resistor
1	0	Input mode with a pull-up resistor
1	1	High-impedance input mode

15.2.4 External Interrupt Control Registers 0, 1 (EXICON0, EXICON1)

Address: 0F020H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON0	—	—	—	—	P03E0	P02E0	P01E0	P00E0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F021H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON1	—	—	—	—	P03E1	P02E1	P01E1	P00E0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON0 and EXICON1 are special function registers (SFRs) to select an interrupt edge of Port 0.

[Description of Bits]

- **P03E0 to P00E0, P03E1 to P00E1** (bits 3 to 0)
  The P03E0 to P00E0 bits and the P03E1 to P00E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P0nE0 bit and the P0nE1 bit determine the interrupt mode of P0n (Example: When P02E0 = "0" and P02E1 = "1", P02 is in rising-edge interrupt mode).

P03E1 to P00E1	P03E0 to P00E0	Description
0	0	Interrupt disabled mode (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

15.2.5 External Interrupt Control Register 2 (EXICON2)

Address: 0F022H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON2	—	—	—	—	P03SM	P02SM	P01SM	P00SM
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON2 is a special function register (SFR) to select detection of signal edge for interrupts with or without sampling.

[Description of Bits]

- **P03SM to P00SM** (bits 3 to 0)
  The P03SM to P00SM bits are used to select detection of signal edge for Port 0 interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P00SM	Description
0	Detects the input signal edge for a P00 interrupt without sampling (initial value).
1	Detects with a sampling.

P01SM	Description
0	Detects the input signal edge for a P01 interrupt without sampling (initial value).
1	Detects with a sampling.

P02SM	Description
0	Detects the input signal edge for a P02 interrupt without sampling (initial value).
1	Detects with a sampling.

P03SM	Description
0	Detects the input signal edge for a P03 interrupt without sampling (initial value).
1	Detects with a sampling.

Note:
In STOP mode, since the T16KHZ sampling clock stops, no sampling is performed regardless of the values set in P03SM to P00SM.

15.3 Description of Operation

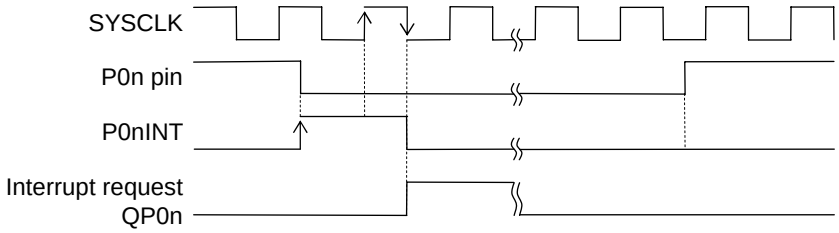
For each pin of Port 0, the setting of the Port 0 control registers 0 and 1 (P0CON0 and P0CON1) allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. High-impedance input mode is selected at system reset.
The pin level of Port 0 can be read by reading the Port 0 data register (P0D).

15.3.1 External Interrupt

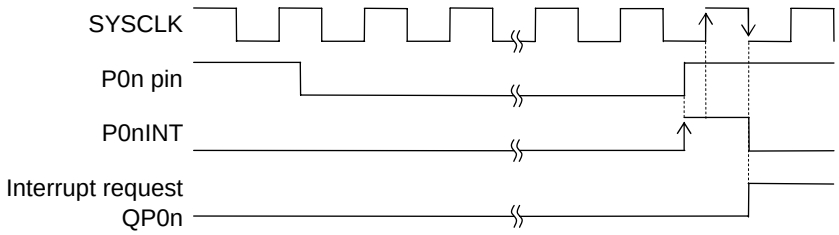
The Port 0 pins (P00 to P03) can be used for P00 to P03 interrupts (P00INT to P03INT). The P00 to P03 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupts".
The P00 can be used for P45EV0 input pin, the P02 can be used for RXD0/2 of UART0/2, the P03 can be used for RXD1 of UART1 For details of PWM, see Chapter 10, "PWM", for detail of UART, see Chapter 12, "UART".

15.3.2 Interrupt Request

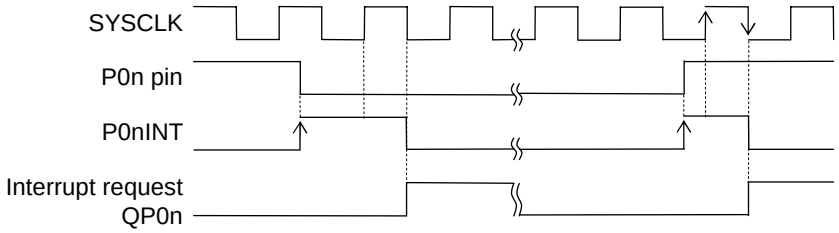
When an interrupt edge selected by the external interrupt control registers 0, 1, 2 (EXICON0, EXICON1, EXICON2) occurs at a Port 0 pin, the corresponding maskable Pxx (P00 to P03) interrupt (P00INT–P03INT) occurs.
Figure 15-2 shows the P00–P03 interrupt generation timing in rising-edge interrupt mode, falling-edge interrupt mode, and both-edges interrupt mode, each without sampling, and the P00 to P03 interrupt generation timing in rising-edge interrupt mode with sampling.



(a) When "falling-edge interrupt; without sampling" is selected

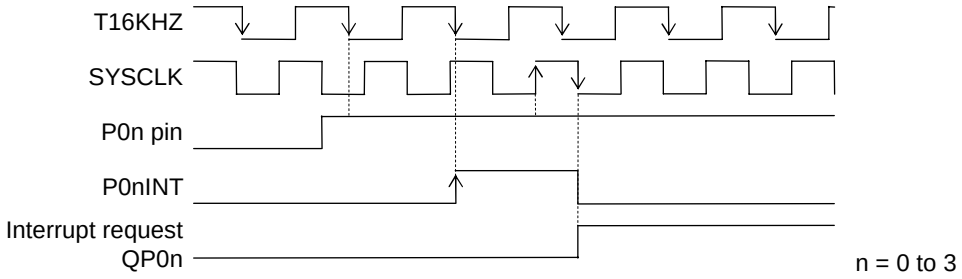


(b) When "rising-edge interrupt; without sampling" is selected



(c) When "both-edges interrupt; without sampling" is selected

When "rising-edge interrupt; with sampling" is selected, The input level of P0n pins are checked by a T16kHz negative going edge. An interrupt condition will be satisfied if an input level is "H" consecutive two times.
An interrupt request occurs to the timing of the SYSCLK negative going edge after the 2nd T16kHz negative going edge.



(d) When "rising-edge interrupt; with sampling" is selected

Figure 15-2 P00 to P03 Interrupt Generation Timing

Chapter 16

Port 1

16. Port 1

16.1 Overview

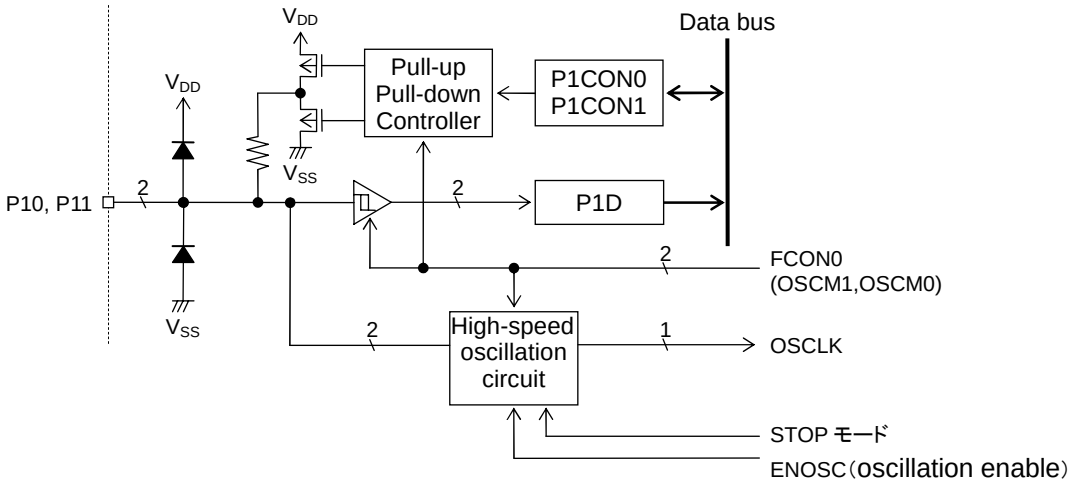
This LSI incorporates a 2-bit input port, Port 1 (P10, P11).
Port 1 can have a high-speed oscillation pin or an external clock input pin, which is selected by mask option. When the port is used as an external clock input pin, the P11 pin functions as an input pin.
For high-speed oscillation and external clock input, see Chapter 6, "Clock Generation Circuit".

16.1.1 Features

- High-impedance input, input with a pull-down resistor, or input with a pull-up resistor can be selected for each bit.
- A high-speed crystal/ceramic oscillation pin or an external clock input pin can be selected by mask option.

16.1.2 Configuration

Figure 16-1 shows the configuration of Port 1.



P1D : Port 1 data register
P1CON0 : Port 1 control register 0
P1CON1 : Port 1 control register 1

Figure 16-1 Configuration of Port 1

16.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P10/OSC0	I	Input port	High-speed crystal/ceramic oscillation pin, external clock input pin
P11/OSC1	I/O	Input port	High-speed crystal/ceramic oscillation pin

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F208H	Port 1 data register	P1D	—	R	8	Depends on pin status
0F20AH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	00H
0F20BH	Port 1 control register 1	P1CON1		R/W	8	00H

16.2.2 Port 1 Data Register (P1D)

Address: 0F208H
Access: R
Access size: 8 bits
Initial value: Depends on pin status

	7	6	5	4	3	2	1	0
P1D	—	—	—	—	—	—	P11D	P10D
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	x	x

P1D is a special function register (SFR) dedicated to read the input level of the Port 1 pin.

[Description of Bits]

- **P11D, P10D** (bit 1,0)
  The P11D, P10D bit is used to read the input level of the Port 1 pin.

P11D	Description
0	Input level of the P11 pin: "L"
1	Input level of the P11 pin: "H"

P10D	Description
0	Input level of the P10 pin: "L"
1	Input level of the P10 pin: "H"

16.2.3 Port 1 Control Registers 0,1 (P1CON0, P1CON1)

Address: 0F20AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P1CON0	—	—	—	—	—	—	P11C0	P10C0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F20BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	—	—	—	P11C1	P10C1
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P1CON0 and P1CON1 are special function registers (SFRs) to select the input mode of Port 1.

[Description of Bits]

- **P11C0, P10C0, P11C1, P00C1** (bit 1 to 0)
  These bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.

P11C1	P11C0	Description
0	0	P11 pin: high-impedance input mode (initial value)
0	1	P11 pin: input mode with a pull-down resistor
1	0	P11 pin: input mode with a pull-up resistor
1	1	P11 pin: high-impedance input mode

P10C1	P10C0	Description
0	0	P10 pin: high-impedance input mode (initial value)
0	1	P10 pin: input mode with a pull-down resistor
1	0	P10 pin: input mode with a pull-up resistor
1	1	P10 pin: high-impedance input mode

Note:
When using P10 and P11 as crystal / a ceramic oscillation pin, be sure to set P10 and P11 pin as a high impedance input. When using P10 pin as an external clock input pin, please set P10 terminal as a high impedance input so that current does not flow into pull-up resistance or pulldown resistance.

16.3 Description of Operation

16.3.1 Input Port Function

For each pin of Port 1, one of high-impedance input mode, input mode with a pull-down resistor, and input mode with a pull-up resistor can be selected by setting the Port 1 control registers 0 and 1 (P1CON0 and P1CON1). At system reset, high-impedance input mode is selected as the initial state.
The input level of the Port 1 pin can be read by reading the Port 1 data register (P1D).

16.3.2 Secondary function

High-speed crystal / ceramic oscillation pin, or the external clock input pin is assigned to the port 1 as a secondary function.
Crystal / ceramic oscillation mode, or an external clock input mode can be selected by the OSCM1,0 bit of the frequency control register 0 (FCON0).
In crystal / ceramic oscillation mode, both P10 and P11 pin are used as a pin crystal / for a ceramic oscillation.
In an external clock input mode, P10 pin is used as an input pin of an external clock, and P11 can be used as a general-purpose input port.

Note:
There is no port mode register for changing the primary function and secondary function of a port 1.
When using it as a high-speed oscillation pin, pin mode changes according to the preset value of the OSCM1, OSCM0 bit of FCON0 register.
Refer to Chapter 6, "Clock Generation Circuit " for details of the FCON0 register, and a high-speed oscillation and an external clock input.

Chapter 17

Port 2

17. Port 2

17.1 Overview

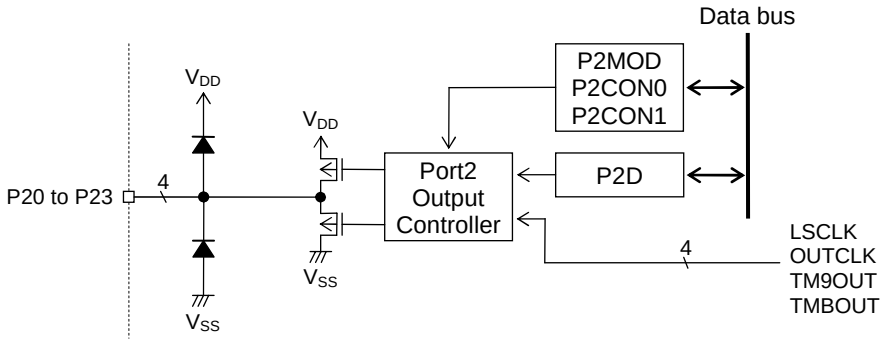
This LSI incorporates Port 2 (P20–P23), a 4-bit port for output only.
Port 2 can output low-speed clock (LSCLK), high-speed clock (OUTCLK), Timer 9 out (TM9OUT) or TimerB out (TMBOUT) as its secondary functions. For clock output, see Chapter 6, "Clock Generation Circuit".

17.1.1 Features

- Allows direct LED drive.
- High-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output can be selected for each bit.
- Allows output of low-speed clock (LSCLK), high-speed clock (OUTCLK), Timer 9 out (TM9OUT) or TimerB out (TMBOUT) as secondary functions.
- Operates as an LED drive port, when a general-purpose output port function is chosen.

17.1.2 Configuration

Figure 17-1 shows the configuration of Port 2.



P2D : Port 2 data register
P2CON0 : Port 2 control register 0
P2CON1 : Port 2 control register 1
P2MOD : Port 2 mode register

Figure 17-1 Configuration of Port 2

17.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P20/LED0/LSCLK	O	Output port, Direct LED drive	Low-speed clock output (LSCLK)
P21/LED1/OUTCLK	O	Output port, Direct LED drive	High-speed clock output (OUTCLK)
P22/LED2/TM9OUT	O	Output port, Direct LED drive	Timer 9 out (TM9OUT)
P23/LED3/TMBOUT	O	Output port, Direct LED drive	Timer B out (TMBOUT)

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F210H	Port 2 data register	P2D	—	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	—	R/W	8	00H
0F215H	Port 2 mode register 1	P2MOD1	—	R/W	8	00H

17.2.2 Port 2 Data Register (P2D)

Address: 0F210H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	—	—	—	—	P23D	P22D	P21D	P20D
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the output value of Port 2. The value of this register is output to Port 2. The value written to P2D is readable.

[Description of Bits]

- **P23D to P20D** (bits 2 to 0)
  The P23D to P20D bits are used to set the output value of the Port 2 pin.

P23D	Description
0	Output level of the P23 pin: "L"
1	Output level of the P23 pin: "H"

P22D	Description
0	Output level of the P22 pin: "L"
1	Output level of the P22 pin: "H"

P21D	Description
0	Output level of the P21 pin: "L"
1	Output level of the P21 pin: "H"

P20D	Description
0	Output level of the P20 pin: "L"
1	Output level of the P20 pin: "H"

17.2.3 Port 2 control registers 0, 1 (P2CON0, P2CON1)

Address: 0F212H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON0	—	—	—	—	P23C0	P22C0	P21C0	P20C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F213H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON1	—	—	—	—	P23C1	P22C1	P21C1	P20C1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select the output state of the output pin Port 2.

[Description of Bits]

- **P23C0 to P20C0, P23C1 to P20C1** (bits 3 to 0)
  The P23C0 to P20C0 and P23C1 to P20C1 bits are used to select high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode.
  To directly drive LEDs, select N-channel open drain output mode.

P23C1	P23C0	Description
0	0	P23 pin: In high-impedance output mode (initial value)
0	1	P23 pin: In P-channel open drain output mode
1	0	P23 pin: In N-channel open drain output mode
1	1	P23 pin: In CMOS output mode

P22C1	P22C0	Description
0	0	P22 pin: In high-impedance output mode (initial value)
0	1	P22 pin: In P-channel open drain output mode
1	0	P22 pin: In N-channel open drain output mode
1	1	P22 pin: In CMOS output mode

P21C1	P21C0	Description
0	0	P21 pin: In high-impedance output mode (initial value)
0	1	P21 pin: In P-channel open drain output mode
1	0	P21 pin: In N-channel open drain output mode
1	1	P21 pin: In CMOS output mode

P20C1	P20C0	Description
0	0	P20 pin: In high-impedance output mode (initial value)
0	1	P20 pin: In P-channel open drain output mode
1	0	P20 pin: In N-channel open drain output mode
1	1	P20 pin: In CMOS output mode

17.2.4 Port 2 Mode Register (P2MOD)

Address: 0F214H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD	—	—	—	—	P23MD	P22MD	P21MD	P20MD
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F215H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD1	—	—	—	—	P23MD1	P22MD1	P21MD1	P20MD1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2MOD, P2MOD1 are a special function register (SFR) to select the primary function or the secondary function of Port 2

[Description of Bits]

- **P23MD, P23MD1** (bit 3)
  The P23MD, P23MD1 bit are used to select the primary function or the secondary function of the P23 pin.

P23MD1	P23MD	Description
0	0	General-purpose input/output , Direct LED Drive (initial value)
0	1	Prohibited
1	0	Timer B out (TMBOUT) output
1	1	Prohibited

- **P22MD, P22MD1** (bit 2)
  The P22MD, P22MD1 bit are used to select the primary function or the secondary function of the P22 pin.

P22MD1	P22MD	Description
0	0	General-purpose input/output , Direct LED Drive (initial value)
0	1	Prohibited
1	0	Timer 9 out (TM9OUT) output
1	1	Prohibited

- **P21MD, P21MD1** (bit 1)
  The P21MD, P21MD1 bit are used to select the primary function or the secondary function of the P21 pin.

P21MD1	P21MD	Description
0	0	General-purpose input/output, Direct LED Drive (initial value)
0	1	High-speed clock (OUTCLK) output
1	0	Prohibited
1	1	Prohibited

- **P20MD, P20MD1** (bit 0)
  The P20MD, P20MD1 bit are used to select the primary function or the secondary function of the P20 pin.

P20MD1	P20MD	Description
0	0	General-purpose input/output , Direct LED Drive (initial value)
0	1	Low-speed clock (LSCLK) output
1	0	Prohibited
1	1	Prohibited

Note:
Since P2 (port 2) is a pin only for an output, it does not have a register which chooses the input-and-output direction.

17.3 Description of Operation

17.3.1 Output Port Function

For each pin of Port 2, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 2 control registers 0 and 1 (P2CON0 and P2CON1). At a system reset, high-impedance output mode is selected as the initial state.
Depending of the value set in the Port 2 data register (P2D), a "L" level or "H" level signal is output to each pin of Port 2.

17.3.2 Secondary Function

Low-speed clock (LSCLK) output, high-speed clock (OUTCLK) output, Timer 9 out,(TM9OUT) or Timer B out (TMBOUT) are assigned to Port 2 as its secondary functions. These secondary functions can be used by setting the P23MD to P20MD, P23MD1 to P20MD1 bits of the Port 2 mode register (P2MOD, P2MOD1) to "1".

Chapter 18

Port 3

18. Port 3

18.1 Overview

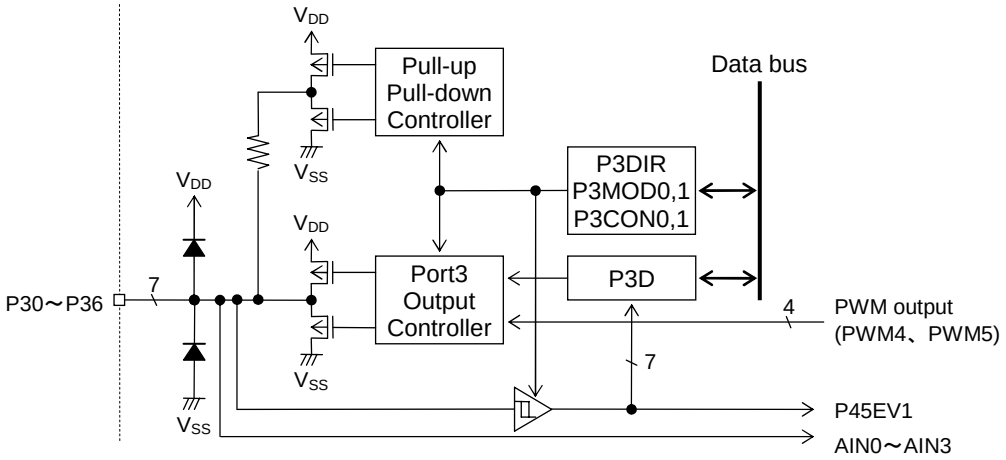
This LSI includes Port 3 (P30 to P36), which is a 8-bit input/output port.
Port 3 can output a PWM output (PWM4, PWM5) as tertiary functional mode. For PWM out put, refer to Chapter 10, "PWM"..

18.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- Allows output of PWM (PWM4, PWM5) as tertiary functions.
- P30 pin can be used as P45EV1 input pin of PWM.
- P30 - P33 pin can be used as an analog input pin of Successive Approximation Type A/D Converter.

18.1.2 Configuration

Figure 18-1 shows the configuration of Port 3.



P3D	: Port 3 data register
P3DIR	: Port 3 direction register
P3CON0	: Port 3 control register 0
P3CON1	: Port 3 control register 1
P3MOD0	: Port 3 mode register 0
P3MOD1	: Port 3 mode register 1

Figure 18-1 Configuration of Port 3

Note:
P30-P33 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

18.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P30/ AIN0/ P45EV1	I/O	Input/output port SA-ADC input P45EV1 input	–	–
P31/ AIN1	I/O	Input/output port SA-ADC input	–	–
P32/ AIN2	I/O	Input/output port SA-ADC input	–	–
P33/ AIN3	I/O	Input/output port SA-ADC input	–	–
P34/PWM4	I/O	Input/output port	–	PWM output (PWM4)
P35/PWM5	I/O	Input/output port	–	PWM output (PWM5)
P36/LSCLK	I/O	Input/output port	Low-speed clock output(LSCLK)	–

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F218H	Port 3 data register	P3D	—	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F21DH	Port 3 mode register 1	P3MOD1		R/W	8	00H

18.2.2 Port 3 Data Register (P3D)

Address: 0F218H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3D	—	P36D	P35D	P34D	P33D	P32D	P31D	P30D
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3D is a special function register (SFR) to set values to be output to, or to read the input levels of, the pins of Port 3. In output mode, the value of this register is output to he pins of Port 3. The value written to P3D is readable. In input mode, when P3D is read, the input level of each pin of Port 3 is read. Output mode or input mode is selected using the port mode register (P3DIR) described later.

[Description of Bits]

- **P36D to P30D** (bits 6 to 0)
  These bits are used to set the output value of each pin of Port 3 in output mode and to read the pin level of each pin of Port 3 in input mode.

P36D	Description
0	Output or input level of the P36 pin: "L"
1	Output or input level of the P36 pin: "H"

P35D	Description
0	Output or input level of the P35 pin: "L"
1	Output or input level of the P35 pin: "H"

P34D	Description
0	Output or input level of the P34 pin: "L"
1	Output or input level of the P34 pin: "H"

P33D	Description
0	Output or input level of the P33 pin: "L"
1	Output or input level of the P33 pin: "H"

P32D	Description
0	Output or input level of the P32 pin: "L"
1	Output or input level of the P32 pin: "H"

P31D	Description
0	Output or input level of the P31 pin: "L"
1	Output or input level of the P31 pin: "H"

P30D	Description
0	Output or input level of the P30 pin: "L"
1	Output or input level of the P30 pin: "H"

18.2.3 Port 3 Direction Register (P3DIR)

Address: 0F219H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3DIR	—	P36DIR	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

[Description of Bits]

- **P36DIR to P30DIR** (bits 6 to 0)
  The P35DIR to P30DIR pins are used to set the input/output direction of the Port 3 pin.

P36DIR	Description
0	P36 pin: Output (initial value)
1	P36 pin: Input

P35DIR	Description
0	P35 pin: Output (initial value)
1	P35 pin: Input

P34DIR	Description
0	P34 pin: Output (initial value)
1	P34 pin: Input

P33DIR	Description
0	P33 pin: Output (initial value)
1	P33 pin: Input

P32DIR	Description
0	P32 pin: Output (initial value)
1	P32 pin: Input

P31DIR	Description
0	P31 pin: Output (initial value)
1	P31 pin: Input

P30DIR	Description
0	P30 pin: Output (initial value)
1	P30 pin: Input

18.2.4 Port 3 Control Registers 0, 1 (P3CON0, P3CON1)

Address: 0F21AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON0	—	P36C0	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F21BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON1	—	P36C1	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3CON0 and P3CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 3. The conditions differ between input mode and output mode. Input or output is selected by the P3DIR register.

[Description of Bits]

- **P36C1 to P30C1, P36C0 to P30C0** (bits 6 to 0)
  The P36C1 to P30C1 pins and the P36C0 to P30C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (P36DIR bit = "0")	When input mode is selected (P36DIR bit = "1")
P36C1	**P36C0**	Description	
0	0	P36 pin: High-impedance output (initial value)	P36 pin: High-impedance output (initial value)
0	1	P36 pin: P-channel open drain output	P36 pin: P-channel open drain output
1	0	P36 pin: N-channel open drain output	P36 pin: N-channel open drain output
1	1	P36 pin: CMOS output	P36 pin: CMOS output

		When output mode is selected (P35DIR bit = "0")	When input mode is selected (P35DIR bit = "1")
P35C1	**P35C0**	Description	
0	0	P35 pin: High-impedance output (initial value)	P35 pin: High-impedance output (initial value)
0	1	P35 pin: P-channel open drain output	P35 pin: P-channel open drain output
1	0	P35 pin: N-channel open drain output	P35 pin: N-channel open drain output
1	1	P35 pin: CMOS output	P35 pin: CMOS output

		When output mode is selected (P34DIR bit = "0")	When input mode is selected (P34DIR bit = "1")
P34C1	**P34C0**	Description	
0	0	P34 pin: High-impedance output (initial value)	P34 pin: High-impedance output (initial value)
0	1	P34 pin: P-channel open drain output	P34 pin: P-channel open drain output
1	0	P34 pin: N-channel open drain output	P34 pin: N-channel open drain output
1	1	P34 pin: CMOS output	P34 pin: CMOS output

		When output mode is selected (P33DIR bit = "0")	When input mode is selected (P33DIR bit = "1")
P33C1	**P33C0**	Description	
0	0	P33 pin: High-impedance output (initial value)	P33 pin: High-impedance output (initial value)
0	1	P33 pin: P-channel open drain output	P33 pin: P-channel open drain output
1	0	P33 pin: N-channel open drain output	P33 pin: N-channel open drain output
1	1	P33 pin: CMOS output	P33 pin: CMOS output

		When output mode is selected (P32DIR bit = "0")	When input mode is selected (P32DIR bit = "1")
P32C1	**P32C0**	Description	
0	0	P32 pin: High-impedance output (initial value)	P32 pin: High-impedance output (initial value)
0	1	P32 pin: P-channel open drain output	P32 pin: P-channel open drain output
1	0	P32 pin: N-channel open drain output	P32 pin: N-channel open drain output
1	1	P32 pin: CMOS output	P32 pin: CMOS output

		When output mode is selected (P31DIR bit = "0")	When input mode is selected (P31DIR bit = "1")
P31C1	**P31C0**	Description	
0	0	P31 pin: High-impedance output (initial value)	P31 pin: High-impedance output (initial value)
0	1	P31 pin: P-channel open drain output	P31 pin: P-channel open drain output
1	0	P31 pin: N-channel open drain output	P31 pin: N-channel open drain output
1	1	P31 pin: CMOS output	P31 pin: CMOS output

		When output mode is selected (P30DIR bit = "0")	When input mode is selected (P30DIR bit = "1")
P30C1	**P30C0**	Description	
0	0	P30 pin: High-impedance output (initial value)	P30 pin: High-impedance output (initial value)
0	1	P30 pin: P-channel open drain output	P30 pin: P-channel open drain output
1	0	P30 pin: N-channel open drain output	P30 pin: N-channel open drain output
1	1	P30 pin: CMOS output	P30 pin: CMOS output

18.2.5 Port 3 Mode Registers 0, 1 (P3MOD0, P3MOD1)

Address: 0F21CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD0	—	P36MD0	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F21DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD1	—	P36MD0	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3MOD0 and P3MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 3.

[Description of Bits]

- **P36MD1, P36MD0** (bit 6)
  The P36MD1 and P36MD0 bits are used to select the primary , secondary function or tertiary function of the P36 pin.

P36MD1	P36MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Low-speed clock (LSCLK) output
1	0	Prohibited
1	1	Prohibited

- **P35MD1, P35MD0** (bit 5)
  The P35MD1 and P35MD0 bits are used to select the primary , secondary function or tertiary function of the P35 pin.

P35MD1	P35MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	PWM5 output
1	1	Prohibited

- **P34MD1, P34MD0** (bit 4)
  The P34MD1 and P34MD0 bits are used to select the primary , secondary function or tertiary function of the P34 pin.

P34MD1	P34MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	PWM4 output
1	1	Prohibited

- **P33MD1, P33MD0** (bit 3)
  The P33MD1 and P33MD0 bits are used to select the primary , secondary function or tertiary function of the P33 pin.

P33MD1	P33MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

- **P32MD1, P32MD0** (bit 2)
  The P32MD1 and P32MD0 bits are used to select the primary , secondary function or tertiary function of the P32 pin.

P32MD1	P32MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

- **P31MD1, P31MD0** (bit 1)
  The P31MD1 and P31MD0 bits are used to select the primary , secondary function or tertiary function of the P31 pin.

P31MD1	P31MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

- **P30MD1, P30MD0** (bit 0)
  The P30MD1 and P30MD0 bits are used to select the primary , secondary function or tertiary function of the P30 pin.

P30MD1	P30MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

Note:
If "Prohibited" is set for a Port 3 pin by this register and output mode is selected (by port 3 direction register) for the pin, the output status of that pin will be fixed irrespective of the port data register (P3D) settings, as shown below.

When high-impedance output selected: Fixed to high-impedance output
When Pch open drain output selected: Fixed to high-impedance output
When Nch open drain output selected: Fixed to a "L" level output
When CMOS output selected: Fixed to a "L" level output

18.3 Description of Operation

18.3.1 Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

18.3.2 Secondary Function

PWM output (PWM4, PWM5) are assigned to Port 3 as its tertiary functions. They can be used by setting the P36MD0–P30MD0 and P36MD1–P30MD1 bits of the port 3 mode registers (P3MOD0, P3MOD1) to designated values.

Note:
P30-P33 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

Chapter 19

Port 4

19. Port 4

19.1 Overview

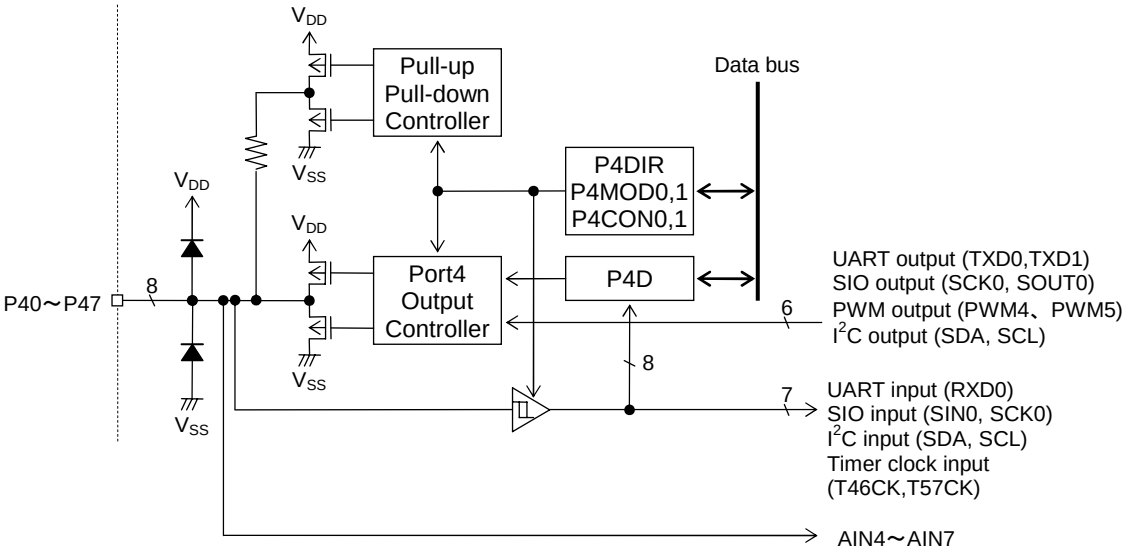
This LSI includes Port 4 (P40 to P47) which is an 8-bit input/output port.
Port 4 can have the PWM output, UART, synchronous serial port or I^2C bus interface functions as secondary, tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM";, for the UART, see Chapter 12, "UART"; for the synchronous serial port, see Chapter 11, "Synchronous Serial Port", for the I^2C, see Chapter 13, "I^2C Bus Interface".

19.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The PWM pin (PWM4, PWM5), UART pins (RXD0, TXD0,TXD1), synchronous serial port pins (SIN0, SCK0, SOUT0) or I^2C pin (SDA, SCL) can be used as secondary, tertiary and fourthly functions.
- P44 – P47 pin can be used as an analog input pin of Successive Approximation Type A/D Converter.

19.1.2 Configuration

Figure 19-1 shows the configuration of Port 4.



P4D	: Port 4 data register
P4DIR	: Port 4 direction register
P4CON0	: Port 4 control register 0
P4CON1	: Port 4 control register 1
P4MOD0	: Port 4 mode register 0
P4MOD1	: Port 4 mode register 1

Figure 19-1 Configuration of Port 4

Note:
P44 – P47 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

19.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
P40/SDA/SIN0	I/O	Input/output port	I^2C bus data input	SSIO0 data input	—
P41/SCL/SCK0	I/O	Input/output port	I^2C bus clock input	SSIO0 synchronous clock input/output	—
P42/RXD0/SOUT0	I/O	Input/output port	UART0 data input	SSIO0 data output	—
P43/TXD0/PWM4/ TXD1	I/O	Input/output port	UART0 data output	PWM4 output	UART1 data output
P44/SIN0/AIN4	I/O	Input/output port SA-ADC input	—	SSIO0 data input	—
P45/SCK0/AIN5	I/O	Input/output port SA-ADC input	—	SSIO0 synchronous clock input/output	—
P46/SOUT0/AIN6	I/O	Input/output port SA-ADC input	—	SSIO0 data output	—
P47/PWM5/AIN7	I/O	Input/output port SA-ADC input	—	PWM5 output	—

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F220H	Port 4 data register	P4D	—	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H

19.2.2 Port 4 Data Register (P4D)

Address: 0F220H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable. In input mode, the input level of the Port 4 pin is read when P4D is read. Output mode or input mode is selected by using the port mode register (P4DIR) described later.

[Description of Bits]

- **P47D to P40D** (bits 7 to 0)
  The P47D to P40D bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P47D	Description
0	Output or input level of the P47 pin: "L"
1	Output or input level of the P47 pin: "H"

P46D	Description
0	Output or input level of the P46 pin: "L"
1	Output or input level of the P46 pin: "H"

P45D	Description
0	Output or input level of the P45 pin: "L"
1	Output or input level of the P45 pin: "H"

P43D	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

P43D	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

P42D	Description
0	Output or input level of the P42 pin: "L"
1	Output or input level of the P42 pin: "H"

P41D	Description
0	Output or input level of the P41 pin: "L"
1	Output or input level of the P41 pin: "H"

P40D	Description
0	Output or input level of the P40 pin: "L"
1	Output or input level of the P40 pin: "H"

19.2.3 Port 4 Direction Register (P4DIR)

Address: 0F221H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

[Description of Bits]

- **P47DIR to P40DIR** (bits 7 to 0)
  The P47DIR to P40DIR pins are used to set the input/output direction of the Port 4 pin.

P47DIR	Description
0	P47 pin: Output (initial value)
1	P47 pin: Input

P46DIR	Description
0	P46 pin: Output (initial value)
1	P46 pin: Input

P45DIR	Description
0	P45 pin: Output (initial value)
1	P45 pin: Input

P44DIR	Description
0	P44 pin: Output (initial value)
1	P44 pin: Input

P43DIR	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

19.2.4 Port 4 Control Registers 0, 1 (P4CON0, P4CON1)

Address: 0F222H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON0	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F223H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON1	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 4. The conditions differ between input mode and output mode. Input or output is selected by the P4DIR register.

[Description of Bits]

- **P47C1 to P40C1, P47C0 to P40C0** (bits 7 to 0)
  The P47C1 to P40C1 pins and the P47C0 to P40C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P47 pin		When output mode is selected (P47DIR bit = "0")	When input mode is selected (P47DIR bit = "1")
P47C1	**P47C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P46 pin		When output mode is selected (P46DIR bit = "0")	When input mode is selected (P46DIR bit = "1")
P46C1	**P46C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P45 pin		When output mode is selected (P45DIR bit = "0")	When input mode is selected (P45DIR bit = "1")
P45C1	**P45C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P44 pin		When output mode is selected (P44DIR bit = "0")	When input mode is selected (P44DIR bit = "1")
P44C1	**P44C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = "0")	When input mode is selected (P43DIR bit = "1")
P43C1	**P43C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = "0")	When input mode is selected (P42DIR bit = "1")
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

19.2.5 Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)

Address: 0F224H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD0	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F225H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD1	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) to select the primary, secondary, tertiary and fourthly functions of Port 4.

[Description of Bits]

- **P47MD1, P47MD0** (bit 7)
  The P47MD1 and P47MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P47 pin.

P47MD1	P47MD0	Description
0	0	General-purpose input/output (initial value)
0	1	Prohibited
1	0	PWM5 output
1	1	Prohibited

- **P46MD1, P46MD0** (bit 6)
  The P46MD1 and P46MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P46 pin.

P46MD1	P46MD0	Description
0	0	General-purpose input/output (initial value)
0	1	Prohibited
1	0	SSIO0 data output
1	1	Prohibited

- **P45MD1, P45MD0** (bit 5)
  The P45MD1 and P45MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P45 pin.

P45MD1	P45MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SSIO0 synchronous clock output
1	1	Prohibited

- **P44MD1, P44MD0** (bit 4)
  The P44MD1 and P44MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P44 pin.

P44MD1	P44MD0	Description
0	0	General-purpose input/output (initial value)
0	1	Prohibited
1	0	SSIO0 data input
1	1	Prohibited

- **P43MD1, P43MD0** (bit 3)
  The P43MD1 and P43MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P43 pin.

P43MD1	P43MD0	Description
0	0	General-purpose input/output (initial value)
0	1	UART0 data output
1	0	PWM4 output
1	1	UART1 data output

- **P42MD1, P42MD0** (bit 2)
  The P42MD1 and P42MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output (initial value)
0	1	UART0 data input
1	0	SSIO0 data output
1	1	Prohibited

- **P41MD1, P41MD0** (bit 1)
  The P41MD1 and P41MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the P41 pin.

P41MD1	P41MD0	Description
0	0	General-purpose input/output (initial value)
0	1	I^2Cbus clock input/output
1	0	SSIO0 clock input/output
1	1	Prohibited

- **P40MD1, P40MD0** (bit 0)
  The P40MD1 and P40MD0 bits are used to select the primary, secondary, tertiary and fourthly function of the P40 pin.

P40MD1	P40MD0	Description
0	0	General-purpose input/output (initial value)
0	1	I^2Cbus data input/output
1	0	SSIO0 data input
1	1	Prohibited

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port 4 is specified to output mode (selected in port4 control register), status of corresponding pin is fixed, regardless the contents of Port4 register (P4D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

Note.
If any pin set to SSIOn or UARTn output pin by secondary, tertiary and fourthly functions, the pin tatus of corresponding pin is fixed CMOS output.

19.3 Description of Operation

19.3.1 Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

19.3.2 Secondary, tertiary and fourthly functions

Port 4 is assigned PWM pins (PWM4, PWM5), UART pins (RXD0, TXD0, TXD1) and synchronous serial port 0 pins (SIN0, SCK0, SOUT) and I^2C bus pin (SDA, SCL) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the P47MD0 to P40MD0 bits and the P47MD1 to P40MD1 bits of the Port 4 mode registers (P4MOD0, P4MOD1).

Note:
P44 – P47 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

Chapter 20

Port 5

20. Port 5

20.1 Overview

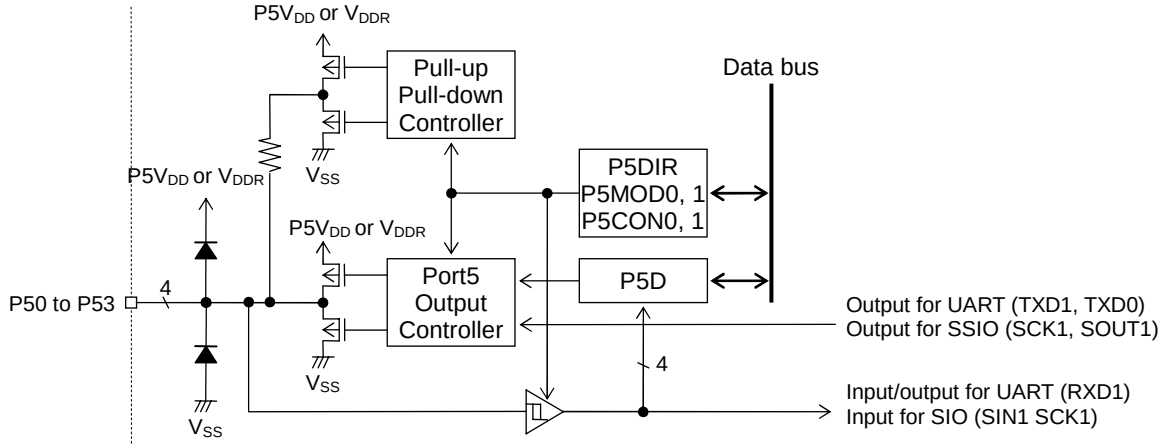
This LSI includes Port 5 (P50 to P53) which is an 4-bit input/output port.

20.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The UART pins (RXD1, TXD1, TXD0), synchronous serial port pins (SIN1, SCK1, SOUT1) can be used as the secondary functions.

20.1.2 Configuration

Figure 20-1 shows the configuration of Port 5.



P5D : Port 5 data register
P5DIR : Port 5 direction register
P5CON0 : Port 5 control register 0
P5CON1 : Port 5 control register 1
P5MOD0 : Port 5 mode register 0
P5MOD1 : Port 5 mode register 1

Figure 20-1 Configuration of Port 5

20.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quaternary function
P50/SIN0	I/O	Input/output port	—	SSIO1 data input	—
P51/SCK1	I/O	Input/output port	—	SSIO1 synchronous clock input/output	—
P52/RXD1/SOUT1	I/O	Input/output port	UART1 data input	SSIO1 data output	—
P53/TXD1/TXD0	I/O	Input/output port	UART1 data output	—	UART0 data output

20.2 Description of Registers

20.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F228H	Port 5 data register	P5D	—	R/W	8	00H
0F229H	Port 5 direction register	P5DIR	—	R/W	8	00H
0F22AH	Port 5 control register 0	P5CON0	P5CON	R/W	8/16	00H
0F22BH	Port 5 control register 1	P5CON1		R/W	8	00H
0F22CH	Port 5 mode register 0	P5MOD0	P5MOD	R/W	8/16	00H
0F22DH	Port 5 mode register 1	P5MOD1		R/W	8	00H

20.2.2 Port 5 Data Register (P5D)

Address: 0F228H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5D	—	—	—	—	P53D	P52D	P51D	P50D
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5D is a special function register (SFR) to set the value to be output to the Port 5 pin or to read the input level of the Port 5. In output mode, the value of this register is output to the Port 5 pin. The value written to P5D is readable. In input mode, the input level of the Port 5 pin is read when P5D is read. Output mode or input mode is selected by using the port mode register (P5DIR) described later.

[Description of Bits]

- **P53D to P50D** (bits 3 to 0)
  The P53D to P50D bits are used to set the output value of the Port 5 pin in output mode and to read the pin level of the Port 5 pin in input mode.

P53D	Description
0	Output or input level of the P53 pin: "L"
1	Output or input level of the P53 pin: "H"

P52D	Description
0	Output or input level of the P52 pin: "L"
1	Output or input level of the P52 pin: "H"

P51D	Description
0	Output or input level of the P51 pin: "L"
1	Output or input level of the P51 pin: "H"

P50D	Description
0	Output or input level of the P50 pin: "L"
1	Output or input level of the P50 pin: "H"

20.2.3 Port 5 Direction Register (P5DIR)

Address: 0F229H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5DIR	—	—	—	—	P53DIR	P52DIR	P51DIR	P50DIR
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5DIR is a special function register (SFR) to select the input/output mode of Port 5.

[Description of Bits]

- **P53DIR to P50DIR** (bits 3 to 0)
  The P53DIR to P50DIR pins are used to set the input/output direction of the Port 5 pin.

P53DIR	Description
0	P53 pin: Output (initial value)
1	P53 pin: Input

P52DIR	Description
0	P52 pin: Output (initial value)
1	P52 pin: Input

P51DIR	Description
0	P51 pin: Output (initial value)
1	P51 pin: Input

P50DIR	Description
0	P50 pin: Output (initial value)
1	P50 pin: Input

20.2.4 Port 5 Control Registers 0, 1 (P5CON0, P5CON1)

Address: 0F22AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON0	—	—	—	—	P53C0	P52C0	P51C0	P50C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON1	—	—	—	—	P53C1	P52C1	P51C1	P50C1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5CON0 and P5CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 5. The conditions differ between input mode and output mode. Input or output is selected by the P5DIR register.

[Description of Bits]

- **P53C1 to P50C1, P53C0 to P50C0** (bits 3 to 0)
  The P57C1 to P50C1 pins and the P57C0 to P50C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P53 pin		When output mode is selected (P53DIR bit = "0")	When input mode is selected (P53DIR bit = "1")
P53C1	**P53C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P52 pin		When output mode is selected (P52DIR bit = "0")	When input mode is selected (P52DIR bit = "1")
P52C1	**P52C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P51 pin		When output mode is selected (P51DIR bit = "0")	When input mode is selected (P51DIR bit = "1")
P51C1	**P51C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P50 pin		When output mode is selected (P50DIR bit = "0")	When input mode is selected (P50DIR bit = "1")
P50C1	**P50C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

20.2.5 Port 5 Mode Registers 0, 1 (P5MOD0, P5MOD1)

Address: 0F22CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD0	—	—	—	—	P53MD0	P52MD0	P51MD0	P50MD0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD1	—	—	—	—	P53MD1	P52MD1	P51MD1	P50MD1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5MOD0 and P5MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 5.

[Description of Bits]

- **P53MD1, P53MD0** (bit 3)
  The P53MD1 and P53MD0 bits are used to select the primary, secondary, tertiary, or fourthly function of the P53 pin.

P53MD1	P53MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART1 data output pin
1	0	Prohibited
1	1	UART0 data output pin

- **P52MD1, P52MD0** (bit 2)
  The P52MD1 and P52MD0 bits are used to select the primary, secondary, tertiary, or fourthly function of the P52 pin.

P52MD1	P52MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART1 input pin
1	0	SIO1 data output pin
1	1	Prohibited

- **P51MD1, P51MD0** (bit 1)
  The P51MD1 and P51MD0 bits are used to select the primary, secondary, tertiary, or fourthly function of the P51 pin.

P51MD1	P51MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SIO1 clock input/output pin
1	1	Prohibited

- **P50MD1, P50MD0** (bit 0)
  The P50MD1 and P50MD0 bits are used to select the primary, secondary, tertiary, or fourthly function of the P50 pin.

P50MD1	P50MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SIO1 data input pin
1	1	Prohibited

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the Port 5 is specified to output mode (selected in Port 5 control register), status of corresponding pin is fixed, regardless the contents of Port 5 register (P5D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

20.3 Description of Operation

20.3.1 Input/Output Port Functions

For each pin of Port 5, either output or input is selected by setting the Port 5 direction register (P5DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 5 control registers 0 and 1 (P5CON0 and P5CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 5 control registers 0 and 1 (P5CON0 and P5CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 5 depending on the value set by the Port 5 data register (P5D).
In input mode, the input level of each pin of Port 5 can be read from the Port 5 data register (P5D).

20.3.2 Secondary, tertiary, and fourthly Function

Port 5 is assigned UART pins (RXD1, TXD1, TXD0) and synchronous serial port 0 pins (SIN1, SCK1, SOUT1) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the P53MD0 to P50MD0 bits and the P53MD1 to P50MD1 bits of the Port 5 mode registers (P5MOD0, P5MOD1).

Chapter 21

Port 6

21. Port 6

21.1 Overview

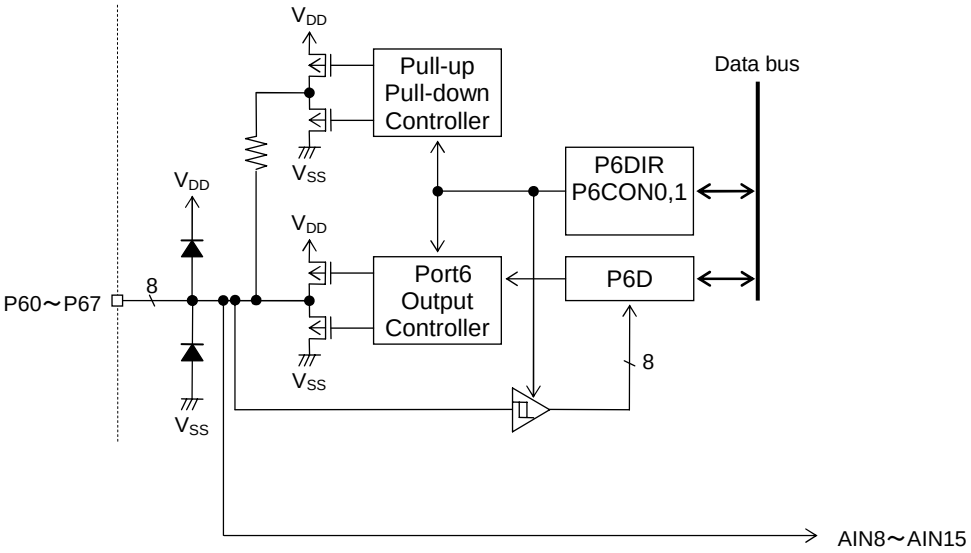
This LSI includes Port 6 (P60 to P67) which is an 8-bit input/output port.

21.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- P60 – P67 pin can be used as an analog input pin of Successive Approximation Type A/D Converter.

21.1.2 Configuration

Figure 21-1 shows the configuration of Port 6.



P6D : Port 6 data register
P6DIR : Port 6 direction register
P6CON0 : Port 6 control register 0
P6CON1 : Port 6 control register 1

Figure 21-1 Configuration of Port 6

Note:
P60 – P67 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

21.1.3 List of Pins

Pin name	I/O	Primary function
P60/ AIN8	I/O	Input/output port, SA-ADC input
P61/ AIN9	I/O	Input/output port, SA-ADC input
P62/ AIN10	I/O	Input/output port, SA-ADC input
P63/ AIN11	I/O	Input/output port, SA-ADC input
P64/ AIN12	I/O	Input/output port, SA-ADC input
P65/ AIN13	I/O	Input/output port, SA-ADC input
P66/ AIN14	I/O	Input/output port, SA-ADC input
P67/ AIN14	I/O	Input/output port, SA-ADC input

21.2 Description of Registers

21.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F230H	Port 6 data register	P6D	—	R/W	8	00H
0F231H	Port 6 direction register	P6DIR	—	R/W	8	00H
0F232H	Port 6 control register 0	P6CON0	P6CON	R/W	8/16	00H
0F233H	Port 6 control register 1	P6CON1		R/W	8	00H

21.2.2 Port 6 Data Register (P6D)

Address: 0F230H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6D	P67D	P66D	P65D	P64D	P63D	P62D	P61D	P60D
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6D is a special function register (SFR) to set the value to be output to the Port 6 pin or to read the input level of the Port 6. In output mode, the value of this register is output to the Port 6 pin. The value written to P6D is readable. In input mode, the input level of the Port 6 pin is read when P6D is read. Output mode or input mode is selected by using the port mode register (P6DIR) described later.

[Description of Bits]

- **P67D to P60D** (bits 7 to 0)
  The P67D to P60D bits are used to set the output value of the Port 6 pin in output mode and to read the pin level of the Port 6 pin in input mode.

P67D	Description
0	Output or input level of the P67 pin: "L"
1	Output or input level of the P67 pin: "H"

P66D	Description
0	Output or input level of the P66 pin: "L"
1	Output or input level of the P66 pin: "H"

P65D	Description
0	Output or input level of the P65 pin: "L"
1	Output or input level of the P65 pin: "H"

P63D	Description
0	Output or input level of the P63 pin: "L"
1	Output or input level of the P63 pin: "H"

P63D	Description
0	Output or input level of the P63 pin: "L"
1	Output or input level of the P63 pin: "H"

P62D	Description
0	Output or input level of the P62 pin: "L"
1	Output or input level of the P62 pin: "H"

P61D	Description
0	Output or input level of the P61 pin: "L"
1	Output or input level of the P61 pin: "H"

P60D	Description
0	Output or input level of the P60 pin: "L"
1	Output or input level of the P60 pin: "H"

21.2.3 Port 6 Direction Register (P6DIR)

Address: 0F231H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6DIR	P67DIR	P66DIR	P65DIR	P64DIR	P63DIR	P62DIR	P61DIR	P60DIR
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6DIR is a special function register (SFR) to select the input/output mode of Port 6.

[Description of Bits]

- **P67DIR to P60DIR** (bits 7 to 0)
  The P67DIR to P60DIR pins are used to set the input/output direction of the Port 6 pin.

P67DIR	Description
0	P67 pin: Output (initial value)
1	P67 pin: Input

P66DIR	Description
0	P66 pin: Output (initial value)
1	P66 pin: Input

P65DIR	Description
0	P65 pin: Output (initial value)
1	P65 pin: Input

P64DIR	Description
0	P64 pin: Output (initial value)
1	P64 pin: Input

P63DIR	Description
0	P63 pin: Output (initial value)
1	P63 pin: Input

P62DIR	Description
0	P62 pin: Output (initial value)
1	P62 pin: Input

P61DIR	Description
0	P61 pin: Output (initial value)
1	P61 pin: Input

P60DIR	Description
0	P60 pin: Output (initial value)
1	P60 pin: Input

21.2.4 Port 6 Control Registers 0, 1 (P6CON0, P6CON1)

Address: 0F232H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6CON0	P67C0	P66C0	P65C0	P64C0	P63C0	P62C0	P61C0	P60C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F233H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6CON1	P67C1	P66C1	P65C1	P64C1	P63C1	P62C1	P61C1	P60C1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6CON0 and P6CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 6. The conditions differ between input mode and output mode. Input or output is selected by the P6DIR register.

[Description of Bits]

- **P67C1 to P60C1, P67C0 to P60C0** (bits 7 to 0)
  The P67C1 to P60C1 pins and the P67C0 to P60C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P67 pin		When output mode is selected (P67DIR bit = "0")	When input mode is selected (P67DIR bit = "1")
P67C1	**P67C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P66 pin		When output mode is selected (P66DIR bit = "0")	When input mode is selected (P66DIR bit = "1")
P66C1	**P66C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P65 pin		When output mode is selected (P65DIR bit = "0")	When input mode is selected (P65DIR bit = "1")
P65C1	**P65C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P64 pin		When output mode is selected (P64DIR bit = "0")	When input mode is selected (P64DIR bit = "1")
P64C1	**P64C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P63 pin		When output mode is selected (P63DIR bit = "0")	When input mode is selected (P63DIR bit = "1")
P63C1	**P63C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P62 pin		When output mode is selected (P62DIR bit = "0")	When input mode is selected (P62DIR bit = "1")
P62C1	**P62C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P61 pin		When output mode is selected (P61DIR bit = "0")	When input mode is selected (P61DIR bit = "1")
P61C1	**P61C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P60 pin		When output mode is selected (P60DIR bit = "0")	When input mode is selected (P60DIR bit = "1")
P60C1	**P60C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

21.3 Description of Operation

21.3.1 Input/Output Port Functions

For each pin of Port 6, either output or input is selected by setting the Port 6 direction register (P6DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 6 control registers 0 and 1 (P6CON0 and P6CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 6 control registers 0 and 1 (P6CON0 and P6CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 6 depending on the value set by the Port 6 data register (P6D).
In input mode, the input level of each pin of Port 6 can be read from the Port 6 data register (P6D).

Chapter 22

Port 9

22. Port 9

22.1 Overview

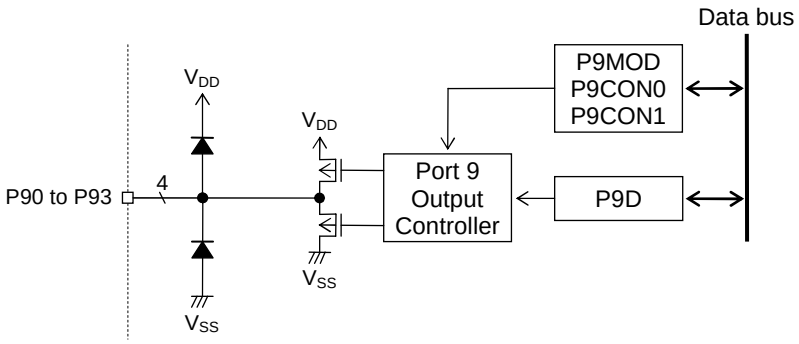
This LSI incorporates Port 9 (P90–P93), a 4-bit port for output only.

22.1.1 Features

- Allows direct LED drive.
- High-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output can be selected for each bit.
- Operates as an LED drive port, when a general-purpose output port function is chosen.

22.1.2 Configuration

Figure 22-1 shows the configuration of Port 9.



P9D : Port 9 data register
P9CON0 : Port 9 control register 0
P9CON1 : Port 9 control register 1
P9MOD : Port 9 mode register

Figure 22-1 Configuration of Port 9

22.1.3 List of Pins

Pin name	I/O	Primary function
P90/LED0	O	Output port, Direct LED drive
P91/LED1	O	Output port, Direct LED drive
P92/LED2	O	Output port, Direct LED drive
P93/LED3	O	Output port, Direct LED drive

22.2 Description of Registers

22.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F248H	Port 9 data register	P9D	—	R/W	8	00H
0F24AH	Port 9 control register 0	P9CON0	P9CON	R/W	8/16	00H
0F24BH	Port 9 control register 1	P9CON1		R/W	8	00H

22.2.2 Port 9 Data Register (P9D)

Address: 0F210H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9D	—	—	—	—	P93D	P92D	P91D	P90D
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P9D is a special function register (SFR) to set the output value of Port 9. The value of this register is output to Port 9. The value written to P9D is readable.

[Description of Bits]

- **P93D to P90D** (bits 2 to 0)
  The P93D to P90D bits are used to set the output value of the Port 9 pin.

P93D	Description
0	Output level of the P93 pin: "L"
1	Output level of the P93 pin: "H"

P92D	Description
0	Output level of the P92 pin: "L"
1	Output level of the P92 pin: "H"

P91D	Description
0	Output level of the P91 pin: "L"
1	Output level of the P91 pin: "H"

P90D	Description
0	Output level of the P90 pin: "L"
1	Output level of the P90 pin: "H"

22.2.3 Port 9 control registers 0, 1 (P9CON0, P9CON1)

Address: 0F212H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9CON0	—	—	—	—	P93C0	P92C0	P91C0	P90C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F213H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9CON1	—	—	—	—	P93C1	P92C1	P91C1	P90C1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P9CON0 and P9CON1 are special function registers (SFRs) to select the output state of the output pin Port 9.

[Description of Bits]

- **P93C0 to P90C0, P93C1 to P90C1** (bits 3 to 0)
  The P93C0 to P90C0 and P93C1 to P90C1 bits are used to select high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode.
  To directly drive LEDs, select N-channel open drain output mode.

P93C1	P93C0	Description
0	0	P93 pin: In high-impedance output mode (initial value)
0	1	P93 pin: In P-channel open drain output mode
1	0	P93 pin: In N-channel open drain output mode
1	1	P93 pin: In CMOS output mode

P92C1	P92C0	Description
0	0	P92 pin: In high-impedance output mode (initial value)
0	1	P92 pin: In P-channel open drain output mode
1	0	P92 pin: In N-channel open drain output mode
1	1	P92 pin: In CMOS output mode

P91C1	P91C0	Description
0	0	P91 pin: In high-impedance output mode (initial value)
0	1	P91 pin: In P-channel open drain output mode
1	0	P91 pin: In N-channel open drain output mode
1	1	P91 pin: In CMOS output mode

P90C1	P90C0	Description
0	0	P90 pin: In high-impedance output mode (initial value)
0	1	P90 pin: In P-channel open drain output mode
1	0	P90 pin: In N-channel open drain output mode
1	1	P90 pin: In CMOS output mode

22.3 Description of Operation

22.3.1 Output Port Function

For each pin of Port 9, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 9 control registers 0 and 1 (P9CON0 and P9CON1). At a system reset, high-impedance output mode is selected as the initial state.
Depending of the value set in the Port 9 data register (P9D), a "L" level or "H" level signal is output to each pin of Port 9.

Chapter 23

Port C

23. Port C

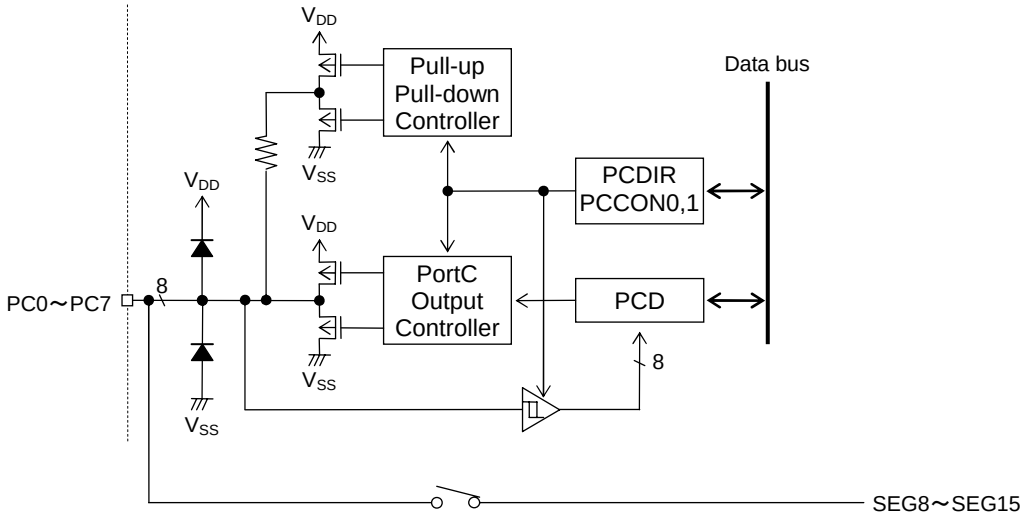
23.1 Overview

This LSI includes Port C (PC0 to PC7), which is a 8-bit input/output port.
Either an I/O Port or a segment driver output can be selected as a function of SEG8 to SEG15 by a LCD port segment selection register(LSELS1). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

23.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- Either an I/O Port or a segment driver output can be selected as a function of SEG8 to SEG15 by a LCD port segment selection register(LSELS1).

23.1.2 Configuration



PCD	: Port C data register
PCDIR	: Port C direction register
PCCON0	: Port C control register 0
PCCON1	: Port C control register 1

Figure 23-1 Configuration of Port C

23.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
PC0	I/O	Input/output port	SEG8
PC1	I/O	Input/output port	SEG9
PC2	I/O	Input/output port	SEG10
PC3	I/O	Input/output port	SEG11
PC4	I/O	Input/output port	SEG12
PC5	I/O	Input/output port	SEG13
PC6	I/O	Input/output port	SEG14
PC7	I/O	Input/output port	SEG15

23.2 Description of Registers

23.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F260H	Port C data register	PCD	—	R/W	8	00H
0F261H	Port C direction register	PCDIR	—	R/W	8	00H
0F262H	Port C control register 0	PCCON0	PCCON	R/W	8/16	00H
0F263H	Port C control register 1	PCCON1		R/W	8	00H

23.2.2 Port C data register (PCD)

Address: 0F260H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCD	PC7D	PC6D	PC5D	PC4D	PC3D	PC2D	PC1D	PC0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCD is a special function register (SFR) to set the value to be output to the Port C pin or to read the input level of the Port C. In output mode, the value of this register is output to the Port C pin. The value written to PCD is readable. In input mode, the input level of the Port C pin is read when PCD is read. Output mode or input mode is selected by using the port direction register (PCDIR) described later.

[Description of Bits]

- **PC7D-PC0D** (bits 7-0)
  The PC7D to PC0D bits are used to set the output value of the Port C pin in output mode and to read the pin level of the Port C pin in input mode.

PC7D	Description
0	Output or input level of the PC7 pin: "L"
1	Output or input level of the PC7 pin: "H"

PC6D	Description
0	Output or input level of the PC6 pin: "L"
1	Output or input level of the PC6 pin: "H"

PC5D	Description
0	Output or input level of the PC5 pin: "L"
1	Output or input level of the PC5 pin: "H"

PC4D	Description
0	Output or input level of the PC4 pin: "L"
1	Output or input level of the PC4 pin: "H"

PC3D	Description
0	Output or input level of the PC3 pin: "L"
1	Output or input level of the PC3 pin: "H"

PC2D	Description
0	Output or input level of the PC2 pin: "L"
1	Output or input level of the PC2 pin: "H"

PC1D	Description
0	Output or input level of the PC1 pin: "L"
1	Output or input level of the PC1 pin: "H"

PC0D	Description
0	Output or input level of the PC0 pin: "L"
1	Output or input level of the PC0 pin: "H"

23.2.3 Port C Direction Register (PCDIR)

Address: 0F261H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCDIR	PC7DIR	PC6DIR	PC5DIR	PC4DIR	PC3DIR	PC2DIR	PC1DIR	PC0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCDIR is a special function register (SFR) to select the input/output mode of Port C.

[Description of Bits]

- **PC7DIR-PC0DIR** (bits 7-0)
  The PC7DIR to PC0DIR pins are used to set the input/output direction of the Port C pin.

PC7DIR	Description
0	PC7 pin: Output (initial value)
1	PC7 pin: Input

PC6DIR	Description
0	PC6 pin: Output (initial value)
1	PC6 pin: Input

PC5DIR	Description
0	PC5 pin: Output (initial value)
1	PC5 pin: Input

PC4DIR	Description
0	PC4 pin: Output (initial value)
1	PC4 pin: Input

PC3DIR	Description
0	PC3 pin: Output (initial value)
1	PC3 pin: Input

PC2DIR	Description
0	PC2 pin: Output (initial value)
1	PC2 pin: Input

PC1DIR	Description
0	PC1 pin: Output (initial value)
1	PC1 pin: Input

PC0DIR	Description
0	PC0 pin: Output (initial value)
1	PC0 pin: Input

23.2.4 Port C control registers 0, 1 (PCCON0, PCCON1)

Address: 0F262H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCCON0	PC7C0	PC6C0	PC5C0	PC4C0	PC3C0	PC2C0	PC1C0	PC0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F263H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCCON1	PC7C1	PC6C1	PC5C1	PC4C1	PC3C1	PC2C1	PC1C1	PC0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCCON0 and PCCON1 are special function registers (SFRs) to select input/output state of the Port C pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PCDIR register.

[Description of Bits]

- **PC7C1-PC0C1, PC7C0-PC0C0** (bits 7-0)
  The PC7C1 to PC0C1 pins and the PC7C0 to PC0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (PC7DIR bit = "0")	When input mode is selected (PC7DIR bit = "1")
PC7C1	**PC7C0**	Description	
0	0	PC7 pin: High-impedance output (initial value)	PC7 pin: High-impedance input
0	1	PC7 pin: P-channel open drain output	PC7 pin: Input with a pull-down resistor
1	0	PC7 pin: N-channel open drain output	PC7 pin: Input with a pull-up resistor
1	1	PC7 pin: CMOS output	PC7 pin: High-impedance input

		When output mode is selected (PC6DIR bit = "0")	When input mode is selected (PC6DIR bit = "1")
PC6C1	**PC6C0**	Description	
0	0	PC6 pin: High-impedance output (initial value)	PC6 pin: High-impedance input
0	1	PC6 pin: P-channel open drain output	PC6 pin: Input with a pull-down resistor
1	0	PC6 pin: N-channel open drain output	PC6 pin: Input with a pull-up resistor
1	1	PC6 pin: CMOS output	PC6 pin: High-impedance input

		When output mode is selected (PC5DIR bit = "0")	When input mode is selected (PC5DIR bit = "1")
PC5C1	**PC5C0**	Description	
0	0	PC5 pin: High-impedance output (initial value)	PC5 pin: High-impedance input
0	1	PC5 pin: P-channel open drain output	PC5 pin: Input with a pull-down resistor
1	0	PC5 pin: N-channel open drain output	PC5 pin: Input with a pull-up resistor
1	1	PC5 pin: CMOS output	PC5 pin: High-impedance input

		When output mode is selected (PC4DIR bit = "0")	When input mode is selected (PC4DIR bit = "1")
PC4C1	**PC4C0**	Description	
0	0	PC4 pin: High-impedance output (initial value)	PC4 pin: High-impedance input
0	1	PC4 pin: P-channel open drain output	PC4 pin: Input with a pull-down resistor
1	0	PC4 pin: N-channel open drain output	PC4 pin: Input with a pull-up resistor
1	1	PC4 pin: CMOS output	PC4 pin: High-impedance input

		When output mode is selected (PC3DIR bit = "0")	When input mode is selected (PC3DIR bit = "1")
PC3C1	**PC3C0**	Description	
0	0	PC3 pin: High-impedance output (initial value)	PC3 pin: High-impedance input
0	1	PC3 pin: P-channel open drain output	PC3 pin: Input with a pull-down resistor
1	0	PC3 pin: N-channel open drain output	PC3 pin: Input with a pull-up resistor
1	1	PC3 pin: CMOS output	PC3 pin: High-impedance input

		When output mode is selected (PC2DIR bit = "0")	When input mode is selected (PC2DIR bit = "1")
PC2C1	**PC2C0**	Description	
0	0	PC2 pin: High-impedance output (initial value)	PC2 pin: High-impedance input
0	1	PC2 pin: P-channel open drain output	PC2 pin: Input with a pull-down resistor
1	0	PC2 pin: N-channel open drain output	PC2 pin: Input with a pull-up resistor
1	1	PC2 pin: CMOS output	PC2 pin: High-impedance input

		When output mode is selected (PC1DIR bit = "0")	When input mode is selected (PC1DIR bit = "1")
PC1C1	**PC1C0**	Description	
0	0	PC1 pin: High-impedance output (initial value)	PC1 pin: High-impedance input
0	1	PC1 pin: P-channel open drain output	PC1 pin: Input with a pull-down resistor
1	0	PC1 pin: N-channel open drain output	PC1 pin: Input with a pull-up resistor
1	1	PC1 pin: CMOS output	PC1 pin: High-impedance input

		When output mode is selected (PC0DIR bit = "0")	When input mode is selected (PC0DIR bit = "1")
PC0C1	**PC0C0**	Description	
0	0	PC0 pin: High-impedance output (initial value)	PC0 pin: High-impedance input
0	1	PC0 pin: P-channel open drain output	PC0 pin: Input with a pull-down resistor
1	0	PC0 pin: N-channel open drain output	PC0 pin: Input with a pull-up resistor
1	1	PC0 pin: CMOS output	PC0 pin: High-impedance input

23.3 Description of Operation

23.3.1 Input/Output Port Functions

For each pin of Port C, either output or input is selected by setting the Port C direction register (PCDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port C control registers 0 and 1 (PCCON0 and PCCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port C control registers 0 and 1 (PCCON0 and PCCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port C depending on the value set by the Port C data register (PCD).
In input mode, the input level of each pin of Port C can be read from the Port C data register (PCD).

Note:
Either an I/O Port or a segment driver output can be selected as a function of SEG8 to SEG15 by a LCD port segment selection register(LSELS1). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

Chapter 24

Port D

24. Port D

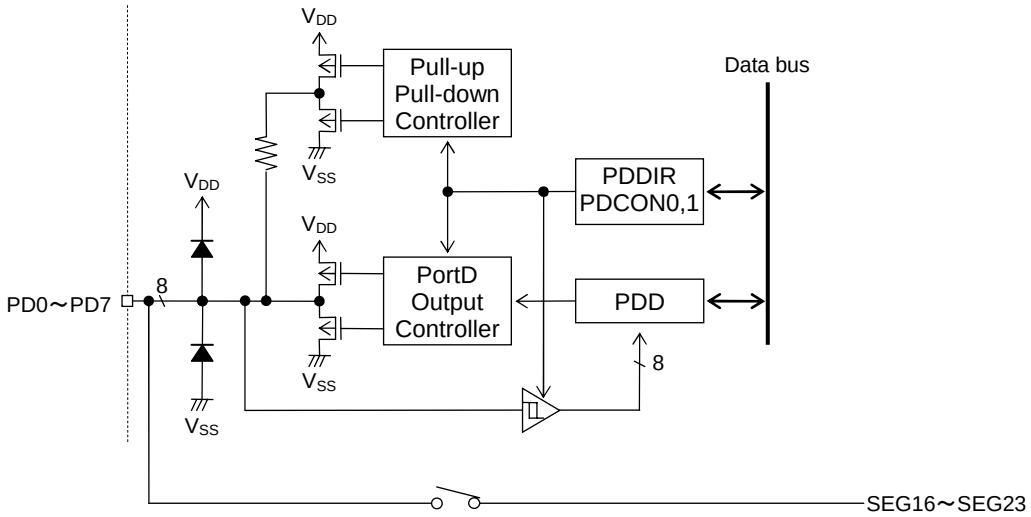
24.1 Overview

This LSI includes Port D (PD0 to PD7), which is a 8-bit input/output port.
Either an I/O Port or a segment driver output can be selected as a function of SEG16 to SEG23 by a LCD port segment selection register(LSELS2). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

24.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- Either an I/O Port or a segment driver output can be selected as a function of SEG16 to SEG23 by a LCD port segment selection register(LSELS2).

24.1.2 Configuration



PDD : Port D data register
PDDIR : Port D direction register
PDCON0 : Port D control register 0
PDCON1 : Port D control register 1

Figure 24-1 Configuration of Port D

24.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
PD0	I/O	Input/output port	SEG16
PD1	I/O	Input/output port	SEG17
PD2	I/O	Input/output port	SEG18
PD3	I/O	Input/output port	SEG19
PD4	I/O	Input/output port	SEG20
PD5	I/O	Input/output port	SEG21
PD6	I/O	Input/output port	SEG22
PD7	I/O	Input/output port	SEG23

24.2 Description of Registers

24.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F268H	Port D data register	PDD	—	R/W	8	00H
0F269H	Port D direction register	PDDIR	—	R/W	8	00H
0F26AH	Port D control register 0	PDCON0	PDCON	R/W	8/16	00H
0F26BH	Port D control register 1	PDCON1		R/W	8	00H

24.2.2 Port D data register (PDD)

Address: 0F268H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDD	PD7D	PD6D	PD5D	PD4D	PD3D	PD2D	PD1D	PD0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDD is a special function register (SFR) to set the value to be output to the Port D pin or to read the input level of the Port D. In output mode, the value of this register is output to the Port D pin. The value written to PDD is readable. In input mode, the input level of the Port D pin is read when PDD is read. Output mode or input mode is selected by using the port direction register (PDDIR) described later.

[Description of Bits]

- **PD7D-PD0D** (bits 7-0)
  The PD7D to PD0D bits are used to set the output value of the Port D pin in output mode and to read the pin level of the Port D pin in input mode.

PD7D	Description
0	Output or input level of the PD7 pin: "L"
1	Output or input level of the PD7 pin: "H"

PD6D	Description
0	Output or input level of the PD6 pin: "L"
1	Output or input level of the PD6 pin: "H"

PD5D	Description
0	Output or input level of the PD5 pin: "L"
1	Output or input level of the PD5 pin: "H"

PD4D	Description
0	Output or input level of the PD4 pin: "L"
1	Output or input level of the PD4 pin: "H"

PD3D	Description
0	Output or input level of the PD3 pin: "L"
1	Output or input level of the PD3 pin: "H"

PD2D	Description
0	Output or input level of the PD2 pin: "L"
1	Output or input level of the PD2 pin: "H"

PD1D	Description
0	Output or input level of the PD1 pin: "L"
1	Output or input level of the PD1 pin: "H"

PD0D	Description
0	Output or input level of the PD0 pin: "L"
1	Output or input level of the PD0 pin: "H"

24.2.3 Port D Direction Register (PDDIR)

Address: 0F269H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDDIR	PD7DIR	PD6DIR	PD5DIR	PD4DIR	PD3DIR	PD2DIR	PD1DIR	PD0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDDIR is a special function register (SFR) to select the input/output mode of Port D.

[Description of Bits]

- **PD7DIR-PD0DIR** (bits 7-0)
  The PD7DIR to PD0DIR pins are used to set the input/output direction of the Port D pin.

PD7DIR	Description
0	PD7 pin: Output (initial value)
1	PD7 pin: Input

PD6DIR	Description
0	PD6 pin: Output (initial value)
1	PD6 pin: Input

PD5DIR	Description
0	PD5 pin: Output (initial value)
1	PD5 pin: Input

PD4DIR	Description
0	PD4 pin: Output (initial value)
1	PD4 pin: Input

PD3DIR	Description
0	PD3 pin: Output (initial value)
1	PD3 pin: Input

PD2DIR	Description
0	PD2 pin: Output (initial value)
1	PD2 pin: Input

PD1DIR	Description
0	PD1 pin: Output (initial value)
1	PD1 pin: Input

PD0DIR	Description
0	PD0 pin: Output (initial value)
1	PD0 pin: Input

24.2.4 Port D control registers 0, 1 (PDCON0, PDCON1)

Address: 0F26AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDCON0	PD7C0	PD6C0	PD5C0	PD4C0	PD3C0	PD2C0	PD1C0	PD0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F26BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDCON1	PD7C1	PD6C1	PD5C1	PD4C1	PD3C1	PD2C1	PD1C1	PD0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDCON0 and PDCON1 are special function registers (SFRs) to select input/output state of the Port D pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PDDIR register.

[Description of Bits]

- **PD7C1-PD0C1, PD7C0-PD0C0** (bits 7-0)
  The PD7C1 to PD0C1 pins and the PD7C0 to PD0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (PD7DIR bit = "0")	When input mode is selected (PD7DIR bit = "1")
PD7C1	**PD7C0**	Description	
0	0	PD7 pin: High-impedance output (initial value)	PD7 pin: High-impedance input
0	1	PD7 pin: P-channel open drain output	PD7 pin: Input with a pull-down resistor
1	0	PD7 pin: N-channel open drain output	PD7 pin: Input with a pull-up resistor
1	1	PD7 pin: CMOS output	PD7 pin: High-impedance input

		When output mode is selected (PD6DIR bit = "0")	When input mode is selected (PD6DIR bit = "1")
PD6C1	**PD6C0**	Description	
0	0	PD6 pin: High-impedance output (initial value)	PD6 pin: High-impedance input
0	1	PD6 pin: P-channel open drain output	PD6 pin: Input with a pull-down resistor
1	0	PD6 pin: N-channel open drain output	PD6 pin: Input with a pull-up resistor
1	1	PD6 pin: CMOS output	PD6 pin: High-impedance input

		When output mode is selected (PD5DIR bit = "0")	When input mode is selected (PD5DIR bit = "1")
PD5C1	**PD5C0**	Description	
0	0	PD5 pin: High-impedance output (initial value)	PD5 pin: High-impedance input
0	1	PD5 pin: P-channel open drain output	PD5 pin: Input with a pull-down resistor
1	0	PD5 pin: N-channel open drain output	PD5 pin: Input with a pull-up resistor
1	1	PD5 pin: CMOS output	PD5 pin: High-impedance input

		When output mode is selected (PD4DIR bit = "0")	When input mode is selected (PD4DIR bit = "1")
PD4C1	**PD4C0**	Description	
0	0	PD4 pin: High-impedance output (initial value)	PD4 pin: High-impedance input
0	1	PD4 pin: P-channel open drain output	PD4 pin: Input with a pull-down resistor
1	0	PD4 pin: N-channel open drain output	PD4 pin: Input with a pull-up resistor
1	1	PD4 pin: CMOS output	PD4 pin: High-impedance input

		When output mode is selected (PD3DIR bit = "0")	When input mode is selected (PD3DIR bit = "1")
PD3C1	**PD3C0**	Description	
0	0	PD3 pin: High-impedance output (initial value)	PD3 pin: High-impedance input
0	1	PD3 pin: P-channel open drain output	PD3 pin: Input with a pull-down resistor
1	0	PD3 pin: N-channel open drain output	PD3 pin: Input with a pull-up resistor
1	1	PD3 pin: CMOS output	PD3 pin: High-impedance input

		When output mode is selected (PD2DIR bit = "0")	When input mode is selected (PD2DIR bit = "1")
PD2C1	**PD2C0**	Description	
0	0	PD2 pin: High-impedance output (initial value)	PD2 pin: High-impedance input
0	1	PD2 pin: P-channel open drain output	PD2 pin: Input with a pull-down resistor
1	0	PD2 pin: N-channel open drain output	PD2 pin: Input with a pull-up resistor
1	1	PD2 pin: CMOS output	PD2 pin: High-impedance input

		When output mode is selected (PD1DIR bit = "0")	When input mode is selected (PD1DIR bit = "1")
PD1C1	**PD1C0**	Description	
0	0	PD1 pin: High-impedance output (initial value)	PD1 pin: High-impedance input
0	1	PD1 pin: P-channel open drain output	PD1 pin: Input with a pull-down resistor
1	0	PD1 pin: N-channel open drain output	PD1 pin: Input with a pull-up resistor
1	1	PD1 pin: CMOS output	PD1 pin: High-impedance input

		When output mode is selected (PD0DIR bit = "0")	When input mode is selected (PD0DIR bit = "1")
PD0C1	**PD0C0**	Description	
0	0	PD0 pin: High-impedance output (initial value)	PD0 pin: High-impedance input
0	1	PD0 pin: P-channel open drain output	PD0 pin: Input with a pull-down resistor
1	0	PD0 pin: N-channel open drain output	PD0 pin: Input with a pull-up resistor
1	1	PD0 pin: CMOS output	PD0 pin: High-impedance input

24.3 Description of Operation

24.3.1 Input/Output Port Functions

For each pin of Port D, either output or input is selected by setting the Port D direction register (PDDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port D control registers 0 and 1 (PDCON0 and PDCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port D control registers 0 and 1 (PDCON0 and PDCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port D depending on the value set by the Port D data register (PDD).
In input mode, the input level of each pin of Port D can be read from the Port D data register (PDD).

Note:
Either an I/O Port or a segment driver output can be selected as a function of SEG16 to SEG23 by a LCD port segment selection register(LSELS2). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

Chapter 25

Port E

25. Port E

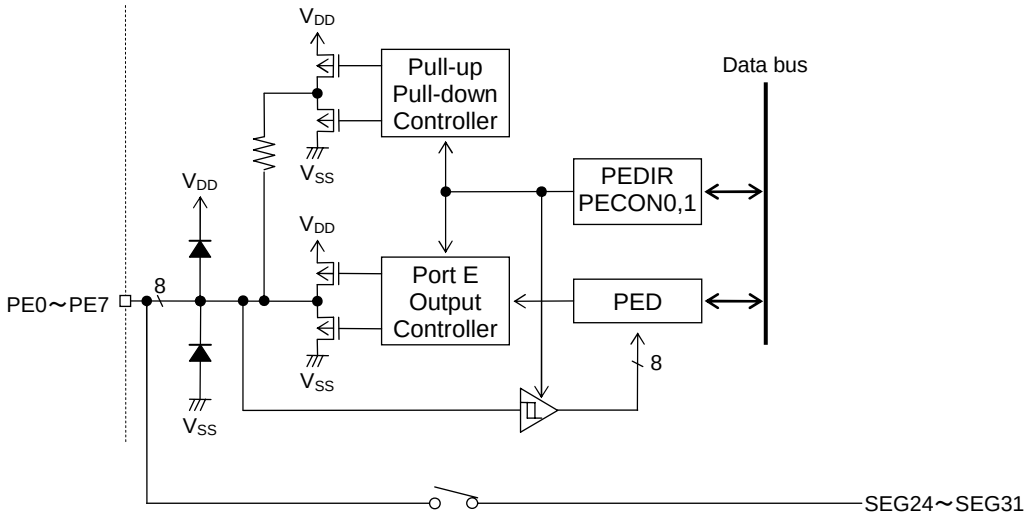
25.1 Overview

This LSI includes Port E (PE0 to PE7), which is a 8-bit input/output port.
Either an I/O Port or a segment driver output can be selected as a function of SEG24 to SEG31 by a LCD port segment selection register(LSELS3). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

25.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- Either an I/O Port or a segment driver output can be selected as a function of SEG24 to SEG31 by a LCD port segment selection register(LSELS3).

25.1.2 Configuration



PED : Port E data register
PEDIR : Port E direction register
PECON0 : Port E control register 0
PECON1 : Port E control register 1

Figure 25-1 Configuration of Port E

25.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
PE0	I/O	Input/output port	SEG24
PE1	I/O	Input/output port	SEG25
PE2	I/O	Input/output port	SEG26
PE3	I/O	Input/output port	SEG27
PE4	I/O	Input/output port	SEG28
PE5	I/O	Input/output port	SEG29
PE6	I/O	Input/output port	SEG30
PE7	I/O	Input/output port	SEG31

25.2 Description of Registers

25.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F270H	Port E data register	PED	—	R/W	8	00H
0F271H	Port E direction register	PEDIR	—	R/W	8	00H
0F272H	Port E control register 0	PECON0	PECON	R/W	8/16	00H
0F273H	Port E control register 1	PECON1		R/W	8	00H

25.2.2 Port E data register (PED)

Address: 0F270H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PED	PE7D	PE6D	PE5D	PE4D	PE3D	PE2D	PE1D	PE0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PED is a special function register (SFR) to set the value to be output to the Port E pin or to read the input level of the Port E. In output mode, the value of this register is output to the Port E pin. The value written to PED is readable. In input mode, the input level of the Port E pin is read when PED is read. Output mode or input mode is selected by using the Port Eirection register (PEDIR) described later.

[Description of Bits]

- **PE7D-PE0D** (bits 7-0)
  The PE7D to PE0D bits are used to set the output value of the Port E pin in output mode and to read the pin level of the Port E pin in input mode.

PE7D	Description
0	Output or input level of the PE7 pin: "L"
1	Output or input level of the PE7 pin: "H"

PE6D	Description
0	Output or input level of the PE6 pin: "L"
1	Output or input level of the PE6 pin: "H"

PE5D	Description
0	Output or input level of the PE5 pin: "L"
1	Output or input level of the PE5 pin: "H"

PE4D	Description
0	Output or input level of the PE4 pin: "L"
1	Output or input level of the PE4 pin: "H"

PE3D	Description
0	Output or input level of the PE3 pin: "L"
1	Output or input level of the PE3 pin: "H"

PE2D	Description
0	Output or input level of the PE2 pin: "L"
1	Output or input level of the PE2 pin: "H"

PE1D	Description
0	Output or input level of the PE1 pin: "L"
1	Output or input level of the PE1 pin: "H"

PE0D	Description
0	Output or input level of the PE0 pin: "L"
1	Output or input level of the PE0 pin: "H"

25.2.3 Port E Direction Register (PEDIR)

Address: 0F271H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PEDIR	PE7DIR	PE6DIR	PE5DIR	PE4DIR	PE3DIR	PE2DIR	PE1DIR	PE0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PEDIR is a special function register (SFR) to select the input/output mode of Port E.

[Description of Bits]

- **PE7DIR-PE0DIR** (bits 7-0)
  The PE7DIR to PE0DIR pins are used to set the input/output direction of the Port E pin.

PE7DIR	Description
0	PE7 pin: Output (initial value)
1	PE7 pin: Input

PE6DIR	Description
0	PE6 pin: Output (initial value)
1	PE6 pin: Input

PE5DIR	Description
0	PE5 pin: Output (initial value)
1	PE5 pin: Input

PE4DIR	Description
0	PE4 pin: Output (initial value)
1	PE4 pin: Input

PE3DIR	Description
0	PE3 pin: Output (initial value)
1	PE3 pin: Input

PE2DIR	Description
0	PE2 pin: Output (initial value)
1	PE2 pin: Input

PE1DIR	Description
0	PE1 pin: Output (initial value)
1	PE1 pin: Input

PE0DIR	Description
0	PE0 pin: Output (initial value)
1	PE0 pin: Input

25.2.4 Port E control registers 0, 1 (PECON0, PECON1)

Address: 0F272H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PECON0	PE7C0	PE6C0	PE5C0	PE4C0	PE3C0	PE2C0	PE1C0	PE0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F273H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PECON1	PE7C1	PE6C1	PE5C1	PE4C1	PE3C1	PE2C1	PE1C1	PE0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PECON0 and PECON1 are special function registers (SFRs) to select input/output state of the Port E pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PEDIR register.

[Description of Bits]

- **PE7C1-PE0C1, PE7C0-PE0C0** (bits 7-0)
  The PE7C1 to PE0C1 pins and the PE7C0 to PE0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (PE7DIR bit = "0")	When input mode is selected (PE7DIR bit = "1")
PE7C1	**PE7C0**	Description	
0	0	PE7 pin: High-impedance output (initial value)	PE7 pin: High-impedance input
0	1	PE7 pin: P-channel open drain output	PE7 pin: Input with a pull-down resistor
1	0	PE7 pin: N-channel open drain output	PE7 pin: Input with a pull-up resistor
1	1	PE7 pin: CMOS output	PE7 pin: High-impedance input

		When output mode is selected (PE6DIR bit = "0")	When input mode is selected (PE6DIR bit = "1")
PE6C1	**PE6C0**	Description	
0	0	PE6 pin: High-impedance output (initial value)	PE6 pin: High-impedance input
0	1	PE6 pin: P-channel open drain output	PE6 pin: Input with a pull-down resistor
1	0	PE6 pin: N-channel open drain output	PE6 pin: Input with a pull-up resistor
1	1	PE6 pin: CMOS output	PE6 pin: High-impedance input

		When output mode is selected (PE5DIR bit = "0")	When input mode is selected (PE5DIR bit = "1")
PE5C1	**PE5C0**	Description	
0	0	PE5 pin: High-impedance output (initial value)	PE5 pin: High-impedance input
0	1	PE5 pin: P-channel open drain output	PE5 pin: Input with a pull-down resistor
1	0	PE5 pin: N-channel open drain output	PE5 pin: Input with a pull-up resistor
1	1	PE5 pin: CMOS output	PE5 pin: High-impedance input

		When output mode is selected (PE4DIR bit = "0")	When input mode is selected (PE4DIR bit = "1")
PE4C1	**PE4C0**	Description	
0	0	PE4 pin: High-impedance output (initial value)	PE4 pin: High-impedance input
0	1	PE4 pin: P-channel open drain output	PE4 pin: Input with a pull-down resistor
1	0	PE4 pin: N-channel open drain output	PE4 pin: Input with a pull-up resistor
1	1	PE4 pin: CMOS output	PE4 pin: High-impedance input

		When output mode is selected (PE3DIR bit = "0")	When input mode is selected (PE3DIR bit = "1")
PE3C1	**PE3C0**	Description	
0	0	PE3 pin: High-impedance output (initial value)	PE3 pin: High-impedance input
0	1	PE3 pin: P-channel open drain output	PE3 pin: Input with a pull-down resistor
1	0	PE3 pin: N-channel open drain output	PE3 pin: Input with a pull-up resistor
1	1	PE3 pin: CMOS output	PE3 pin: High-impedance input

		When output mode is selected (PE2DIR bit = "0")	When input mode is selected (PE2DIR bit = "1")
PE2C1	**PE2C0**	Description	
0	0	PE2 pin: High-impedance output (initial value)	PE2 pin: High-impedance input
0	1	PE2 pin: P-channel open drain output	PE2 pin: Input with a pull-down resistor
1	0	PE2 pin: N-channel open drain output	PE2 pin: Input with a pull-up resistor
1	1	PE2 pin: CMOS output	PE2 pin: High-impedance input

		When output mode is selected (PE1DIR bit = "0")	When input mode is selected (PE1DIR bit = "1")
PE1C1	**PE1C0**	Description	
0	0	PE1 pin: High-impedance output (initial value)	PE1 pin: High-impedance input
0	1	PE1 pin: P-channel open drain output	PE1 pin: Input with a pull-down resistor
1	0	PE1 pin: N-channel open drain output	PE1 pin: Input with a pull-up resistor
1	1	PE1 pin: CMOS output	PE1 pin: High-impedance input

		When output mode is selected (PE0DIR bit = "0")	When input mode is selected (PE0DIR bit = "1")
PE0C1	**PE0C0**	Description	
0	0	PE0 pin: High-impedance output (initial value)	PE0 pin: High-impedance input
0	1	PE0 pin: P-channel open drain output	PE0 pin: Input with a pull-down resistor
1	0	PE0 pin: N-channel open drain output	PE0 pin: Input with a pull-up resistor
1	1	PE0 pin: CMOS output	PE0 pin: High-impedance input

25.3 Description of Operation

25.3.1 Input/Output Port Functions

For each pin of Port E, either output or input is selected by setting the Port E direction register (PEDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port E control registers 0 and 1 (PECON0 and PECON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port E control registers 0 and 1 (PECON0 and PECON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port E depending on the value set by the Port E data register (PED).
In input mode, the input level of each pin of Port E can be read from the Port E data register (PED).

Note:
Either an I/O Port or a segment driver output can be selected as a function of SEG24 to SEG31 by a LCD port segment selection register(LSELS3). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

Chapter 26

Port F

26. Port F

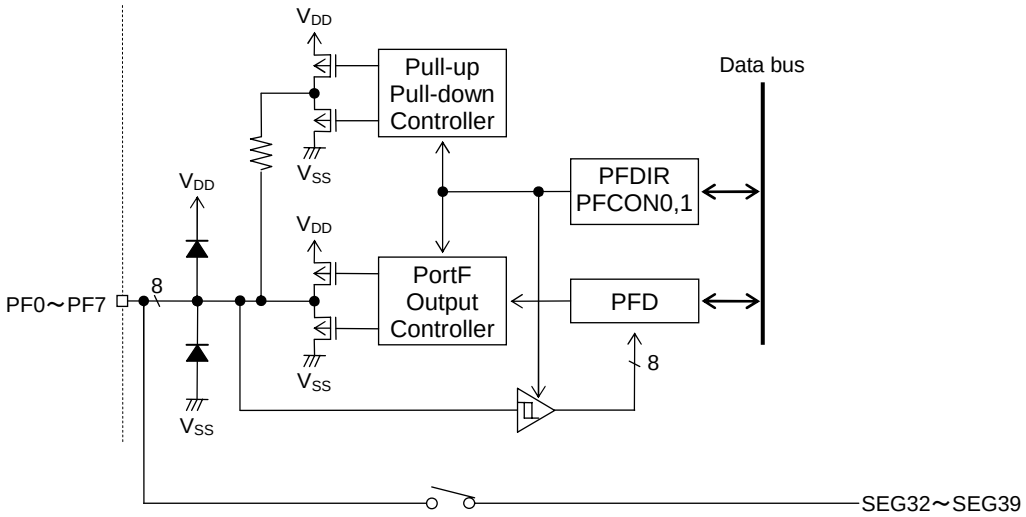
26.1 Overview

This LSI includes Port F (PF0 to PF7), which is a 8-bit input/output port.
Either an I/O Port or a segment driver output can be selected as a function of SEG32 to SEG39 by a LCD port segment selection register(LSELS4). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

26.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- Either an I/O Port or a segment driver output can be selected as a function of SEG32 to SEG39 by a LCD port segment selection register(LSELS4).

26.1.2 Configuration



PFD	: Port F data register
PFDIR	: Port F direction register
PFCON0	: Port F control register 0
PFCON1	: Port F control register 1

Figure 26-1 Configuration of Port F

26.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
PF0	I/O	Input/output port	SEG32
PF1	I/O	Input/output port	SEG33
PF2	I/O	Input/output port	SEG34
PF3	I/O	Input/output port	SEG35
PF4	I/O	Input/output port	SEG36
PF5	I/O	Input/output port	SEG37
PF6	I/O	Input/output port	SEG38
PF7	I/O	Input/output port	SEG39

26.2 Description of Registers

26.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F278H	Port F data register	PFD	—	R/W	8	00H
0F279H	Port F direction register	PFDIR	—	R/W	8	00H
0F27AH	Port F control register 0	PFCON0	PFCON	R/W	8/16	00H
0F27BH	Port F control register 1	PFCON1		R/W	8	00H

26.2.2 Port F data register (PFD)

Address: 0F278H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PFD	PF7D	PF6D	PF5D	PF4D	PF3D	PF2D	PF1D	PF0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PFD is a special function register (SFR) to set the value to be output to the Port F pin or to read the input level of the Port F. In output mode, the value of this register is output to the Port F pin. The value written to PFD is readable. In input mode, the input level of the Port F pin is read when PFD is read. Output mode or input mode is selected by using the Port Firection register (PFDIR) described later.

[Description of Bits]

- **PF7D-PF0D** (bits 7-0)
  The PF7D to PF0D bits are used to set the output value of the Port F pin in output mode and to read the pin level of the Port F pin in input mode.

PF7D	Description
0	Output or input level of the PF7 pin: "L"
1	Output or input level of the PF7 pin: "H"

PF6D	Description
0	Output or input level of the PF6 pin: "L"
1	Output or input level of the PF6 pin: "H"

PF5D	Description
0	Output or input level of the PF5 pin: "L"
1	Output or input level of the PF5 pin: "H"

PF4D	Description
0	Output or input level of the PF4 pin: "L"
1	Output or input level of the PF4 pin: "H"

PF3D	Description
0	Output or input level of the PF3 pin: "L"
1	Output or input level of the PF3 pin: "H"

PF2D	Description
0	Output or input level of the PF2 pin: "L"
1	Output or input level of the PF2 pin: "H"

PF1D	Description
0	Output or input level of the PF1 pin: "L"
1	Output or input level of the PF1 pin: "H"

PF0D	Description
0	Output or input level of the PF0 pin: "L"
1	Output or input level of the PF0 pin: "H"

26.2.3 Port F Direction Register (PFDIR)

Address: 0F279H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PFDIR	PF7DIR	PF6DIR	PF5DIR	PF4DIR	PF3DIR	PF2DIR	PF1DIR	PF0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PFDIR is a special function register (SFR) to select the input/output mode of Port F.

[Description of Bits]

- **PF7DIR-PF0DIR** (bits 7-0)
  The PF7DIR to PF0DIR pins are used to set the input/output direction of the Port F pin.

PF7DIR	Description
0	PF7 pin: Output (initial value)
1	PF7 pin: Input

PF6DIR	Description
0	PF6 pin: Output (initial value)
1	PF6 pin: Input

PF5DIR	Description
0	PF5 pin: Output (initial value)
1	PF5 pin: Input

PF4DIR	Description
0	PF4 pin: Output (initial value)
1	PF4 pin: Input

PF3DIR	Description
0	PF3 pin: Output (initial value)
1	PF3 pin: Input

PF2DIR	Description
0	PF2 pin: Output (initial value)
1	PF2 pin: Input

PF1DIR	Description
0	PF1 pin: Output (initial value)
1	PF1 pin: Input

PF0DIR	Description
0	PF0 pin: Output (initial value)
1	PF0 pin: Input

26.2.4 Port F control registers 0, 1 (PFCON0, PFCON1)

Address: 0F27AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PFCON0	PF7C0	PF6C0	PF5C0	PF4C0	PF3C0	PF2C0	PF1C0	PF0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F27BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PFCON1	PF7C1	PF6C1	PF5C1	PF4C1	PF3C1	PF2C1	PF1C1	PF0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PFCON0 and PFCON1 are special function registers (SFRs) to select input/output state of the Port F pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PFDIR register.

[Description of Bits]

- **PF7C1-PF0C1, PF7C0-PF0C0** (bits 7-0)
  The PF7C1 to PF0C1 pins and the PF7C0 to PF0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (PF7DIR bit = "0")	When input mode is selected (PF7DIR bit = "1")
PF7C1	**PF7C0**	Description	
0	0	PF7 pin: High-impedance output (initial value)	PF7 pin: High-impedance input
0	1	PF7 pin: P-channel open drain output	PF7 pin: Input with a pull-down resistor
1	0	PF7 pin: N-channel open drain output	PF7 pin: Input with a pull-up resistor
1	1	PF7 pin: CMOS output	PF7 pin: High-impedance input

		When output mode is selected (PF6DIR bit = "0")	When input mode is selected (PF6DIR bit = "1")
PF6C1	**PF6C0**	Description	
0	0	PF6 pin: High-impedance output (initial value)	PF6 pin: High-impedance input
0	1	PF6 pin: P-channel open drain output	PF6 pin: Input with a pull-down resistor
1	0	PF6 pin: N-channel open drain output	PF6 pin: Input with a pull-up resistor
1	1	PF6 pin: CMOS output	PF6 pin: High-impedance input

		When output mode is selected (PF5DIR bit = "0")	When input mode is selected (PF5DIR bit = "1")
PF5C1	**PF5C0**	Description	
0	0	PF5 pin: High-impedance output (initial value)	PF5 pin: High-impedance input
0	1	PF5 pin: P-channel open drain output	PF5 pin: Input with a pull-down resistor
1	0	PF5 pin: N-channel open drain output	PF5 pin: Input with a pull-up resistor
1	1	PF5 pin: CMOS output	PF5 pin: High-impedance input

		When output mode is selected (PF4DIR bit = "0")	When input mode is selected (PF4DIR bit = "1")
PF4C1	**PF4C0**	Description	
0	0	PF4 pin: High-impedance output (initial value)	PF4 pin: High-impedance input
0	1	PF4 pin: P-channel open drain output	PF4 pin: Input with a pull-down resistor
1	0	PF4 pin: N-channel open drain output	PF4 pin: Input with a pull-up resistor
1	1	PF4 pin: CMOS output	PF4 pin: High-impedance input

		When output mode is selected (PF3DIR bit = "0")	When input mode is selected (PF3DIR bit = "1")
PF3C1	**PF3C0**	Description	
0	0	PF3 pin: High-impedance output (initial value)	PF3 pin: High-impedance input
0	1	PF3 pin: P-channel open drain output	PF3 pin: Input with a pull-down resistor
1	0	PF3 pin: N-channel open drain output	PF3 pin: Input with a pull-up resistor
1	1	PF3 pin: CMOS output	PF3 pin: High-impedance input

		When output mode is selected (PF2DIR bit = "0")	When input mode is selected (PF2DIR bit = "1")
PF2C1	**PF2C0**	Description	
0	0	PF2 pin: High-impedance output (initial value)	PF2 pin: High-impedance input
0	1	PF2 pin: P-channel open drain output	PF2 pin: Input with a pull-down resistor
1	0	PF2 pin: N-channel open drain output	PF2 pin: Input with a pull-up resistor
1	1	PF2 pin: CMOS output	PF2 pin: High-impedance input

		When output mode is selected (PF1DIR bit = "0")	When input mode is selected (PF1DIR bit = "1")
PF1C1	**PF1C0**	Description	
0	0	PF1 pin: High-impedance output (initial value)	PF1 pin: High-impedance input
0	1	PF1 pin: P-channel open drain output	PF1 pin: Input with a pull-down resistor
1	0	PF1 pin: N-channel open drain output	PF1 pin: Input with a pull-up resistor
1	1	PF1 pin: CMOS output	PF1 pin: High-impedance input

		When output mode is selected (PF0DIR bit = "0")	When input mode is selected (PF0DIR bit = "1")
PF0C1	**PF0C0**	Description	
0	0	PF0 pin: High-impedance output (initial value)	PF0 pin: High-impedance input
0	1	PF0 pin: P-channel open drain output	PF0 pin: Input with a pull-down resistor
1	0	PF0 pin: N-channel open drain output	PF0 pin: Input with a pull-up resistor
1	1	PF0 pin: CMOS output	PF0 pin: High-impedance input

26.3 Description of Operation

26.3.1 Input/Output Port Functions

For each pin of Port F, either output or input is selected by setting the Port F direction register (PFDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port F control registers 0 and 1 (PFCON0 and PFCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port F control registers 0 and 1 (PFCON0 and PFCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port F depending on the value set by the Port F data register (PFD).
In input mode, the input level of each pin of Port F can be read from the Port F data register (PFD).

Note:
Either an I/O Port or a segment driver output can be selected as a function of SEG32 to SEG39 by a LCD port segment selection register(LSELS4). For details of the LCD driver, refer to the "Chapter 27 LCD driver".

Chapter 27

LCD Drivers

27. LCD Drivers

27.1 Overview

This LSI includes LCD drivers that display the contents that are set in the display register.
The LCD drivers handle the LCD display functions with three blocks.

1. Display registers
2. Display control
3. Drivers

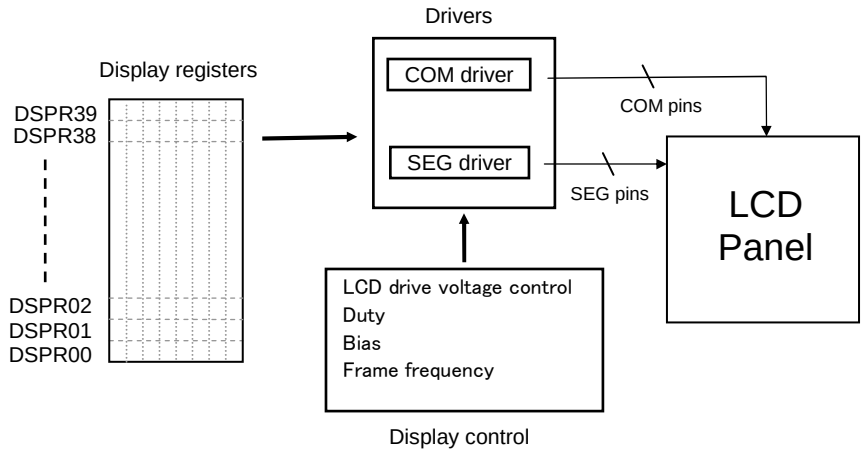


Figure 27-1 Configuration of LCD Display Function

The display registers are used to store the contents to be displayed as bit patterns.
The bit patterns depends on the specification of the LCD panel to be used (display pattern and assignment of the COM pin and SEG pin).

The display control circuit generates LCD drive waveforms according to the characteristics of the LCD.
A duty, a frame frequency suitable for the LCD panel can be selected.
SEG8 to SEG39 pins can be used also as I/O port. When not using a LCD display function, it can be used as an I/O Port.

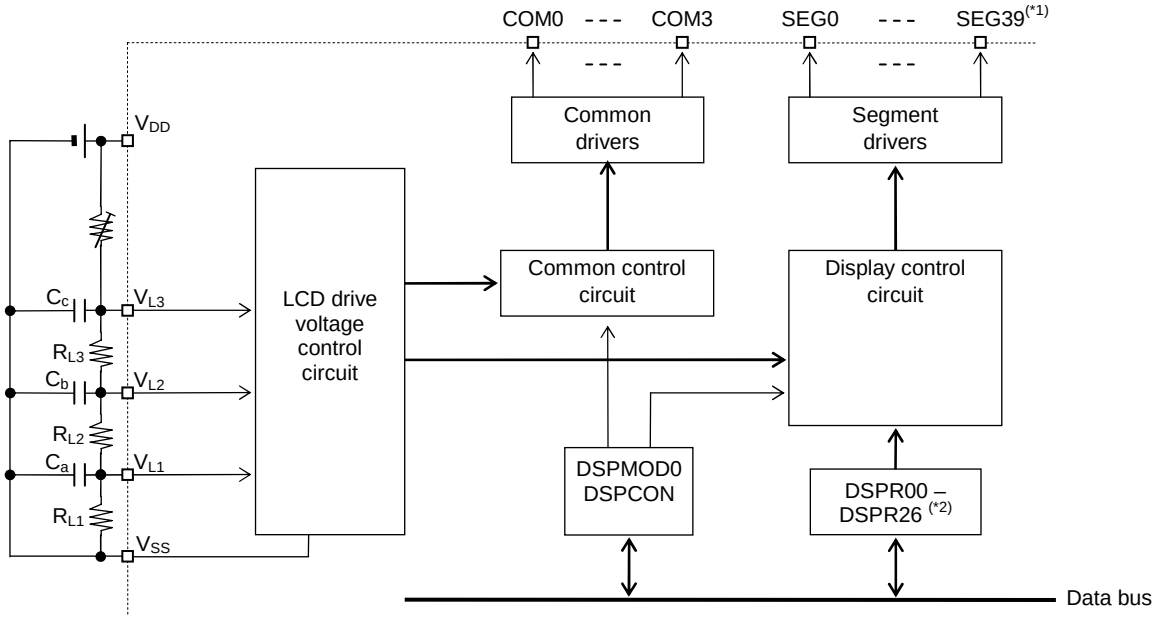
27.1.1 Features

The LCD drivers are applicable to various types of LCD panels. The features include:

- 160 dots max. (40seg x 4com)
- 1/1 to 1/4 duty
- 1/2, 1/3bias
- Frame frequency selectable (8 types)
- "ALL LCDs on" mode and "ALL LCDs off" mode.
- "SEG port output: SEG ports can be individually selected in a segment output function or a I/O port function.

27.1.2 Configuration of the LCD Drivers

Figure 27-2 shows the configuration of the LCD drivers and the bias generation circuit.



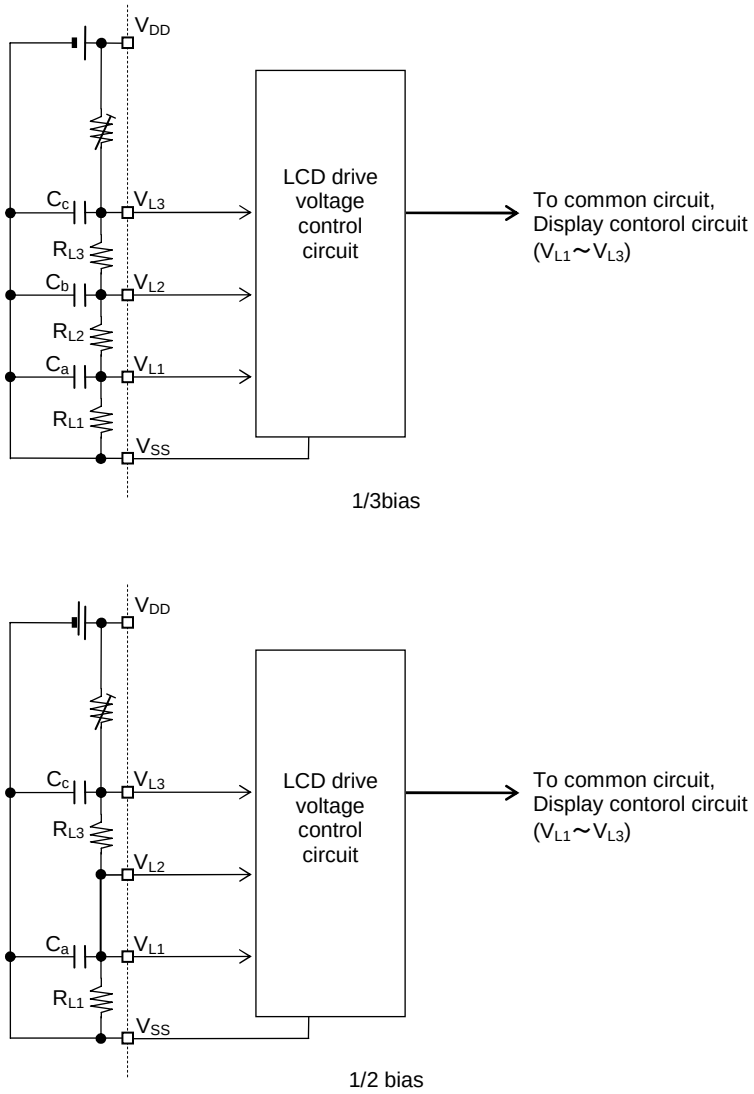
(*1) combination SEG port and I/O port.

DSPMOD0	: Display mode register 0
DSPCON	: Display control register
DSPR00 to DSPR26	: Display registers

Figure 27-2 Configuration of LCD Drivers

27.1.3 Configuration of the LCD drive voltage control circuit

Connect external partial pressure resistance to the power supply terminal for LCD drivers (V_{L1}toV_{L3}), and impress LCD driver drive voltage..
Figure 27-3 shows the configurations of the LCD drive voltage control circuit..



27-3 Configuration of the LCD drive voltage control circuit

Note;
The recommendation value of R_{L1} to R_{L3} is 200kΩ and the recommendation value of Ca to C_C is 0.22 µF.
Adjust a value according to the LCD panel, the number of segment pins, the number of common pins, and frame frequency to be used.

27.1.4 List of Pins

Pin name	I/O	Description
V_{L1}	—	Power supply pin for LCD bias
V_{L2}	—	Power supply pin for LCD bias
V_{L3}	—	Power supply pin for LCD bias
COM0	O	LCD common pin
COM1	O	LCD common pin
COM2	O	LCD common pin
COM3	O	LCD common pin
SEG0	O	LCD segment pin
SEG1	O	LCD segment pin
SEG2	O	LCD segment pin
SEG3	O	LCD segment pin
SEG4	O	LCD segment pin
SEG5	O	LCD segment pin
SEG6	O	LCD segment pin
SEG7	O	LCD segment pin
PC0/SEG8	O	LCD segment pin
PC1/SEG9	O	LCD segment pin
PC2/SEG10	O	LCD segment pin
PC3/SEG11	O	LCD segment pin
PC4/SEG12	O	LCD segment pin
PC5/SEG13	O	LCD segment pin
PC6/SEG14	O	LCD segment pin
PC7/SEG15	O	LCD segment pin
PD0/SEG16	O	LCD segment pin
PD1/SEG17	O	LCD segment pin
PD2/SEG18	O	LCD segment pin
PD3/SEG19	O	LCD segment pin
PD4/SEG20	O	LCD segment pin
PD5/SEG21	O	LCD segment pin
PD6/SEG22	O	LCD segment pin
PD7/SEG23	O	LCD segment pin
PE0/SEG24	O	LCD segment pin
PE1/SEG25	O	LCD segment pin
PE2/SEG26	O	LCD segment pin
PE3/SEG27	O	LCD segment pin
PE4/SEG28	O	LCD segment pin
PE5/SEG29	O	LCD segment pin
PE6/SEG30	O	LCD segment pin
PE7/SEG31	O	LCD segment pin
PF0/SEG32	O	LCD segment pin
PF1/SEG33	O	LCD segment pin
PF2/SEG34	O	LCD segment pin
PF3/SEG35	O	LCD segment pin
PF4/SEG36	O	LCD segment pin
PF5/SEG37	O	LCD segment pin
PF6/SEG38	O	LCD segment pin
PF7/SEG39	O	LCD segment pin

27.2 Description of Registers

27.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0F0H	Bias circuit control register	BIASCON	—	R/W	8	30H
0F0F2H	Display mode register 0	DSPMOD0	—	R/W	8	00H
0F0F4H	Display control register	DSPCON	—	R/W	8	00H
0F100H to 0F127H	Display register 00 to Display register 27	DSPR00 to DSPR27	—	R/W	8	00H
0F8F1H	LCD port segment selection register 1	LSELS1	—	R/W	8	00H
0F8F2H	LCD port segment selection register 2	LSELS2	—	R/W	8	00H
0F8F3H	LCD port segment selection register 3	LSELS3	—	R/W	8	00H
0F8F4H	LCD port segment selection register 4	LSELS4	—	R/W	8	00H

27.2.2 Bias Circuit Control Register 0 (BIASCON)

Address: 0F0F0H
Access: R/W
Access size: 8 bits
Initial value: 30H

	7	6	5	4	3	2	1	0
BIASCON	—	—	BSEL1	BSEL0	—	—	—	—
R/W	R	R	R/W	R/W	R	R	R	R
Initial value	0	0	1	1	0	0	0	0

BIASCON is a special function register (SFR) to control the bias generation circuit.

[Description of Bits]

- **BSEL** (bit 5 to 4)
  The BSEL bit sets up the bias of a bias generating circuit.
  1/2 bias or 1/3 bias can be chosen..

BSEL1	BSEL0	Description
0	0	1/3 bias
0	1	Prohibited
1	0	Prohibited
1	1	1/2 bias (initial value)

27.2.3 Display Mode Register 0 (DSPMOD0)

Address: 0F0F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPMOD0	FRM2	FRM1	FRM0	—	—	—	DUTY1	DUTY0
R/W	R/W	R/W	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPMOD0 is a special function register (SFR) to control the display mode of the LCD drivers.

[Description of Bits]

- **DUTY1-DUTY0** (bits 1-0)

The DUTY1 to DUTY0 bits are used to specify the duty in 4steps (1/1 to 1/4).

DUTY1	DUTY0	Description
0	0	1/1 duty (initial value)
0	1	1/2 duty
1	0	1/3 duty
1	1	1/4 duty

- **FRM1-FRM0** (bits 7-5)

The FRM2 to FRM0 bits are used to select a frame frequency of the LCD drivers.

FRM2	FRM1	FRM0	Description
0	0	0	Reference frequency: 64 Hz (initial value)
0	0	1	Reference frequency: 73 Hz
0	1	0	Reference frequency: 85 Hz
0	1	1	Reference frequency: 102 Hz
1	0	0	Reference frequency: 32 Hz
1	0	1	Reference frequency: 128 Hz
1	1	0	Reference frequency: 171 Hz
1	1	1	Reference frequency: 256 Hz

Table 27-1-1 Frame Frequency for Each Duty

Duty	Frame frequency [Hz]			
	Reference frequency 64Hz	Reference frequency 73Hz	Reference frequency 85Hz	Reference frequency 102Hz
1/1 duty	64.00	73.14	85.33	102.40
1/2 duty	64.00	73.14	85.33	102.40
1/3 duty	64.25	73.31	85.33	103.04
1/4 duty	64.00	73.14	85.33	102.40

Duty	Frame frequency [Hz]			
	Reference frequency 32Hz	Reference frequency 128Hz	Reference frequency 171Hz	Reference frequency 256Hz
1/1 duty	32.00	128.00	170.67	256.00
1/2 duty	32.00	128.00	170.67	256.00
1/3 duty	32.13	128.50	170.67	256.02
1/4 duty	32.00	128.00	170.67	256.00

27.2.4 Display Control Register (DSPCON)

Address: 0F0F4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPCON	—	—	—	—	—	—	LMD1	LMD0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPCON is a special function register (SFR) to control the LCD drivers.

[Description of Bits]

- **LMD1-LMD0** (bits 1, 0)
  The LMD1 and LMD0 bits are used to select an LCD display mode.
  LCD stop mode, all LCDs off mode, LCD display mode, and all LCDs on mode can be selected.
  In LCD stop mode, V_{ss} level is output to all the common drivers and segment drivers. The charge and discharge current to and from the display panel can be stopped.
  In all LCDs off mode, off waveform is output to all the segment drivers irrespective of the contents of the display registers.
  In LCD display mode, the contents of the display registers are output to each segment driver.
  In all LCDs on mode, on waveform is output to all the segment drivers irrespective of the contents of the display registers.

LMD1	LMD0	Description
0	0	LCD stop mode (initial value)
0	1	All LCDs off mode
1	0	LCD display mode
1	1	All LCDs on mode

27.2.5 Display Registers (DSPR00 to DSPR27)

Address: 0F100H to 0F127H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPRxx	—	—	—	—	c3	c2	c1	c0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPRxx (xx = 00 to 27) are special function registers (SFRs) to store display data.
Set data in DSPRxx before setting LCD display mode.
Table 27-2 list display registers.
[Description of Bits]

- **c3-c0** (bits 4-0)
  The c3 to c0 bits are used to set display data.

c3 to c0	Description
0	off waveform
1	on waveform

Table 27-4 Display Registers

Symbol	Address	Segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR00	0F100H	SEG0	-	-	-	-	c3	c2	c1	c0	R/W
DSPR01	0F101H	SEG1	-	-	-	-	c3	c2	c1	c0	R/W
DSPR02	0F102H	SEG2	-	-	-	-	c3	c2	c1	c0	R/W
DSPR03	0F103H	SEG3	-	-	-	-	c3	c2	c1	c0	R/W
DSPR04	0F104H	SEG4	-	-	-	-	c3	c2	c1	c0	R/W
DSPR05	0F105H	SEG5	-	-	-	-	c3	c2	c1	c0	R/W
DSPR06	0F106H	SEG6	-	-	-	-	c3	c2	c1	c0	R/W
DSPR07	0F107H	SEG7	-	-	-	-	c3	c2	c1	c0	R/W
DSPR08	0F108H	SEG8	-	-	-	-	c3	c2	c1	c0	R/W
DSPR09	0F109H	SEG9	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0A	0F10AH	SEG10	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0B	0F10BH	SEG11	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0C	0F10CH	SEG12	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0D	0F10DH	SEG13	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0E	0F10EH	SEG14	-	-	-	-	c3	c2	c1	c0	R/W
DSPR0F	0F10FH	SEG15	-	-	-	-	c3	c2	c1	c0	R/W
DSPR10	0F110H	SEG16	-	-	-	-	c3	c2	c1	c0	R/W
DSPR11	0F111H	SEG17	-	-	-	-	c3	c2	c1	c0	R/W
DSPR12	0F112H	SEG18	-	-	-	-	c3	c2	c1	c0	R/W
DSPR13	0F113H	SEG19	-	-	-	-	c3	c2	c1	c0	R/W
DSPR14	0F114H	SEG20	-	-	-	-	c3	c2	c1	c0	R/W
DSPR15	0F115H	SEG21	-	-	-	-	c3	c2	c1	c0	R/W
DSPR16	0F116H	SEG22	-	-	-	-	c3	c2	c1	c0	R/W
DSPR17	0F117H	SEG23	-	-	-	-	c3	c2	c1	c0	R/W
DSPR18	0F118H	SEG24	-	-	-	-	c3	c2	c1	c0	R/W
DSPR19	0F119H	SEG25	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1A	0F11AH	SEG26	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1B	0F11BH	SEG27	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1C	0F11CH	SEG28	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1D	0F11DH	SEG29	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1E	0F11EH	SEG30	-	-	-	-	c3	c2	c1	c0	R/W
DSPR1F	0F11FH	SEG31	-	-	-	-	c3	c2	c1	c0	R/W
DSPR20	0F120H	SEG32	-	-	-	-	c3	c2	c1	c0	R/W
DSPR21	0F121H	SEG33	-	-	-	-	c3	c2	c1	c0	R/W
DSPR22	0F122H	SEG34	-	-	-	-	c3	c2	c1	c0	R/W
DSPR23	0F123H	SEG35	-	-	-	-	c3	c2	c1	c0	R/W
DSPR24	0F124H	SEG36	-	-	-	-	c3	c2	c1	c0	R/W
DSPR25	0F125H	SEG37	-	-	-	-	c3	c2	c1	c0	R/W
DSPR26	0F126H	SEG38	-	-	-	-	c3	c2	c1	c0	R/W
DSPR27	0F127H	SEG39	-	-	-	-	c3	c2	c1	c0	R/W

27.2.6 LCD port segment selection register 1 (LSELS1)

Address: 0F8F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LSELS1	LSELS15	LSELS14	LSELS13	LSELS12	LSELS11	LSELS10	LSELS09	LSELS08
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LSELS1 is a Special function register which selects I/O Port (port C) or Segment driver output as a function of SEG8 to SEG15 port.
Set up LSELS1 before displaying LCD.

[Description of Bits]

- **LSELS15** (bits 7)

LSELS15 is a bit which selects I/O Port (PC7) or Segment driver output (SEG15) as a function of SEG15.

LSELS15	Description
0	Use as an I/O Port (PC7) (initial value)
1	Use as a segment driver output (SEG15)

- **LSELS14** (bits 6)

LSELS14 is a bit which selects I/O Port (PC6) or Segment driver output (SEG14) as a function of SEG14.

LSELS14	Description
0	Use as an I/O Port (PC6) (initial value)
1	Use as a segment driver output (SEG14)

- **LSELS13** (bits 5)

LSELS13 is a bit which selects I/O Port (PC5) or Segment driver output (SEG13) as a function of SEG13.

LSELS13	Description
0	Use as an I/O Port (PC5) (initial value)
1	Use as a segment driver output (SEG13)

- **LSELS12** (bits 4)

LSELS12 is a bit which selects I/O Port (PC4) or Segment driver output (SEG12) as a function of SEG12.

LSELS12	Description
0	Use as an I/O Port (PC4) (initial value)
1	Use as a segment driver output (SEG12)

- **LSELS11** (bits 3)

LSELS11 is a bit which selects I/O Port (PC3) or Segment driver output (SEG11) as a function of SEG11.

LSELS11	Description
0	Use as an I/O Port (PC3) (initial value)
1	Use as a segment driver output (SEG11)

- **LSELS10** (bits 2)

LSELS10 is a bit which selects I/O Port (PC2) or Segment driver output (SEG10) as a function of SEG10.

LSELS10	Description
0	Use as an I/O Port (PC2) (initial value)
1	Use as a segment driver output (SEG10)

- **LSELS09** (bits 1)

LSELS09 is a bit which selects I/O Port (PC1) or Segment driver output (SEG09) as a function of SEG09.

LSELS09	Description
0	Use as an I/O Port (PC1) (initial value)
1	Use as a segment driver output (SEG09)

- **LSELS08** (bits 0)

LSELS08 is a bit which selects I/O Port (PC0) or Segment driver output (SEG08) as a function of SEG08.

LSELS08	Description
0	Use as an I/O Port (PC0) (initial value)
1	Use as a segment driver output (SEG08)

27.2.7 LCD port segment selection register 2 (LSELS2)

Address: 0F8F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LSELS2	LSELS23	LSELS22	LSELS21	LSELS20	LSELS19	LSELS18	LSELS17	LSELS16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LSELS2 is a Special function register which selects I/O Port (port D) or Segment driver output as a function of SEG16 to SEG23 port.
Set up LSELS2 before displaying LCD.

[Description of Bits]

- **LSELS23** (bits 7)

LSELS23 is a bit which selects I/O Port (PD7) or Segment driver output (SEG23) as a function of SEG23.

LSELS23	Description
0	Use as an I/O Port (PD7) (initial value)
1	Use as a segment driver output (SEG23)

- **LSELS22** (bits 6)

LSELS22 is a bit which selects I/O Port (PD6) or Segment driver output (SEG22) as a function of SEG22.

LSELS22	Description
0	Use as an I/O Port (PD6) (initial value)
1	Use as a segment driver output (SEG22)

- **LSELS21** (bits 5)

LSELS21 is a bit which selects I/O Port (PD5) or Segment driver output (SEG21) as a function of SEG21.

LSELS21	Description
0	Use as an I/O Port (PD5) (initial value)
1	Use as a segment driver output (SEG21)

- **LSELS20** (bits 4)

LSELS20 is a bit which selects I/O Port (PD4) or Segment driver output (SEG20) as a function of SEG20.

LSELS20	Description
0	Use as an I/O Port (PD4) (initial value)
1	Use as a segment driver output (SEG20)

- **LSELS19**(bits 3)

LSELS19 is a bit which selects I/O Port (PD3) or Segment driver output (SEG19) as a function of SEG19.

LSELS19	Description
0	Use as an I/O Port (PD3) (initial value)
1	Use as a segment driver output (SEG19)

- **LSELS18** (bits 2)

LSELS18 is a bit which selects I/O Port (PD2) or Segment driver output (SEG18) as a function of SEG18.

LSELS18	Description
0	Use as an I/O Port (PD2) (initial value)
1	Use as a segment driver output (SEG18)

- **LSELS17** (bits 1)

LSELS17 is a bit which selects I/O Port (PD1) or Segment driver output (SEG17) as a function of SEG17.

LSELS17	Description
0	Use as an I/O Port (PD1) (initial value)
1	Use as a segment driver output (SEG17)

- **LSELS16** (bits 0)

LSELS16 is a bit which selects I/O Port (PD0) or Segment driver output (SEG16) as a function of SEG16.

LSELS16	Description
0	Use as an I/O Port (PD0) (initial value)
1	Use as a segment driver output (SEG16)

27.2.8 LCD port segment selection register 3 (LSELS3)

Address: 0F8F3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LSELS3	LSELS31	LSELS30	LSELS29	LSELS28	LSELS27	LSELS26	LSELS25	LSELS24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LSELS3 is a Special function register which selects I/O Port (port E) or Segment driver output as a function of SEG24 to SEG31 port.
Set up LSELS3 before displaying LCD.

[Description of Bits]

- **LSELS31** (bits 7)

LSELS31 is a bit which selects I/O Port (PE7) or Segment driver output (SEG31) as a function of SEG23.

LSELS31	Description
0	Use as an I/O Port (PE7) (initial value)
1	Use as a segment driver output (SEG31)

- **LSELS30** (bits 6)

LSELS30 is a bit which selects I/O Port (PE6) or Segment driver output (SEG30) as a function of SEG30.

LSELS30	Description
0	Use as an I/O Port (PE6) (initial value)
1	Use as a segment driver output (SEG30)

- **LSELS29** (bits 5)

LSELS29 is a bit which selects I/O Port (PE5) or Segment driver output (SEG29) as a function of SEG29.

LSELS29	Description
0	Use as an I/O Port (PE5) (initial value)
1	Use as a segment driver output (SEG29)

- **LSELS28** (bits 4)

LSELS28 is a bit which selects I/O Port (PE4) or Segment driver output (SEG28) as a function of SEG28.

LSELS20	Description
0	Use as an I/O Port (PE4) (initial value)
1	Use as a segment driver output (SEG20)

- **LSELS27**(bits 3)

LSELS27 is a bit which selects I/O Port (PE3) or Segment driver output (SEG27) as a function of SEG27.

LSELS27	Description
0	Use as an I/O Port (PE3) (initial value)
1	Use as a segment driver output (SEG27)

- **LSELS26** (bits 2)

LSELS26 is a bit which selects I/O Port (PE2) or Segment driver output (SEG26) as a function of SEG26.

LSELS26	Description
0	Use as an I/O Port (PE2) (initial value)
1	Use as a segment driver output (SEG26)

- **LSELS25** (bits 1)

LSELS25 is a bit which selects I/O Port (PE1) or Segment driver output (SEG25) as a function of SEG25.

LSELS25	Description
0	Use as an I/O Port (PE1) (initial value)
1	Use as a segment driver output (SEG25)

- **LSELS24** (bits 0)

LSELS24 is a bit which selects I/O Port (PE0) or Segment driver output (SEG24) as a function of SEG24.

LSELS24	Description
0	Use as an I/O Port (PE0) (initial value)
1	Use as a segment driver output (SEG24)

27.2.9 LCD port segment selection register 4 (LSELS4)

Address: 0F8F4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LSELS4	LSELS39	LSELS38	LSELS37	LSELS36	LSELS35	LSELS34	LSELS33	LSELS32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LSELS4 is a Special function register which selects I/O Port (port F) or Segment driver output as a function of SEG39 to SEG32 port.
Set up LSELS4 before displaying LCD.

[Description of Bits]

- **LSELS39** (bits 7)

LSELS39 is a bit which selects I/O Port (PF7) or Segment driver output (SEG39) as a function of SEG39.

LSELS39	Description
0	Use as an I/O Port (PF7) (initial value)
1	Use as a segment driver output (SEG39)

- **LSELS38** (bits 6)

LSELS38 is a bit which selects I/O Port (PF6) or Segment driver output (SEG38) as a function of SEG38.

LSELS38	Description
0	Use as an I/O Port (PF6) (initial value)
1	Use as a segment driver output (SEG38)

- **LSELS37** (bits 5)

LSELS21 is a bit which selects I/O Port (PF5) or Segment driver output (SEG37) as a function of SEG37.

LSELS37	Description
0	Use as an I/O Port (PF5) (initial value)
1	Use as a segment driver output (SEG37)

- **LSELS36** (bits 4)

LSELS36 is a bit which selects I/O Port (PF4) or Segment driver output (SEG36) as a function of SEG36.

LSELS36	Description
0	Use as an I/O Port (PF4) (initial value)
1	Use as a segment driver output (SEG36)

- **LSELS35**(bits 3)

LSELS35 is a bit which selects I/O Port (PF3) or Segment driver output (SEG35) as a function of SEG35.

LSELS35	Description
0	Use as an I/O Port (PF3) (initial value)
1	Use as a segment driver output (SEG35)

- **LSELS34** (bits 2)

LSELS34 is a bit which selects I/O Port (PF2) or Segment driver output (SEG34) as a function of SEG34.

LSELS34	Description
0	Use as an I/O Port (PF2) (initial value)
1	Use as a segment driver output (SEG34)

- **LSELS33**(bits 1)

LSELS33 is a bit which selects I/O Port (PF1) or Segment driver output (SEG34) as a function of SEG33.

LSELS33	Description
0	Use as an I/O Port (PF1) (initial value)
1	Use as a segment driver output (SEG33)

- **LSELS32** (bits 0)

LSELS32 is a bit which selects I/O Port (PF0) or Segment driver output (SEG32) as a function of SEG32.

LSELS32	Description
0	Use as an I/O Port (PF0) (initial value)
1	Use as a segment driver output (SEG32)

27.3 Description of Operation

27.3.1 Operation of LCD Drivers and Bias Generation Circuit

Figure 27-4 shows the operation of the LCD drivers and the bias generation circuit.

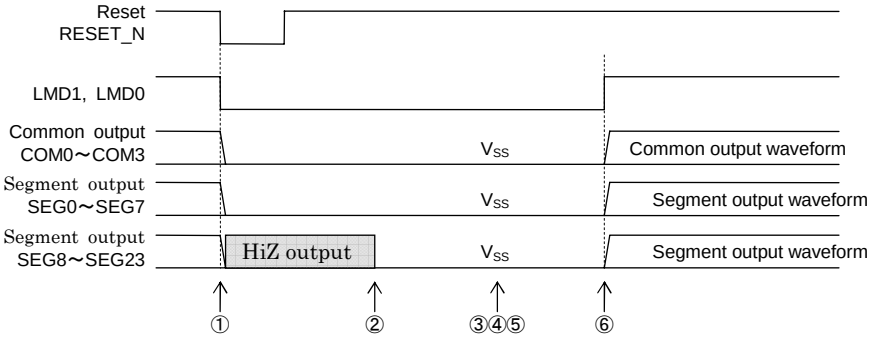


Figure 27-4 Operation of LCD Drivers and Bias Generation Circuit

① System reset causes the LCD drivers to stop operation and the segment port which is the combination with a general-purpose port will function as a general-purpose port, and will be in a HiZ output state.
② Segment port output is selected by the LCD port segment register (LSELS1 to 4). V_{SS} level is outputted to each segment port.
③ 1/2 bias or 1/3 bias is selected by the bias circuit control register (BIASCON).
④ Frame frequency and duty are set up with a display mode register(DSPMOD).
⑤ Display data (DSPR00 to DSPR27) is set as an display register..
⑥ LDC is set as display mode by LMD1, LMD0 bit of a display control register (DSPCON).(A display waveform is outputted to each segment port.)

27.3.2 Display Registers Segment Map

Figure 27-5 shows the display registers segment map.

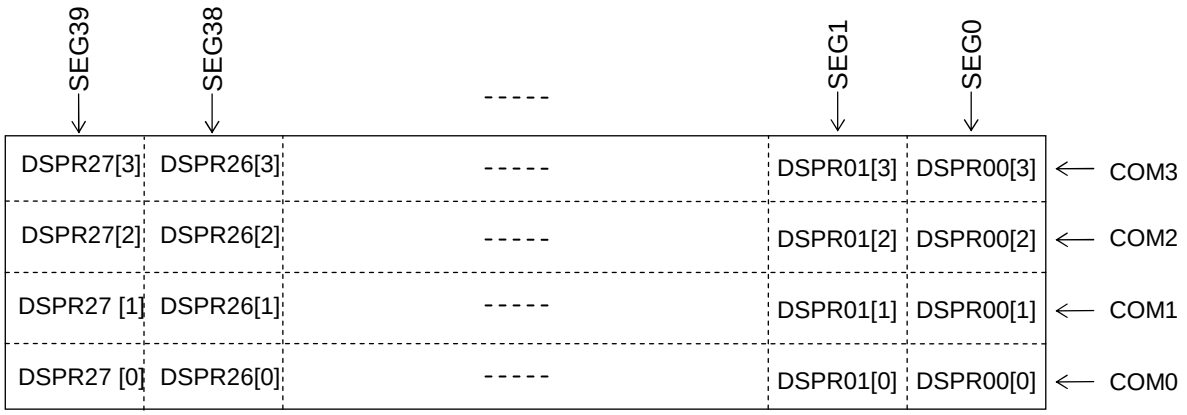


Figure 27-5 Configurations of Display register segment map

27.3.3 Common Output Waveform for 1/4 duty and 1/3 bias

Figure 27-6 shows the common output waveforms for 1/4 duty and 1/3 bias.

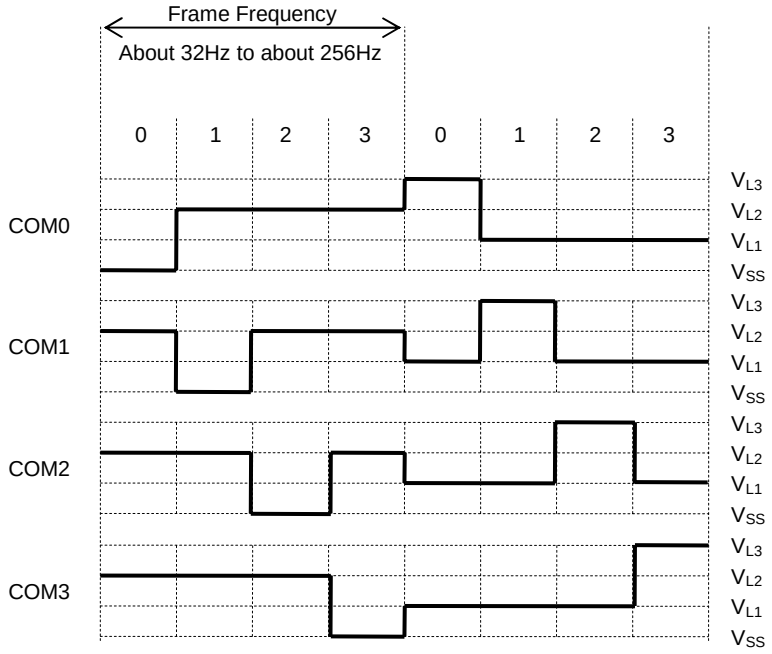


Figure 27-6 Common Output Waveforms for 1/4 Duty and 1/3 Bias

27.3.4 Segment Output Waveform for 1/4 duty and 1/3 bias

Figure 27-7 shows the segment output waveforms for 1/4 duty and 1/3 bias.

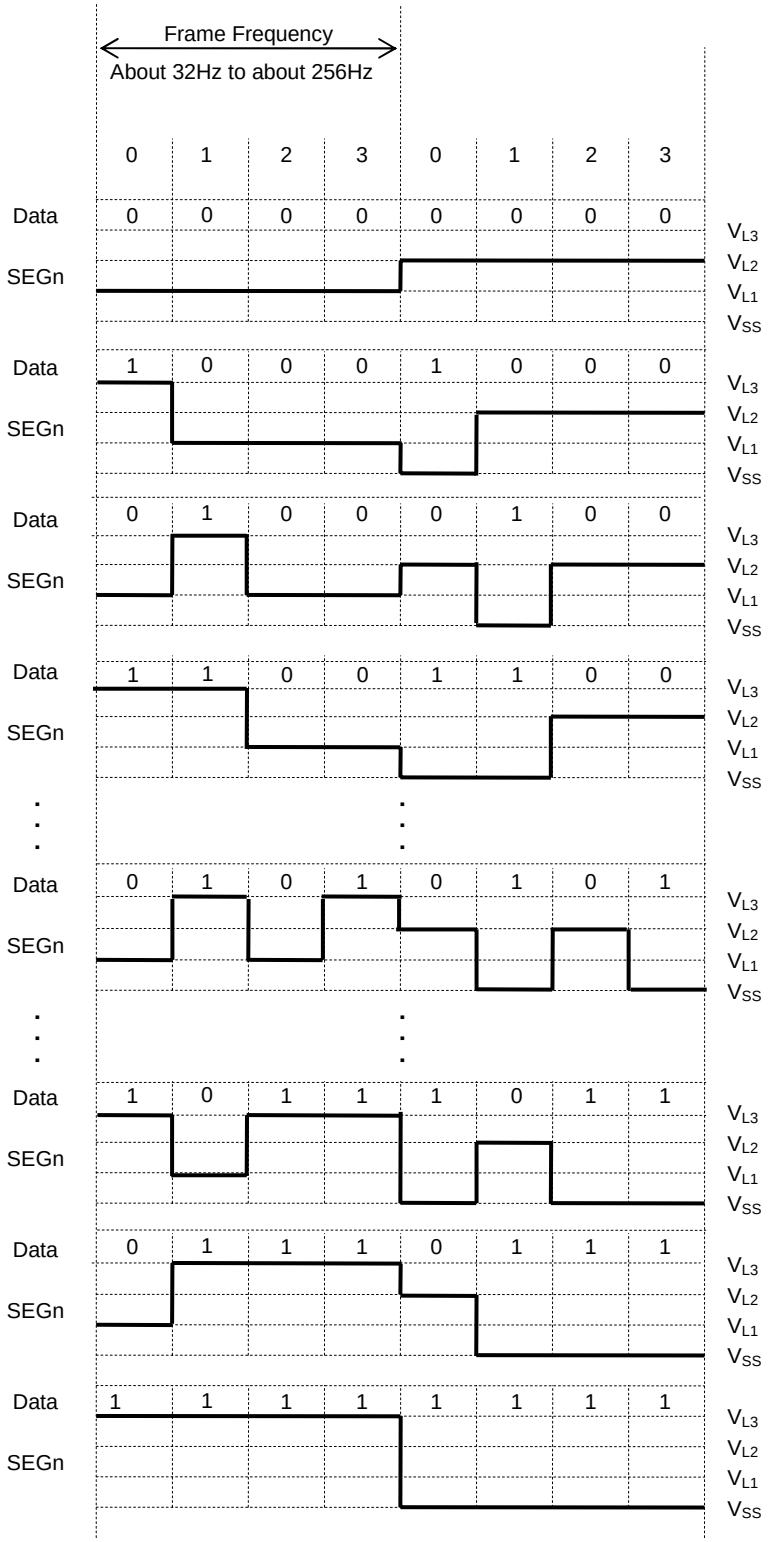


Figure 27-7 Segment Output Waveforms for 1/4 Duty and 1/3 Bias

27.3.5 Common Output Waveform for 1/4 duty and 1/2 bias

Figure 27-8 shows the segment output waveforms for 1/4 duty and 1/2 bias.

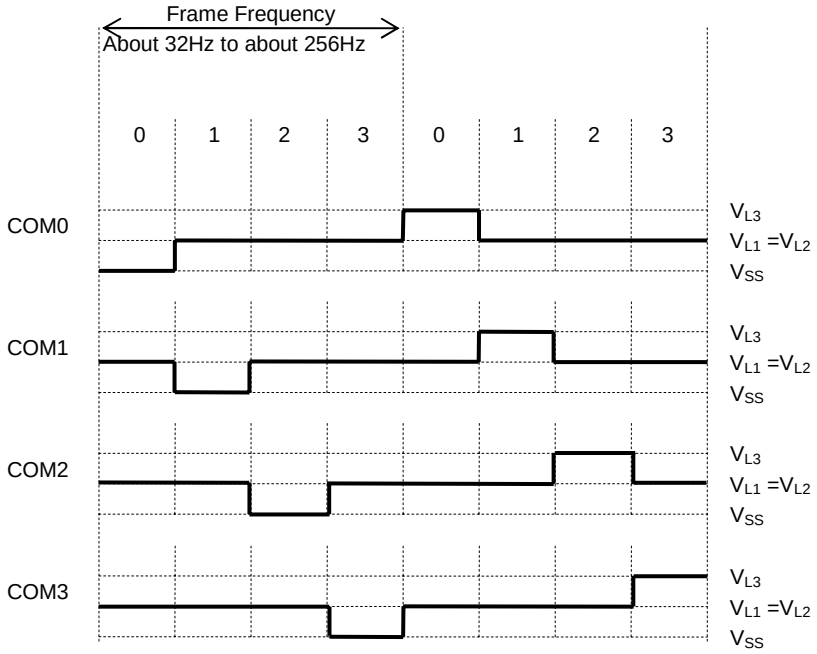


Figure 27-8 Common Output Waveforms for 1/4 Duty and 1/2 Bias

27.3.6 Segment Output Waveform for 1/4 duty and 1/2 bias

Figure 27-9 shows the segment output waveforms for 1/4 duty and 1/2 bias.

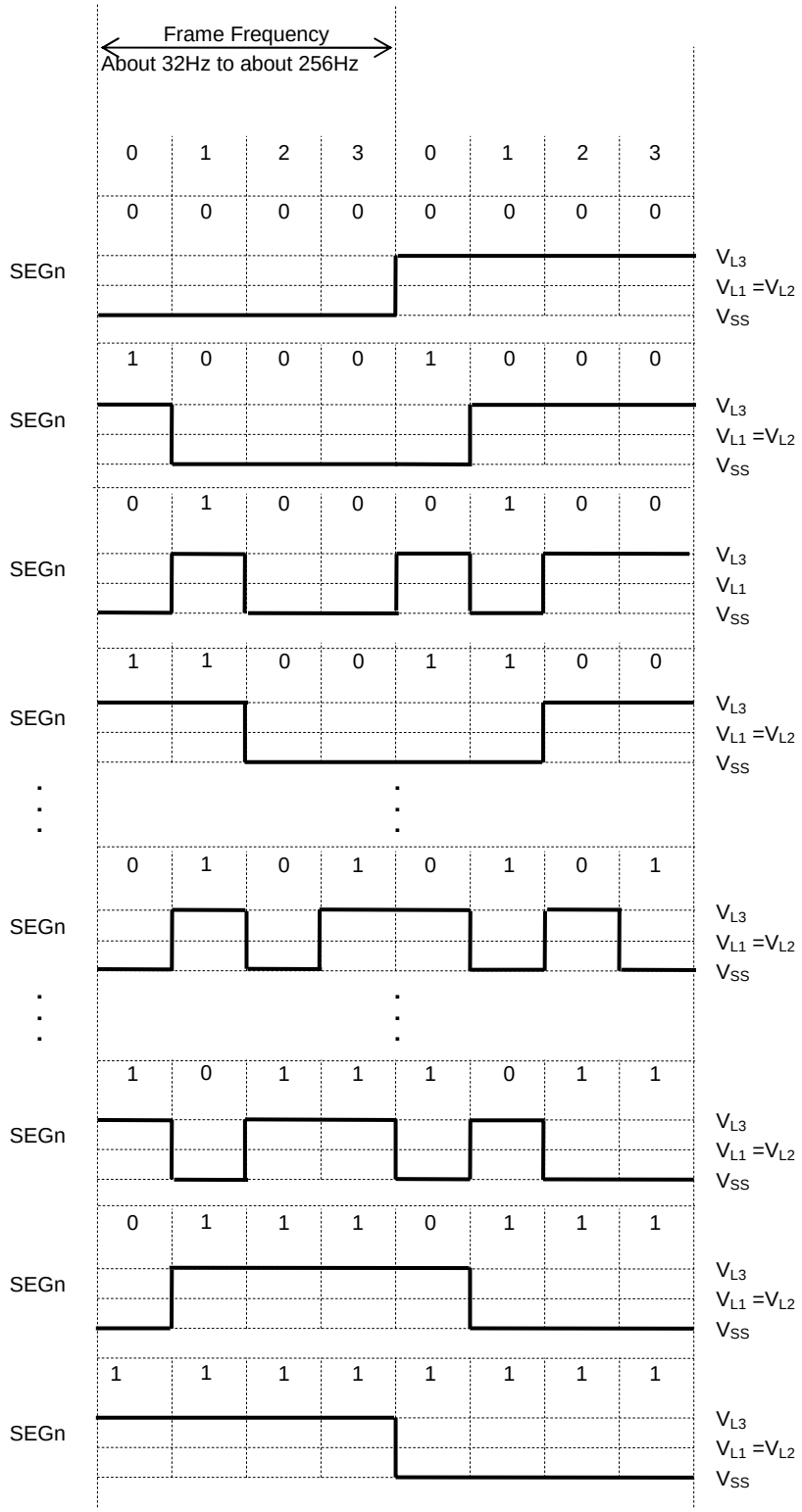


Figure 27-9 Segment Output Waveforms for 1/4 Duty and 1/2 Bias

Chapter 28

Successive Approximation Type A/D Converter

28. Successive Approximation Type A/D Converter (SA-ADC)

28.1 Overview

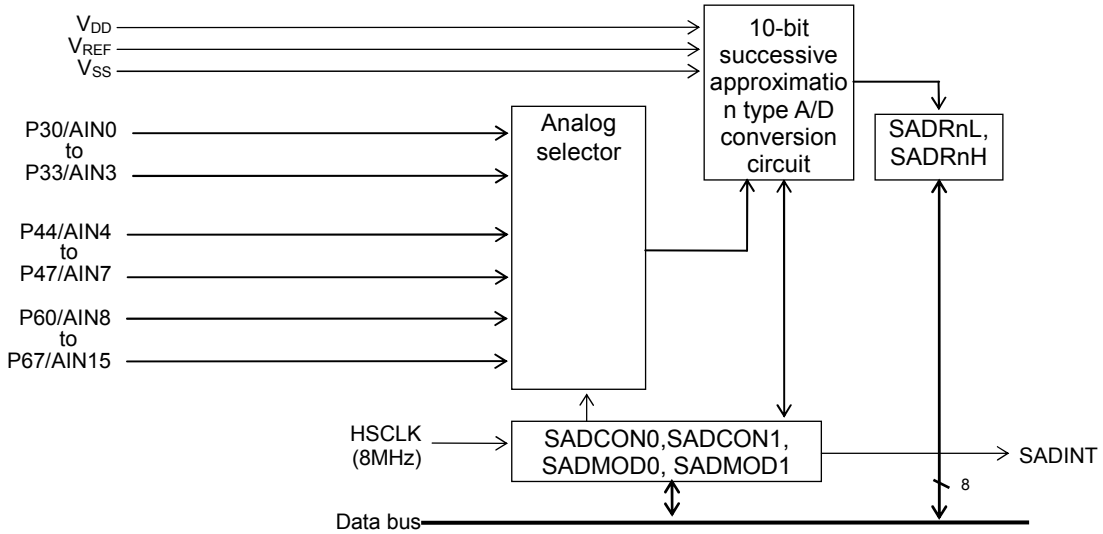
This LSI has a built-in 16-channel successive approximation type A/D converter (SA-ADC).
The SA-ADC operates only when the DSAD bit of the block control register 4 (BLKCON4) is "0". When the DSAD bit is "1", every function of the SA-ADC is in a reset state.
For the block control registers, see Chapter 4, "MCU Control Function".

28.1.1 Features

- Built-in sample/hold 10-bit successive approximation type A-D converter, which enables channel selection from 16 channels

28.1.2 Configuration

Figure 28-1 shows the configuration of SA-ADC.



SADRnL : SA-ADC result register nL
SADRnH : SA-ADC result register nH

SADCON0 : SA-ADC control register 0
SADCON1 : SA-ADC control register 1
SADMOD0 : SA-ADC mode register 0
SADMOD1 : SA-ADC mode register 1

Figure 28-1 Configuration of SA-ADC

28.1.3 List of Pins

Pin name	I/O	Description
V_{DD}	—	Positive power supply pin for the successive approximation type A/D converter
V_{SS}	—	Negative power supply pin for the successive approximation type A/D converter
V_{REF}	—	Reference power supply pin for the successive approximation type A/D converter
P30/AIN0	I	Input/output port, successive approximation type A/D converter input pin 0
P31/AIN1	I	Input/output port, successive approximation type A/D converter input pin 1
P32/AIN2	I	Input/output port, successive approximation type A/D converter input pin 2
P33/AIN3	I	Input/output port, successive approximation type A/D converter input pin 3
P44/AIN4	I	Input/output port, Timer 0 external clock input (T0P0CK) successive approximation type A/D converter input pin 4
P45/AIN5	I	Input/output port, Timer 0 external clock input (T0P1CK) successive approximation type A/D converter input pin 5
P46/AIN6	I	Input/output port, Timer 4,6 external clock input (T46CK) successive approximation type A/D converter input pin 6
P47/AIN7	I	Input/output port, Timer 5,7 external clock input (T571CK) successive approximation type A/D converter input pin 7
P60/AIN8	I	Input/output port, successive approximation type A/D converter input pin 8
P61/AIN9	I	Input/output port, successive approximation type A/D converter input pin 9
P62/AIN10	I	Input/output port, successive approximation type A/D converter input pin 10
P63/AIN11	I	Input/output port, successive approximation type A/D converter input pin 11
P64/AIN12	I	Input/output port, successive approximation type A/D converter input pin 12
P65/AIN13	I	Input/output port, successive approximation type A/D converter input pin 13
P66/AIN14	I	Input/output port, successive approximation type A/D converter input pin 14
P67/AIN15	I	Input/output port, successive approximation type A/D converter input pin 15

28.2 Description of Registers

28.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F2D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F2D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F2DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F2DBH	SA-ADC result register 5H	SADR5H		R	8	00H
0F2DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F2DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F2DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F2DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F2E0H	SA-ADC result register 8L	SADR8L	SADR8	R	8/16	00H
0F2E1H	SA-ADC result register 8H	SADR8H		R	8	00H
0F2E2H	SA-ADC result register 9L	SADR9L	SADR9	R	8/16	00H
0F2E3H	SA-ADC result register 9H	SADR9H		R	8	00H
0F2E4H	SA-ADC result register AL	SADRAL	SADRA	R	8/16	00H
0F2E5H	SA-ADC result register AH	SADRAH		R	8	00H
0F2E6H	SA-ADC result register BL	SADRBL	SADRB	R	8/16	00H
0F2E7H	SA-ADC result register BH	SADRBH		R	8	00H
0F2E8H	SA-ADC result register CL	SADRCL	SADRC	R	8/16	00H
0F2E9H	SA-ADC result register CH	SADRCH		R	8	00H
0F2EAH	SA-ADC result register DL	SADRDL	SADRD	R	8/16	00H
0F2EBH	SA-ADC result register DH	SADRDH		R	8	00H
0F2ECH	SA-ADC result register EL	SADREL	SADRE	R	8/16	00H
0F2EDH	SA-ADC result register EH	SADREH		R	8	00H
0F2EEH	SA-ADC result register FL	SADRFL	SADRF	R	8/16	00H
0F2EFH	SA-ADC result register FH	SADRFH		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	02H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	SADMOD	R/W	8	00H
0F2F3H	SA-ADC mode register 1	SADMOD1		R/W	8	00H

28.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F2D0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR03	SAR02	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0L is updated after A/D conversion.

[Description of Bits]

- **SAR03 to SAR02** (bits 7 to 6)
  The SAR03–SAR02 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 0.

28.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F2D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR0B	SAR0A	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0H is updated after A/D conversion.

[Description of Bits]

- **SAR0B to SAR04** (bits 7 to 0)
  The SAR0B3–SAR04 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 0.

28.2.4 SA-ADC Result Register 1L (SADR1L)

Address: 0F2D2H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1L	SAR13	SAR12	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1L is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1L is updated after A/D conversion.

[Description of Bits]

- **SAR13 to SAR12** (bits 7 to 6)
  The SAR13–SAR12 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 1.

28.2.5 SA-ADC Result Register 1H (SADR1H)

Address: 0F2D3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1H	SAR1B	SAR1A	SAR19	SAR18	SAR17	SAR16	SAR15	SAR14
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1H is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1H is updated after A/D conversion.

[Description of Bits]

- **SAR1B to SAR14** (bits 7 to 0)
  The SAR1B–SAR14 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 1.

28.2.6 SA-ADC Result Register 2L (SADR2L)

Address: 0F2D4H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2L	SAR23	SAR22	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2L is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2L is updated after A/D conversion.

[Description of Bits]

- **SAR23 to SAR22** (bits 7 to 6)
  The SAR23–SAR22 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 2.

28.2.7 SA-ADC Result Register 2H (SADR2H)

Address: 0F2D5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2H	SAR2B	SAR2A	SAR29	SAR28	SAR27	SAR26	SAR25	SAR24
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2H is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2H is updated after A/D conversion.

[Description of Bits]

- **SAR2B to SAR24** (bits 7 to 0)
  The SAR2B–SAR24 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 2.

28.2.8 SA-ADC Result Register 3L (SADR3L)

Address: 0F2D6H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3L	SAR33	SAR32	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3L is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3L is updated after A/D conversion.

[Description of Bits]

- **SAR33 to SAR32** (bits 7 to 6)
  The SAR33–SAR32 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 3.

28.2.9 SA-ADC Result Register 3H (SADR3H)

Address: 0F2D7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3H	SAR3B	SAR3A	SAR39	SAR38	SAR37	SAR36	SAR35	SAR34
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3H is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3H is updated after A/D conversion.

[Description of Bits]

- **SAR3B to SAR34** (bits 7 to 0)
  The SAR3B–SAR34 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 3.

28.2.10 SA-ADC Result Register 4L (SADR4L)

Address: 0F2D8H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4L	SAR43	SAR42	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR4L is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4L is updated after A/D conversion.

[Description of Bits]

- **SAR43 to SAR42** (bits 7 to 6)
  The SAR43–SAR42 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 4.

28.2.11 SA-ADC Result Register 4H (SADR4H)

Address: 0F2D9H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4H	SAR4B	SAR4A	SAR49	SAR48	SAR47	SAR46	SAR45	SAR44
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR4H is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4H is updated after A/D conversion.

[Description of Bits]

- **SAR4B to SAR44** (bits 7 to 0)
  The SAR4B–SAR44 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 4.

28.2.12 SA-ADC Result Register 4L (SADR5L)

Address: 0F2DAH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5L	SAR53	SAR52	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR5L is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5L is updated after A/D conversion.

[Description of Bits]

- **SAR53 to SAR52** (bits 7 to 6)
  The SAR53–SAR52 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 5.

28.2.13 SA-ADC Result Register 4H (SADR5H)

Address: 0F2DBH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5H	SAR5B	SAR5A	SAR59	SAR58	SAR57	SAR56	SAR55	SAR54
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR5H is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5H is updated after A/D conversion.

[Description of Bits]

- **SAR5B to SAR54** (bits 7 to 0)
  The SAR5B–SAR54 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 5.

28.2.14 SA-ADC Result Register 4L (SADR6L)

Address: 0F2DCH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6L	SAR63	SAR62	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR6L is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6L is updated after A/D conversion.

[Description of Bits]

- **SAR63 to SAR62** (bits 7 to 6)
  The SAR63–SAR62 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 6.

28.2.15 SA-ADC Result Register 4H (SADR6H)

Address: 0F2DDH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6H	SAR6B	SAR6A	SAR69	SAR68	SAR67	SAR66	SAR65	SAR64
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR6H is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6H is updated after A/D conversion.

[Description of Bits]

- **SAR6B to SAR64** (bits 7 to 0)
  The SAR6B–SAR64 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 6.

28.2.16 SA-ADC Result Register 4L (SADR7L)

Address: 0F2DEH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7L	SAR73	SAR72	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR7L is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7L is updated after A/D conversion.

[Description of Bits]

- **SAR73 to SAR72** (bits 7 to 6)
  The SAR73–SAR72 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 7.

28.2.17 SA-ADC Result Register 4H (SADR7H)

Address: 0F2DFH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7H	SAR7B	SAR7A	SAR79	SAR78	SAR77	SAR76	SAR75	SAR74
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR7H is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7H is updated after A/D conversion.

[Description of Bits]

- **SAR7B to SAR74** (bits 7 to 0)
  The SAR7B–SAR74 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 7.

28.2.18 SA-ADC Result Register 8L (SADR8L)

Address: 0F2E0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR8L	SAR83	SAR82	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR8L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR8L is updated after A/D conversion.

[Description of Bits]

- **SAR83 to SAR82** (bits 7 to 6)
  The SAR83–SAR82 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 8.

28.2.19 SA-ADC Result Register 8H (SADR8H)

Address: 0F2E1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR8H	SAR8B	SAR8A	SAR89	SAR88	SAR87	SAR86	SAR85	SAR84
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR8H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR8H is updated after A/D conversion.

[Description of Bits]

- **SAR8B to SAR84** (bits 7 to 0)
  The SAR8B3–SAR84 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 8.

28.2.20 SA-ADC Result Register 9L (SADR9L)

Address: 0F2E2H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR9L	SAR93	SAR92	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR9L is a special function register (SFR) used to store SA-ADC conversion results on channel 9.
SADR9L is updated after A/D conversion.

[Description of Bits]

- **SAR93 to SAR92** (bits 7 to 6)
  The SAR93–SAR92 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 9.

28.2.21 SA-ADC Result Register 1H (SADR1H)

Address: 0F2E3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR9H	SAR9B	SAR9A	SAR99	SAR98	SAR97	SAR96	SAR95	SAR94
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR9H is a special function register (SFR) used to store SA-ADC conversion results on channel 9.
SADR9H is updated after A/D conversion.

[Description of Bits]

- **SAR9B to SAR94** (bits 7 to 0)
  The SAR9B–SAR94 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 9.

28.2.22 SA-ADC Result Register AL (SADRAL)

Address: 0F2E4H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRAL	SARA3	SARA2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRAL is a special function register (SFR) used to store SA-ADC conversion results on channel A.
SADRAL is updated after A/D conversion.

[Description of Bits]

- **SARA3 to SARA2** (bits 7 to 6)
  The SARA3–SARA2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel A.

28.2.23 SA-ADC Result Register 2H (SADR2H)

Address: 0F2E5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRAH	SARAB	SARAA	SARA9	SARA8	SARA7	SARA6	SARA5	SARA4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRAH is a special function register (SFR) used to store SA-ADC conversion results on channel A.
SADRAH is updated after A/D conversion.

[Description of Bits]

- **SARAB to SARA4** (bits 7 to 0)
  The SARAB–SARA4 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel A.

28.2.24 SA-ADC Result Register BL (SADRBL)

Address: 0F2E6H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRBL	SARB3	SARB2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRBL is a special function register (SFR) used to store SA-ADC conversion results on channel B.
SADRBL is updated after A/D conversion.

[Description of Bits]

- **SARB3 to SARB2** (bits 7 to 6)
  The SARB3–SARB2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel B.

28.2.25 SA-ADC Result Register BH (SADRBH)

Address: 0F2E7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRBH	SARBB	SARBA	SARB9	SARB8	SARB7	SARB6	SARB5	SARB4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRBH is a special function register (SFR) used to store SA-ADC conversion results on channel B.
SADRBH is updated after A/D conversion.

[Description of Bits]

- **SARBB to SARB4** (bits 7 to 0)
  The SARBB–SARB4 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel B.

28.2.26 SA-ADC Result Register CL (SADRCL)

Address: 0F2E8H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRCL	SARC3	SARC2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRCL is a special function register (SFR) used to store SA-ADC conversion results on channel C.
SADRCL is updated after A/D conversion.

[Description of Bits]

- **SARC3 to SARC2** (bits 7 to 6)
  The SARC3–SARC2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel C.

28.2.27 SA-ADC Result Register CH (SADRCH)

Address: 0F2E9H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRCH	SARCB	SARCA	SARC9	SARC8	SARC7	SARC6	SARC5	SARC4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRCH is a special function register (SFR) used to store SA-ADC conversion results on channel C.
SADRCH is updated after A/D conversion.

[Description of Bits]

- **SARCB to SARC4** (bits 7 to 0)
  The SARCB–SARC4 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel C.

28.2.28 SA-ADC Result Register 4L (SADRDL)

Address: 0F2EAH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRDL	SARD3	SARD2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRDL is a special function register (SFR) used to store SA-ADC conversion results on channel D.
SADRDL is updated after A/D conversion.

[Description of Bits]

- **SARD3 to SARD2** (bits 7 to 6)
  The SARD3–SARD2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel D.

28.2.29 SA-ADC Result Register 4H (SADRDH)

Address: 0F2EBH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRDH	SARDB	SARDA	SARD9	SARD8	SARD7	SARD6	SARD5	SARD4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRDH is a special function register (SFR) used to store SA-ADC conversion results on channel D.
SADRDH is updated after A/D conversion.

[Description of Bits]

- **SARDB to SARD4** (bits 7 to 0)
  The SARDB–SARD4 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel D.

28.2.30 SA-ADC Result Register EL (SADREL)

Address: 0F2ECH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADREL	SARE3	SARE2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADREL is a special function register (SFR) used to store SA-ADC conversion results on channel E.
SADREL is updated after A/D conversion.

[Description of Bits]

- **SARE3 to SARE2** (bits 7 to 6)
  The SARE3–SARE2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel E.

28.2.31 SA-ADC Result Register EH (SADREH)

Address: 0F2EDH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADREH	SAREB	SAREA	SARE9	SARE8	SARE7	SARE6	SARE5	SARE4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADREH is a special function register (SFR) used to store SA-ADC conversion results on channel E.
SADREH is updated after A/D conversion.

[Description of Bits]

- **SAREB to SARE4** (bits 7 to 0)
  The SAREB–SARE4 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel E.

28.2.32 SA-ADC Result Register FL (SADRFL)

Address: 0F2EEH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRFL	SARF3	SARF2	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRFL is a special function register (SFR) used to store SA-ADC conversion results on channel F.
SADRF7L is updated after A/D conversion.

[Description of Bits]

- **SARF3 to SARF0** (bits F to 6)
  The SARF3–SARF2 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel F.

28.2.33 SA-ADC Result Register 4H (SADRFH)

Address: 0F2EFH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRFH	SARFB	SARFA	SARF9	SARF8	SARF7	SARF6	SARF5	SARF4
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRFH is a special function register (SFR) used to store SA-ADC conversion results on channel F.
SADRFH is updated after A/D conversion.

[Description of Bits]

- **SARFB to SARF4** (bits 7 to 0)
  The SARFB–SAR74 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel F.

28.2.34 SA-ADC Control Register 0 (SADCON0)

Address: 0F2F0H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON0	—	—	—	—	—	—	—	SALP
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SALP** (bit 0)
  This bit is used to select whether A/D conversion is performed once only for each channel or continuously . When this bit is set to "0", A/D conversion is performed once only for each channel and when it is set to "1", A/D conversion is performed continuously.

SALP	Description
0	Single A/D conversion only (Initial value)
1	Continuous A/D conversion

28.2.35 SA-ADC Control Register 1 (SADCON1)

Address: 0F2F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	—	—	—	—	—	—	—	SARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SARUN** (bit 0)
  The SARUN bit is used to start or stop SA-ADC conversion. Setting this bit to "1" starts A/D conversion and setting it to "0" stops A/D conversion.
  When SALP of SADCON0 is "0" and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to "0".

SARUN	Description
0	Stops conversion. (Initial value)
1	Starts conversion.

Notes:
Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).
The SA-ADC is available only when V_{DD} = 4.5 V to 5.5 V and HSCLK is in the ranges of 3MHz to 8.4MHz.
Do not start A/D conversion with all of bit-7 (SACHF) to bit-0 (SACH0) of the SA-ADC mode register 0 and register1 set to "0". If A/D conversion is started in this state, the A/D converter circuit is turned on but no A/D conversion is carried out. Therefore, the SA-ADC result register is not updated. In addition, the A/D conversion termination interrupt is not generated and A/D conversion is not terminated automatically, so that SARUN remains "1".

28.2.36 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F2F2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	SACH7	SACH6	SACH5	SACH4	SACH3	SACH2	SACH1	SACH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]

- **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

- **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

- **SACH2** (bit 2)

SACH2	Description
0	Stops conversion on channel 2. (Initial value)
1	Performs conversion on channel 2.

- **SACH3** (bit 3)

SACH3	Description
0	Stops conversion on channel 3. (Initial value)
1	Performs conversion on channel 3.

- **SACH4** (bit 4)

SACH4	Description
0	Stops conversion on channel 4. (Initial value)
1	Performs conversion on channel 4.

- **SACH5** (bit 5)

SACH5	Description
0	Stops conversion on channel 5. (Initial value)
1	Performs conversion on channel 5.

- **SACH6** (bit 6)

SACH6	Description
0	Stops conversion on channel 6. (Initial value)
1	Performs conversion on channel 6.

- **SACH7** (bit 7)

SACH7	Description
0	Stops conversion on channel 7. (Initial value)
1	Performs conversion on channel 7.

The SACH7–SACH0 bits are used to select channel(s) on which A/D conversion is performed.
If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

Do not start A/D conversion in the state that all the bits of the bit 7 (SACH7) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) and the bit 7 (SACHF) to the bit 0 (SACH8) of the SA-ADC mode register 1 (SADMOD1) are "0". If A/D conversion is started in this state, the A/D converter circuit is turned on but no A/D conversion is carried out. Therefore, the SA-ADC result register is not updated. In addition, the A/D conversion termination interrupt is not generated and A/D conversion is not terminated automatically, so that bit-0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

28.2.37 SA-ADC Mode Register 1 (SADMOD1)

Address: 0F2F3H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	SACHF	SACHE	SACHD	SACHC	SACHB	SACHA	SACH9	SACH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]

- **SACH8** (bit 0)

SACH8	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

- **SACH9** (bit 1)

SACH9	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

- **SACHA** (bit 2)

SACHA	Description
0	Stops conversion on channel 2. (Initial value)
1	Performs conversion on channel 2.

- **SACHB** (bit 3)

SACHB	Description
0	Stops conversion on channel 3. (Initial value)
1	Performs conversion on channel 3.

- **SACHC** (bit 4)

SACHC	Description
0	Stops conversion on channel 4. (Initial value)
1	Performs conversion on channel 4.

- **SACHD** (bit 5)

SACHD	Description
0	Stops conversion on channel 5. (Initial value)
1	Performs conversion on channel 5.

- **SACHE** (bit 6)

SACHE	Description
0	Stops conversion on channel 6. (Initial value)
1	Performs conversion on channel 6.

- **SACHF** (bit 7)

SACHF	Description
0	Stops conversion on channel 7. (Initial value)
1	Performs conversion on channel 7.

The SACH8–SACHF bits are used to select channel(s) on which A/D conversion is performed.
If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

Do not start A/D conversion in the state that all the bits of the bit 7 (SACH7) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) and the bit 7 (SACHF) to the bit 0 (SACH8) of the SA-ADC mode register 1 (SADMOD1) are "0". If A/D conversion is started in this state, the A/D converter circuit is turned on but no A/D conversion is carried out. Therefore, the SA-ADC result register is not updated. In addition, the A/D conversion termination interrupt is not generated and A/D conversion is not terminated automatically, so that bit-0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

28.3 Description of Operation

28.3.1 Setup of the A/D conversion channel

By setup of the SA-ADC mode register 0 (SADMOD0), as shown in the following table, A/D conversion operation is performed, and the A/D conversion result is stored in the SA-ADC result register.

SA-ADC mode register 0/1					SA-ADC result register					Remarks
SACHF	・・・	SACH2	SACH1	SACH0	SADR7	・・・	SADR2	SADR1	SADR0	
0	0	0	0	0						Prohibition of use
0	0	0	0	1					AIN0	
0	0	0	1	0				AIN1		
0	0	0	1	1				AIN1	AIN0	
0	0	1	0	0			AIN2			
0	0	1	0	1			AIN2		AIN0	
0	0	1	1	0			AIN2	AIN1		
0	0	1	1	1			AIN2	AIN1	AIN0	
1	0	0	0	0	AIN15					
1	0	0	0	1	AIN15				AIN0	
1	0	0	1	0	AIN15			AIN1		
1	0	0	1	1	AIN15			AIN1	AIN0	
1	0	1	0	0	AIN15		AIN2			
1	0	1	0	1	AIN15		AIN2		AIN0	
1	0	1	1	0	AIN15		AIN2	AIN1		
1	0	1	1	1	AIN15		AIN2	AIN1	AIN0	

The value of the result register of a slash part does not change.
Do not start A/D conversion in the state that all the bits of the bit 7 (SACH7) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) and the bit 7 (SACHF) to the bit 0 (SACH8) of the SA-ADC mode register 1 (SADMOD1) are "0". If A/D conversion is started in this state, the A/D converter circuit is turned on but no A/D conversion is carried out. Therefore, the SA-ADC result register is not updated. In addition, the A/D conversion termination interrupt is not generated and A/D conversion is not terminated automatically, so that bit-0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

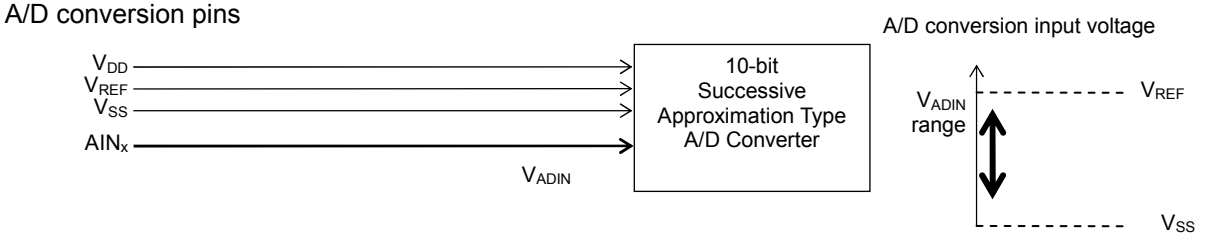


Figure 28-2 The A/D conversion pins and the conversion range

28.3.2 Operation of Successive Approximation Type A/D Converter

Use the following procedure to operate the SA-ADC:

1. Before starting the SA-ADC, start oscillation of the high-speed clock (HSCLK) and wait until the oscillation stabilizes.
2. Set the SA-ADC mode register 0 (SADMOD0).
3. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the lower channel number that is selected in the SA-ADC mode register (SADMOD0).
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRnL, SADRnH), and when A/D conversion of the largest channel number that is selected is terminated, an SA-ADC conversion termination interrupt (ADSINT) is generated.
5. Finally, by using bit 0 (SALP) of the SADCON0 register, it is possible to specify whether to terminate A/D conversion (SARUN bit is "0") or restart A/D conversion automatically at termination of A/D conversion of the last channel.

Note:
When conversion accuracy is important, perform ADC measurement in HALT mode.

Even if a channel is switched during A/D conversion, the channel that was selected at the start of A/D conversion is used until an A/D conversion termination interrupt occurs.
Figure 28-2 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

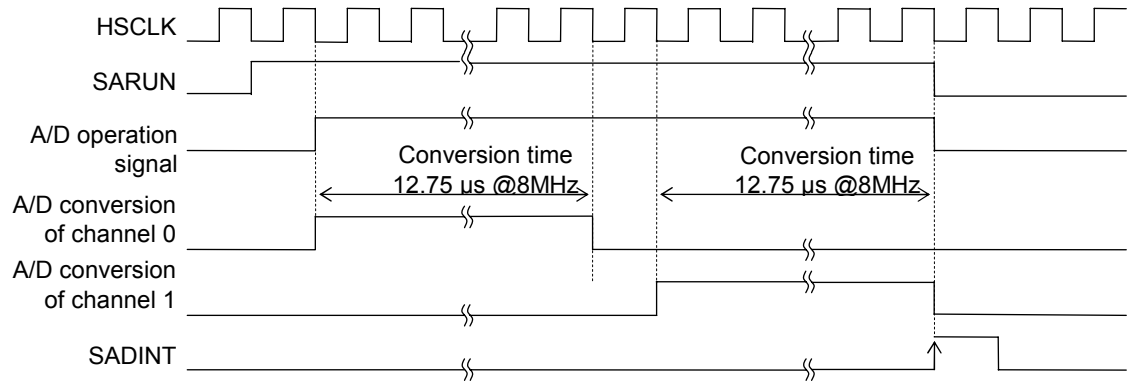


Figure 28-3 SA-ADC Operation Timing

Chapter 29

Battery Level Detector

29. Battery Level Detector

29.1 Overview

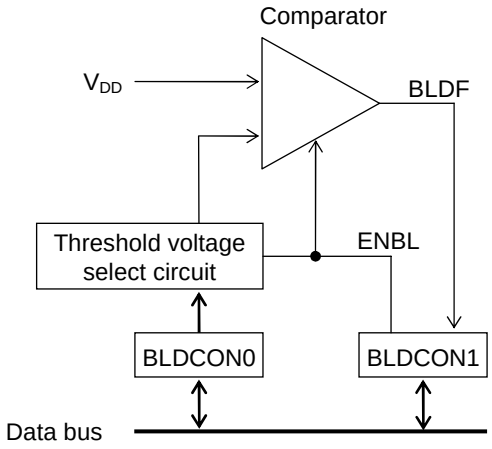
This LSI includes a Battery Level Detector (BLD).
4 levels of threshold voltages can be selected by setting Battery Level Detector control register 0 (BLDCON0).

29.1.1 Features

- Threshold voltages: One out of the 16 levels can be selected
- Accuracy: ±2% (Typ.)
- Self supply current: 10μA(Typ.)

29.1.2 Configuration

BLD consists of the comparator and threshold voltage select circuits.
Figure 29-1 shows the configuration of the Battery Level Detector.



BLDCON0 : Battery Level Detector control register 0
BLDCON1 : Battery Level Detector control register 1

Figure 29-1 Configuration of Battery Level Detector

29.2 Description of Registers

29.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0D0H	Battery Level Detector control register 0	BLDCON0	BLDCON	R/W	8/16	00H
0F0D1H	Battery Level Detector control register 1	BLDCON1		R/W	8	00H

29.2.2 Battery Level Detector Control Register 0 (BLDCON0)

Address: 0F0D0H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLDCON0	—	—	—	—	LD3	LD2	LD1	LD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLDCON0 is a special function register (SFR) to control the Battery Level Detector

[Description of Bits]

- **LD3, LD2, LD1, LD0** (bits 3-0)
  The LD3, LD2, LD1, and LD0 bits are used to select a threshold voltage (VCMP) of the Battery Level Detector. 16 levels of threshold voltages can be selected.

LD3	LD2	LD1	LD0	Description
0	0	0	0	2.35 V ±2% (initial value)
0	0	0	1	Prohibited
0	0	1	0	Prohibited
0	0	1	1	2.80 V ±2%
0	1	0	0	Prohibited
0	1	0	1	Prohibited
0	1	1	0	Prohibited
0	1	1	1	Prohibited
1	0	0	0	Prohibited
1	0	0	1	3.70 V ±2%
1	0	1	0	Prohibited
1	0	1	1	Prohibited
1	1	0	0	Prohibited
1	1	0	1	Prohibited
1	1	1	0	Prohibited
1	1	1	1	4.60 V ±2%

29.2.3 Battery Level Detector Control Register 1 (BLDCON1)

Address: 0F0D1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLDCON1	—	—	—	—	—	—	BLDF	ENBL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLDCON1 is a special function register (SFR) to control the Battery Level Detector.

[Description of Bits]

- **ENBL** (bit 0)

The ENBL bit is used to control activation (ON) or deactivation (OFF) of the Battery Level Detector.
The Battery Level Detector is activated (ON) and deactivated (OFF) by setting the ENBL bit to "1" and "0", respectively.

ENBL	Description
0	Deactivates the Battery Level Detector (OFF) (initial value)
1	Activates the Battery Level Detector (ON).

- **BLDF** (bit 1)

The BLDF bit is the judgment result flag of the Battery Level Detector.
The BLDF bit is set to "1" or "0" when the power supply voltage (VDD) is lower than or higher than the threshold voltage selected by LD3 to LD0 bits of BLDCON0 register, respectively.

BLDF	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

29.3 Description of Operation

29.3.1 Threshold Voltage

The threshold voltage (VCMP) is selected by setting the bits of BLDCON0.
Table 29-1 shows the threshold voltages and the accuracy.

Table 29-1 Threshold Voltages and Accuracy

BLDCON0				Threshold voltage	Accuracy
LD3	LD2	LD1	LD0	V_{CMP}	Ta = 25°C
0	0	0	0	2.35 V	±2.0%
0	0	1	1	2.80 V	
1	0	0	1	3.70 V	
1	1	1	1	4.60 V	

29.3.2 Operation of Battery Level Detector

Activation (ON) and deactivation (OFF) of the Battery Level Detector are controlled by setting the ENBL bit of the Battery Level Detector control register (BLDCON1), and the result of the comparison of the power supply voltage (VDD) to the threshold voltage is output to the BLDF bit of BLDCON1.
When ENBL, the enable control bit of the Battery Level Detector, is set to "1", the detector is activated (ON). When ENBL is set to "0", the detector is deactivated (OFF) and has no supply current.
BLDF indicates the result of comparison. When BLDF bit is set to "1", it indicates the power supply voltage is lower than the threshold voltage. When BLDF bit is set to "0", it indicates the power supply voltage (VDD) is higher than the threshold voltage. The Battery Level Detector requires a settling time. Read BLDF bit 1ms or more after ENBL bit is set to "1".
Figure 29-2 shows an example of the operation timing diagram.

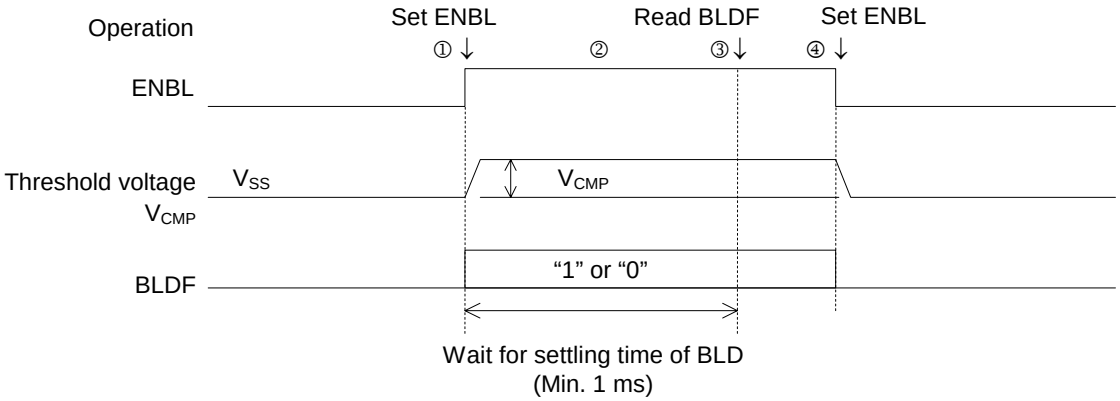


Figure 29-2 Example of Operation Timing Diagram

The operations in Figure 29-2 are described below.

① The Battery Level Detector is activated (ON) by setting the ENBL bit to "1".
② Wait the settling time (min. 1 ms) of the Battery Level Detector.
③ Read BLDF bit.
④ Set ENBL bit to "0".

Note:
Select the threshold voltage (VCMP) when the ENBL bit is "0".

Chapter 30

Power Supply Circuit

30. Power Supply Circuit

30.1 Overview

This LSI incorporates a regulated power supply circuit for the internal logic (VRL).
The VRL outputs the operating voltage, V_{DDL}, for the internal logic, program memory, RAM, etc.

30.1.1 Features

- VRL outputs the operating voltage, V_{DDL}, of the internal logic, program memory, RAM, etc.

30.1.2 Configuration

Figure 30-1 shows the configuration of the power supply circuit.

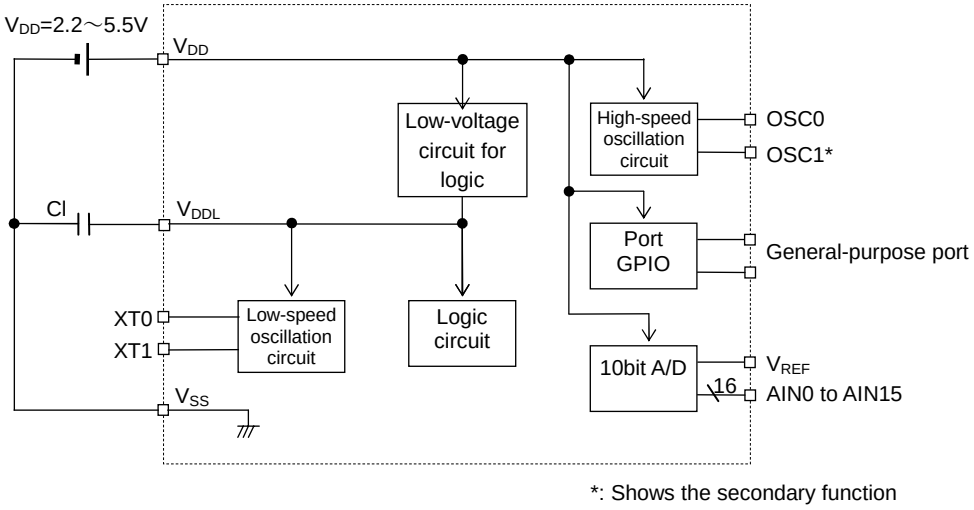


Figure 30-1 Configuration of Power Supply Circuit

30.1.3 List of Pins

Pin name	I/O	Description
V_{DDL}	—	Positive power supply pin for the internal logic circuits

30.2 Description of Operation

V_{DDL} voltage is set to about 2.1v in all the operational modes after a power supply injection.

Figure 30-2 shows the operation waveforms of the power supply circuit.

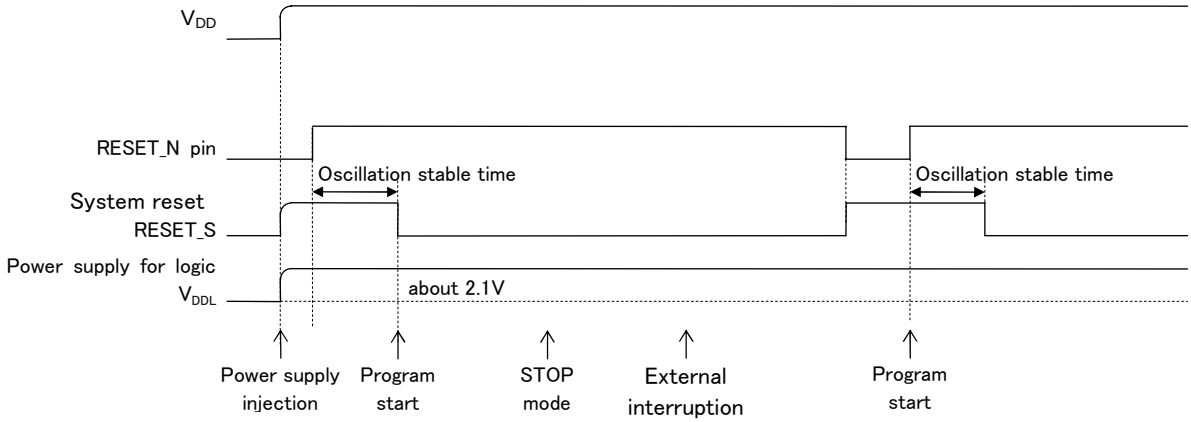


Figure 30-2 Waveforms of Power Supply Circuit Operation

Chapter 31

On-Chip Debug Function

31. On-Chip Debug Function

31.1 Overview

This LSI has an on-chip debug function that enables flash memory reprogramming.
To use the on-chip debug function, connect the LSI to the on-chip debug emulator (uEASE).

31.2 How to Connect the On-Chip Debug Emulator

Figure 31-1 shows the connections to the on-chip debug emulator (uEASE).
For the on-chip debug emulator, refer to the "uEASE User's Manual."

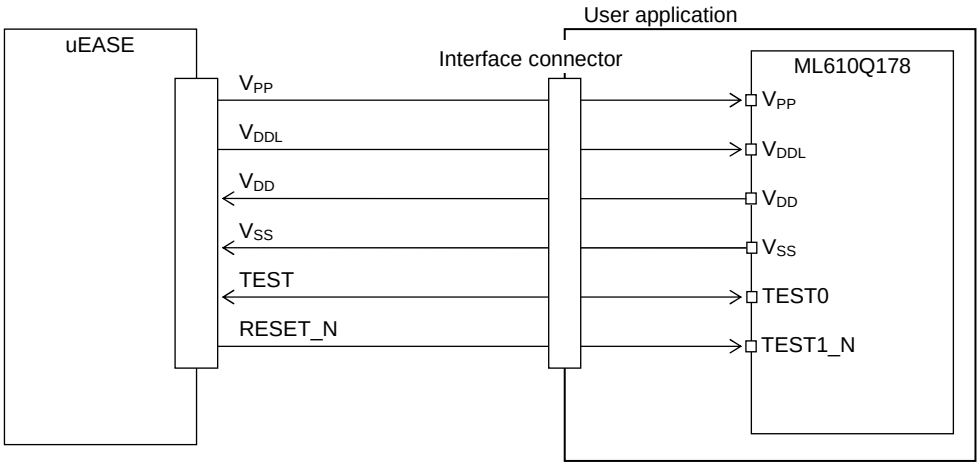


Figure 31-1 Connections to the On-Chip Debug Emulator (uEASE)

Note:
- Do not use LSI used for debugging as a mass-production article.
- When using the on-chip debug function or flash memory reprogramming function after mounting the LSI on the board, design the board so that the six pins of V_{DD}, V_{SS}, ,TEST1_N, TEST0, VDDL and VPP which are required for connection to the on-chip debug emulator, are capable of connection. Also, apply 2.7 to 5.5 V to $V_{DD.}$
- For details, refer to the "uEASE User's Manual" and the "uEASE connection Manual".

Note:
When debugging is performed by the on-chip debugging emulator (uEASE), as a target chip, select "ML610Q178A" for ML610Q178.

Chapter 32

Code-Option

32. Code-Option

32.1 Overview

This LSI includes Code-option function.
Used or unused of an 32.768kHz crystal oscillation can be selected as a low-speed clock with the code-option data written in the test data domain of the program memory.

32.1.1 Features

- Used or unused of an 32.768kHz crystal oscillation can be selected as a low-speed clock

32.2 Description of Registers

32.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F3D8H	Code-option register	CODEOP0	—	R	8	—*

* The contents of the Code-Option register 0 are dependent on the Code-Option data written in the test data domain of the program memory.

32.2.2 Code-Option Register (CODEOP0)

Address: 0F3D8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CODEOP0	COLOSC	—*	—*	—*	—*	—*	—*	—*
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

CODEOP0 is a special function register by which the set-up code-option data can be read. CODEOP0 can be read and writing is impossible.
About the method of setup of Code-option data, refer to Chapter 32.3, "The method of a setup of Code-Option data "

[Description of Bits]

- **COLOSC** (bits 7)
  COLOSC is a bit which shows use / un-using it of a low-speed crystal oscillation as a low-speed clock.

COLOSC	Description
0	32.768kHz crystal oscillation is not used as a low-speed clock.
1	32.768kHz crystal oscillation is used as a low-speed clock.

32.3 The method of a setup of Code-Option data

32.3.1 The format of Code-Option data

Set Code-Option data as 0:FDE0H address which is a test data domain of a program memory.

	7	6	5	4	3	2	1	0
0:FDE0H	COLOSC	—*	—*	—*	—*	—*	—*	—*

32.3.2 The method of programming of Code-Option data

The example program of Code-Option data is shown in Fig. 32-1.

- The case which uses a 32.768kHz crystal oscillation as a low-speed clock

```
;------------------------------------------------------
;       Setting the code-option data
;------------------------------------------------------
        cseg at 0:fde0h
        dw      0080h
;
```

- The case which does not use a 32.768kHz crystal oscillation as a low-speed clock

```
; -----------------------------------------------------
;       Setting the code-option data
; -----------------------------------------------------
        cseg at 0:fde0h
        dw      0000h
;
```

Figure 32-1 The example program of Code-Option data

Note:
Set Code-option data as the test data domain of a program memory.
Set "0FFH"data to test data domains other than Code-option data.

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	size	initial value
0F000H	Data segment register	DSR	–	R/W	8	00H
0F001H	Reset status register	RSTAT	–	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	83H
0F008H	Stop code acceptor	STPACP	–	W	8	Undefined
0F009H	Standby control register	SBYCON	–	W	8	00H
0F00AH	Low-speed time base counter divide register	LTBR	–	R/W	8	00H
0F00BH	High-speed time base counter divide register	HTBDR	–	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register	LTBADJH		R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	–	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	–	R/W	8	02H
0F010H	Interrupt enable register 0	IE0	–	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	–	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	–	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	–	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	–	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	–	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	–	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	–	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	–	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	–	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	–	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	–	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	–	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	–	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	–	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	–	R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	–	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	–	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	–	R/W	8	00H
0F028H	Block control register 0	BLKCON0	–	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	–	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	–	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	–	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	–	R/W	8	00H
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H

0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R	8	04H
0F070H	Frequency status register	FSTAT	−	R/W	8	00H
0F0D0H	Battery Level Detector control register 0	BLDCON0	BLDCON	R/W	8/16	00H
0F0D1H	Battery Level Detector control register 1	BLDCON1		R/W	8	00H
0F0F0H	Bias circuit control register	BIASCON	−	R/W	8	30H
0F0F2H	Display mode register 0	DSPMOD0	−	R/W	8	00H
0F0F4H	Display control register	DSPCON	−	R/W	8	00H
0F100H	Display register 00	DSPR00	−	R/W	8	Undefined
0F101H	Display register 01	DSPR01	−	R/W	8	Undefined
0F102H	Display register 02	DSPR02	−	R/W	8	Undefined
0F103H	Display register 03	DSPR03	−	R/W	8	Undefined
0F104H	Display register 04	DSPR04	−	R/W	8	Undefined
0F105H	Display register 05	DSPR05	−	R/W	8	Undefined
0F106H	Display register 06	DSPR06	−	R/W	8	Undefined
0F107H	Display register 07	DSPR07	−	R/W	8	Undefined
0F108H	Display register 08	DSPR08	−	R/W	8	Undefined
0F109H	Display register 09	DSPR09	−	R/W	8	Undefined
0F10AH	Display register 0A	DSPR0A	−	R/W	8	Undefined
0F10BH	Display register 0B	DSPR0B	−	R/W	8	Undefined
0F10CH	Display register 0C	DSPR0C	−	R/W	8	Undefined
0F10DH	Display register 0D	DSPR0D	−	R/W	8	Undefined
0F10EH	Display register 0E	DSPR0E	−	R/W	8	Undefined
0F10FH	Display register 0F	DSPR0F	−	R/W	8	Undefined
0F110H	Display register 10	DSPR10	−	R/W	8	Undefined
0F111H	Display register 11	DSPR11	−	R/W	8	Undefined
0F112H	Display register 12	DSPR12	−	R/W	8	Undefined
0F113H	Display register 13	DSPR13	−	R/W	8	Undefined
0F114H	Display register 14	DSPR14	−	R/W	8	Undefined
0F115H	Display register 15	DSPR15	−	R/W	8	Undefined
0F116H	Display register 16	DSPR16	−	R/W	8	Undefined
0F117H	Display register 17	DSPR17	−	R/W	8	Undefined
0F118H	Display register 18	DSPR18	−	R/W	8	Undefined
0F119H	Display register 19	DSPR19	−	R/W	8	Undefined
0F11AH	Display register 1A	DSPR1A	−	R/W	8	Undefined
0F11BH	Display register 1B	DSPR1B	−	R/W	8	Undefined
0F11CH	Display register 1C	DSPR1C	−	R/W	8	Undefined
0F11DH	Display register 1D	DSPR1D	−	R/W	8	Undefined
0F11EH	Display register 1E	DSPR1E	−	R/W	8	Undefined
0F11FH	Display register 1F	DSPR1F	−	R/W	8	Undefined
0F120H	Display register 20	DSPR20	−	R/W	8	Undefined
0F121H	Display register 21	DSPR21	−	R/W	8	Undefined

0F122H	Display register 22	DSPR22	–	R/W	8	Undefined
0F123H	Display register 23	DSPR23	–	R/W	8	Undefined
0F124H	Display register 24	DSPR24	–	R/W	8	Undefined
0F125H	Display register 25	DSPR25	–	R/W	8	Undefined
0F126H	Display register 26	DSPR26	–	R/W	8	Undefined
0F127H	Display register 27	DSPR27	–	R/W	8	Undefined
0F200H	NMI data register	NMID	–	R	8	Undefined
0F201H	NMI control register	NMICON	–	R/W	8	00H
0F204H	Port 0 data register	P0D	–	R	8	Undefined
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F208H	Port 1 data register	P1D	–	R	8	Undefined
0F20AH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	00H
0F20BH	Port 1 control register 1	P1CON1		R/W	8	00H
0F210H	Port 2 data register	P2D	–	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	–	R/W	8	00H
0F215H	Port 2 mode register 1	P2MOD1	–	R/W	8	00H
0F218H	Port 3 data register	P3D	–	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	–	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F21DH	Port 3 mode register 1	P3MOD1		R/W	8	00H
0F220H	Port 4 data register	P4D	–	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	–	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H
0F260H	Port C data register	PCD	–	R/W	8	00H
0F261H	Port C direction register	PCDIR	–	R/W	8	00H
0F262H	Port C control register 0	PCCON0	PACON	R/W	8/16	00H
0F263H	Port C control register 1	PCCON1		R/W	8	00H
0F268H	Port D data register	PDD	–	R/W	8	00H
0F269H	Port D direction register	PDDIR	–	R/W	8	00H
0F26AH	Port D control register 0	PDCON0	PBCON	R/W	8/16	00H
0F26BH	Port D control register 1	PDCON1		R/W	8	00H
0F270H	Port E data register	PED	–	R/W	8	00H
0F271H	Port E direction register	PEDIR	–	R/W	8	00H
0F272H	Port E control register 0	PECON0	PACON	R/W	8/16	00H
0F273H	Port E control register 1	PECON1		R/W	8	00H
0F278H	Port F data register	PFD	–	R/W	8	00H
0F279H	Port F direction register	PFDIR	–	R/W	8	00H

0F27AH	Port F control register 0	PFCON0	PBCON	R/W	8/16	00H
0F27BH	Port F control register 1	PFCON1		R/W	8	00H
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	−	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F288H	Serial port 1 transmit/receive buffer L	SIO1BUFL	SIO1BUF	R/W	8/16	00H
0F289H	Serial port 1 transmit/receive buffer H	SIO1BUFH		R/W	8	00H
0F28AH	Serial port 1 control register	SIO1CON	−	R/W	8	00H
0F28CH	Serial port 1 mode register 0	SIO1MOD0	SIO1MOD	R/W	8/16	00H
0F28DH	Serial port 1 mode register 1	SIO1MOD1		R/W	8	00H
0F290H	UART0 transmit/receive buffer	UA0BUF	−	R/W	8	00H
0F291H	UART0 control register	UA0CON	−	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	−	R/W	8	00H
0F298H	UART1 transmit/receive buffer	UA1BUF	−	R/W	8	00H
0F299H	UART1 control register	UA1CON	−	R/W	8	00H
0F29AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F29BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F29CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F29DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F29EH	UART1 status register	UA1STAT	−	R/W	8	00H
0F2A0H	I2C bus 0 receive data register	I2C0RD	−	R	8	00H
0F2A1H	I2C bus 0 slave address register	I2C0SA	−	R/W	8	00H
0F2A2H	I2C bus 0 transmit data register	I2C0TD	−	R/W	8	00H
0F2A3H	I2C bus 0 control register	I2C0CON	−	R/W	8	00H
0F2A4H	I2C bus 0 mode register	I2C0MOD	−	R/W	8	00H
0F2A5H	I2C bus 0 status register	I2C0STAT	−	R	8	00H
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F2D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F2D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F2DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F2DBH	SA-ADC result register 5H	SADR5H		R	8	00H

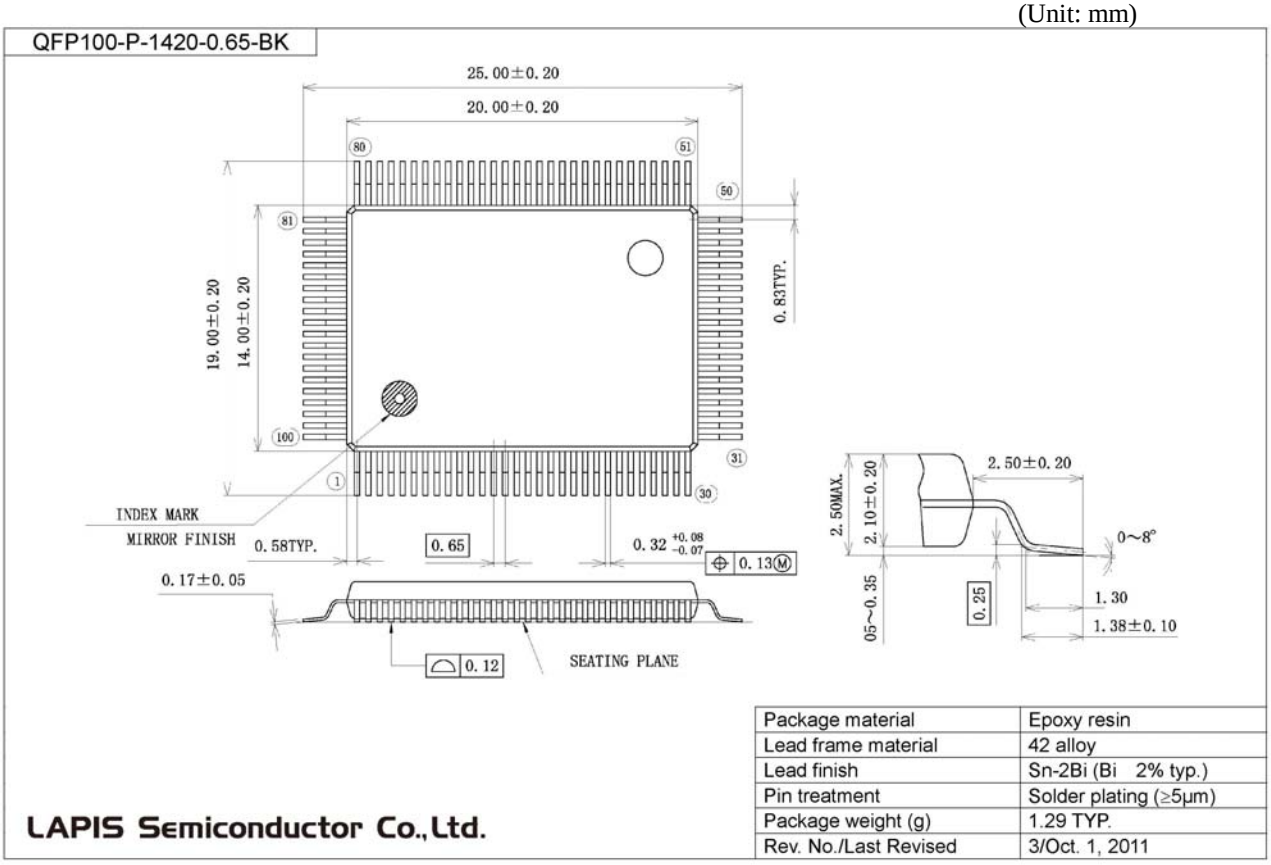
0F2DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F2DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F2DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F2DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F2E0H	SA-ADC result register 8L	SADR8L	SADR8	R	8/16	00H
0F2E1H	SA-ADC result register 8H	SADR8H		R	8	00H
0F2E2H	SA-ADC result register 9L	SADR9L	SADR9	R	8/16	00H
0F2E3H	SA-ADC result register 9H	SADR9H		R	8	00H
0F2E4H	SA-ADC result register AL	SADRAL	SADRA	R	8/16	00H
0F2E5H	SA-ADC result register AH	SADRAH		R	8	00H
0F2E6H	SA-ADC result register BL	SADRBL	SADRB	R	8/16	00H
0F2E7H	SA-ADC result register BH	SADRBH		R	8	00H
0F2E8H	SA-ADC result register CL	SADRCL	SADRC	R	8/16	00H
0F2E9H	SA-ADC result register CH	SADRCH		R	8	00H
0F2EAH	SA-ADC result register DL	SADRDL	SADRD	R	8/16	00H
0F2EBH	SA-ADC result register DH	SADRDH		R	8	00H
0F2ECH	SA-ADC result register EL	SADREL	SADRE	R	8/16	00H
0F2EDH	SA-ADC result register EH	SADREH		R	8	00H
0F2EEH	SA-ADC result register FL	SADRFL	SADRF	R	8/16	00H
0F2EFH	SA-ADC result register FH	SADRFH		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	SADMOD	R/W	8/16	00H
0F2F3H	SA-ADC mode register 1	SADMOD1		R/W	8/16	00H
0F3D8H	Code-Option register 0	CODEOP0	–	R/W	8	00H
0F8A0H	PWM4 period register L	PW4PL	PW4P	R/W	8/16	0FFH
0F8A1H	PWM4 period register H	PW4PH		R/W	8	0FFH
0F8A2H	PWM4 duty register L	PW4DL	PW4D	R/W	8/16	00H
0F8A3H	PWM4 duty register H	PW4DH		R/W	8	00H
0F8A4H	PWM4counter register L	PW4CL	PW4C	R/W	8/16	00H
0F8A5H	PWM4 counter register H	PW4CH		R/W	8	00H
0F8A6H	PWM4 control register 0	PW4CON0	PW4CON	R/W	8/16	00H
0F8A7H	PWM4 control register 1	PW4CON1		R/W	8	40H
0F8A8H	PWM4 control register 2	PW4CON2	–	R/W	8	00H
0F8A9H	PWM4 control register 3	PW4CON3		R/W	8	10H
0F8B0H	PWM4 period register L	PW5PL	PW5P	R/W	8/16	0FFH
0F8B1H	PWM4 period register H	PW5PH		R/W	8	0FFH
0F8B2H	PWM4 duty register L	PW5DL	PW5D	R/W	8/16	00H
0F8B3H	PWM4 duty register H	PW5DH		R/W	8	00H
0F8B4H	PWM4counter register L	PW5CL	PW5C	R/W	8/16	00H
0F8B5H	PWM4 counter register H	PW5CH		R/W	8	00H
0F8B6H	PWM4 control register 0	PW5CON0	PW5CON	R/W	8/16	00H
0F8B7H	PWM4 control register 1	PW5CON1		R/W	8	40H
0F8B8H	PWM4 control register 2	PW5CON2		R/W	8	00H
0F8E0H	Timer 8 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 8 counter register	TM8C		R/W	8	00H

0F8E2H	Timer 8 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 8 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 9 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 9 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 9 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 9 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer A data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer A counter register	TMAC		R/W	8	00H
0F8EAH	Timer A control register 0	TMACON0	TMACON	R/W	8/16	00H
0F8EBH	Timer A control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer B data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer B counter register	TMBC		R/W	8	00H
0F8EEH	Timer B control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer B control register 1	TMBCON1		R/W	8	00H
0F8F1H	LCD port segment selection register 1	LSELS1	−	R/W	8	00H
0F8F2H	LCD port segment selection register 2	LSELS2	−	R/W	8	00H
0F8F3H	LCD port segment selection register 3	LSELS3	−	R/W	8	00H
0F8F4H	LCD port segment selection register 4	LSELS4	−	R/W	8	00H

Appendix B Package Dimensions

ML610Q178

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.29 TYP.
Rev. No./Last Revised	3/Oct. 1, 2011

Figure B-1 P-QFP100

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C Electrical Characteristics

• Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 3	V_{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V_{L1}	Ta = 25°C	−0.3 to +2.33	V
Power supply voltage 5	V_{L2}	Ta = 25°C	−0.3 to +4.66	V
Power supply voltage 6	V_{L3}	Ta = 25°C	−0.3 to +7.0	V
Reference voltage	V_{REF}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3,4,5,6,C,D,E,F Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2,9 Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T_{STG}	—	−55 to +150	°C

• Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +85	°C
Operating voltage	V_{DD}	—	2.2 to 5.5	V
Reference voltage	V_{REF}	—	4.5 to V_{DD}	V
Analog input voltage	V_{AI}	—	V_{SS} to V_{REF}	
Operating frequency (CPU)	f_{OP}	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Capacitor externally connected to V_{DD} pin	C_V	—	10±30%	μF
Capacitor externally connected to V_{PP} pin	C_1	—	1±30%	μF
Capacitor externally connected to V_{ref} pin	C_{AV}	—	1±30%	μF
Low-speed crystal oscillation external capacitor	C_{DL}	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C_{GL}		12 to 25	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	8M/8.192M	Hz
High-speed crystal oscillation external capacitor*	C_{DH}	—	47±30%	pF
	C_{GH}	—	47±30%	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	μF

* C_{GH} and C_{DH} are built into, external capacity is unnecessary for CSTLS8M00G56 (made by Murata Mfg.).

• Operating Conditions of Flash Memory

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.7 to 5.5	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase[1]	7.7 to 8.3	
Maximum rewrite count	C_{EP}	—	80	times
Data retention period	Y_{DR}	—	10	years

*1: At the writing of a flash ROM, it is necessary to supply voltage to V_{DDL} pin within the limits of the above-mentioned regulation. Pulldown resistance is built in the V_{PP} pin.

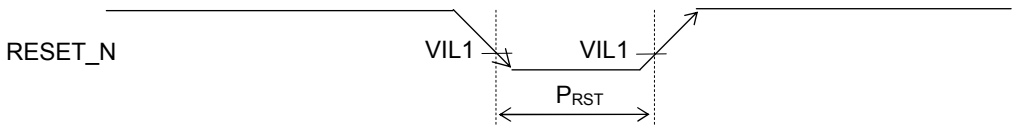
• DC Characteristics (1 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed crystal oscillation start time	T_{XTH}	—	—	2	20	ms	1
Low-speed crystal oscillation start time*2	T_{XTL}	—	—	0.6	2	s	
Low-speed RC oscillator frequency	f_{LCR}	Ta= -10 to 60°C	Typ -5%	32.7k	Typ +5%	Hz	
PLL oscillation frequency	f_{PLL}	LSCLK=32.768kHz 100 clock average	Typ -1%	8.192	Typ +1%	MHz	
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		

*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance C_{GL}/C_{DL}=12pF.

• RESET



Reset by RESET_N pin

• DC Characteristics (2 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	Ta = 25°C	LD3 to 0 = 0H	Typ. -2%	2.35	Typ. +2%	V	1
			LD3 to 0 = 3H		2.80			
			LD3 to 0 = 9H		3.70			
			LD3 to 0 = FH		4.60			

• DC Characteristics (3 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state Low-speed/high-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	0.7	6	μA	1
			-40 to +85°C	—	0.7	22		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WBC: Operating*2) High-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	2.0	7		
			-40 to +85°C	—	2.0	24		
Supply current 3	IDD3	CPU: Running at 32kHz*1 High-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	13	20		
			-40 to +85°C	—	13	42		
Supply current 4	IDD4	CPU: Running at 8.192MHz Crystal/ceramic oscillating mode*2 V_{DD} = SPV_{DD} = 5.0V		—	5	8	mA	

*1: Case when the CPU operating rate is 100% (with no HALT state)
*2 : Significant bits of BLKCON0 to BLKCON4 registers are all "1".

• DC Characteristics (4 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23) (P90-P93)	VOL2	When LED drive mode is selected	IOL2 = +10mA $V_{DD} \geq$ 4.5V	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	When I^2C mode is selected	IOL3 = +3mA	—	—	0.4		
Output leakage current (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Output current 1 COM0 to COM3	IOL1	VL3=3V、VOL=0.3V		15	40	—	μA	3
		VL3=5V、VOL=0.5V		100	200	—		
	IOH1	VL3=3V、VOH=2.7V		—	-30	-15		
		VL3=5V、VOH=4.5V		—	-90	-45		
Output current 2 SEG0 to SEG39	IOL2	VL3=3V、VOL=0.3V		15	30	—		
		VL3=5V、VOL=0.5V		70	150	—		
	IOH2	VL3=3V、VOH=2.7V		—	-13	-6		
		VL3=5V、VOH=4.5V		—	-40	-20		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}		–1500	–300	–20		
Input current 2 (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	IIH2	VIH2 = V_{DD} (when pulled down)		2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)		–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		-1	—	—		
Input current 3 (TEST0)	IIH3	VIH3 = V_{DD}		20	300	1500		
	IIL3	VIL3 = V_{SS}		-1	—	—		

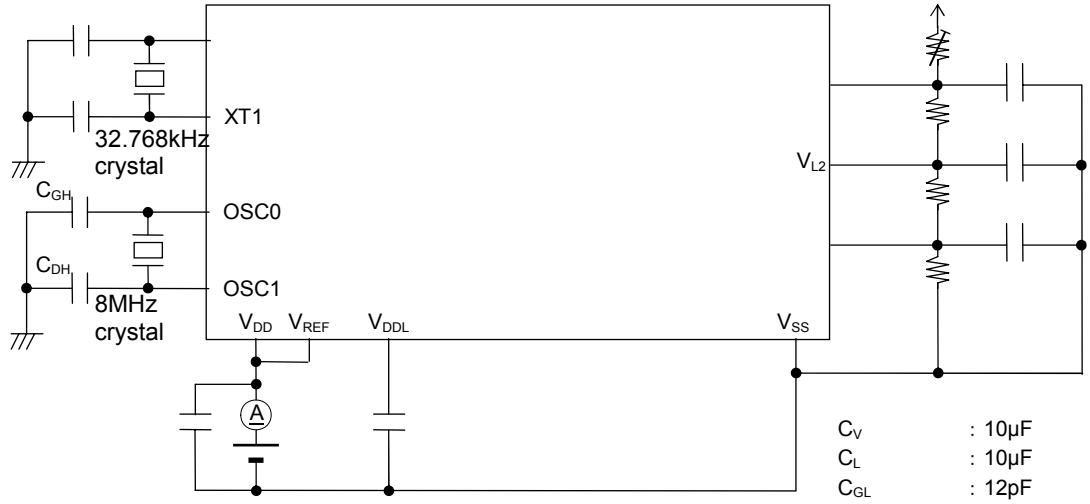
• DC Characteristics (5 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P43) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Input pin capacitance (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P43) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

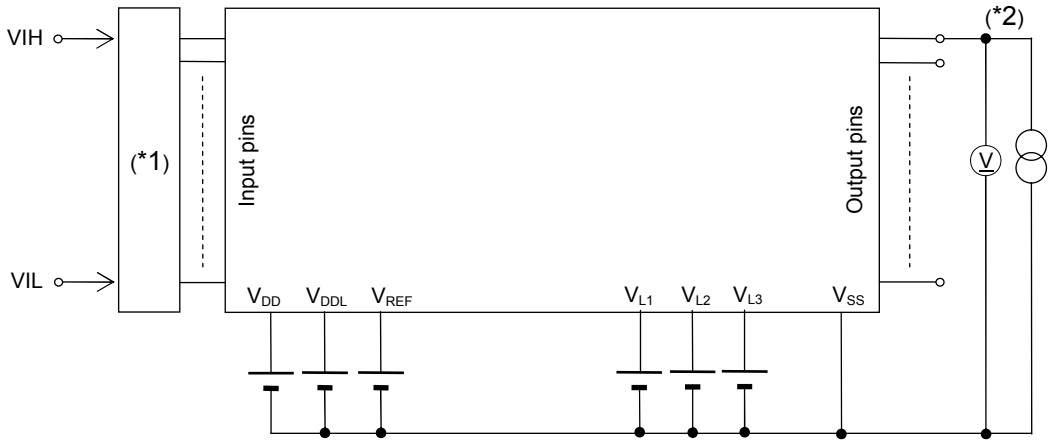
• Measuring circuit

Measuring Circuit 1



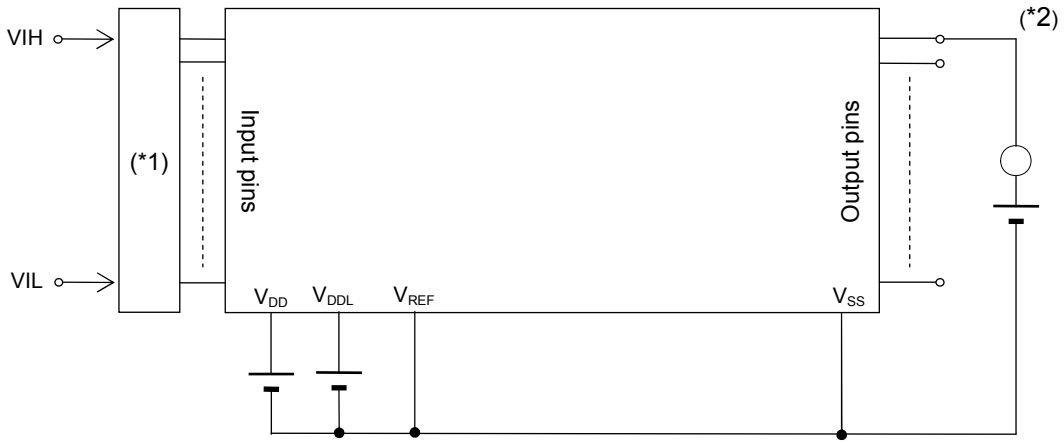
C_V : 10µF
C_L : 10µF
C_{GL} : 12pF
C_{DL} : 12pF
C_{GH} : 47pF
C_{DH} : 47pF
C_a,C_b,C_c : 0.22µF
32.768kHz Crystal oscillator
(DMX-26 DAISHINKU Corp.)
8MHz Crystal oscillator
CSTLS8M00G56 (MURATA Corp.) it has built-in C_{GH}, and C_{DH}

Measuring Circuit 2



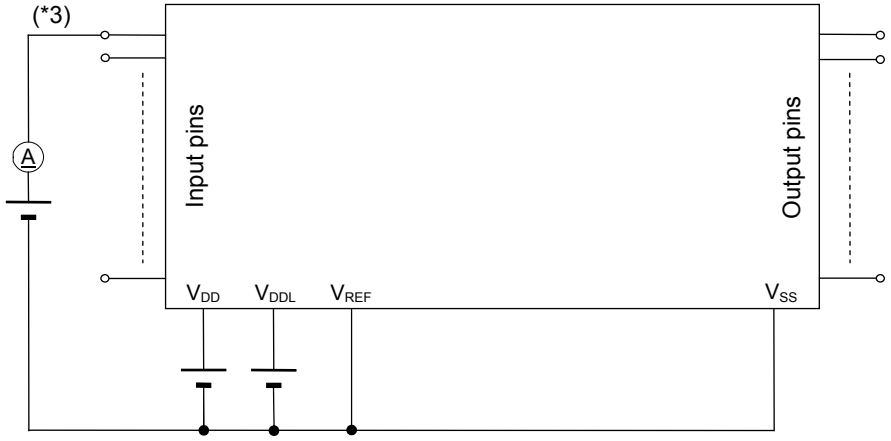
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring Circuit 3



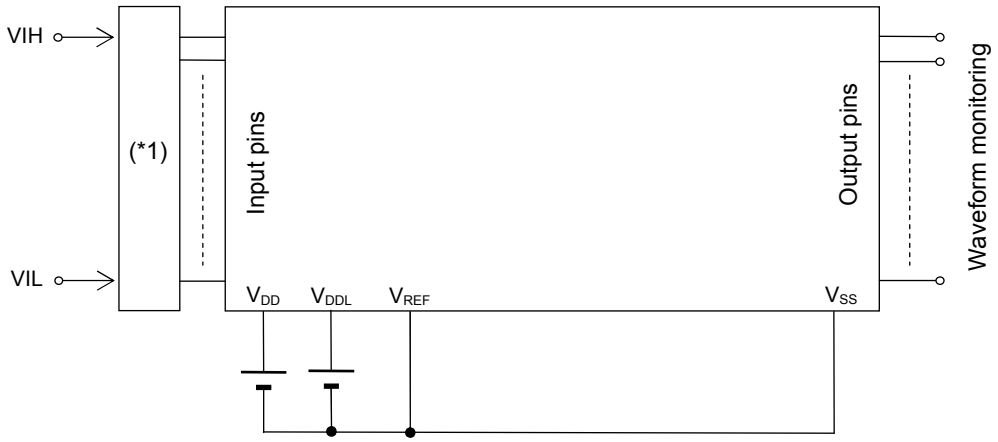
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring Circuit 4



*3: Measured at the specified input pins.

Measuring Circuit 5

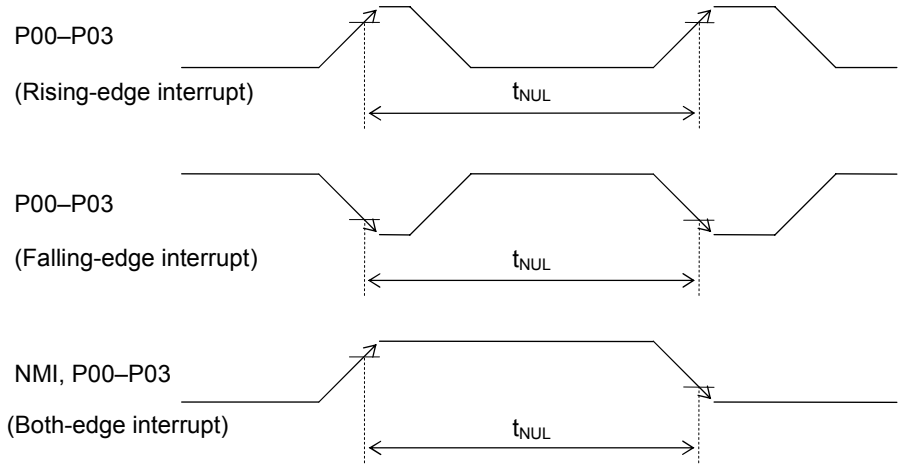


*1: Input logic circuit to determine the specified measuring conditions.

• AC Characteristics (External Interrupt)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× sysclk	—	3.5× sysclk	μs

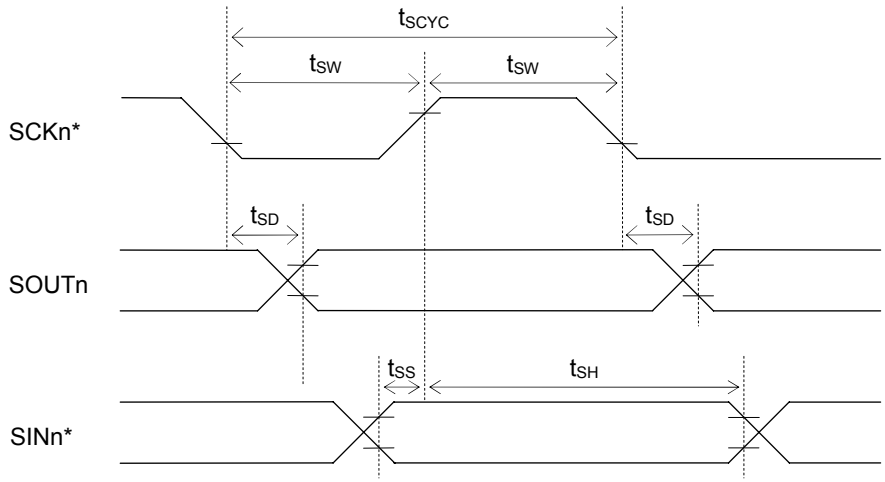


• AC Characteristics (Synchronous Serial Port)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	μs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	μs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIOnMOD1)



*: Indicates the secondary function of the corresponding port.

• AC Characteristics (I^2C bus interface : Standard mode 100kHz)

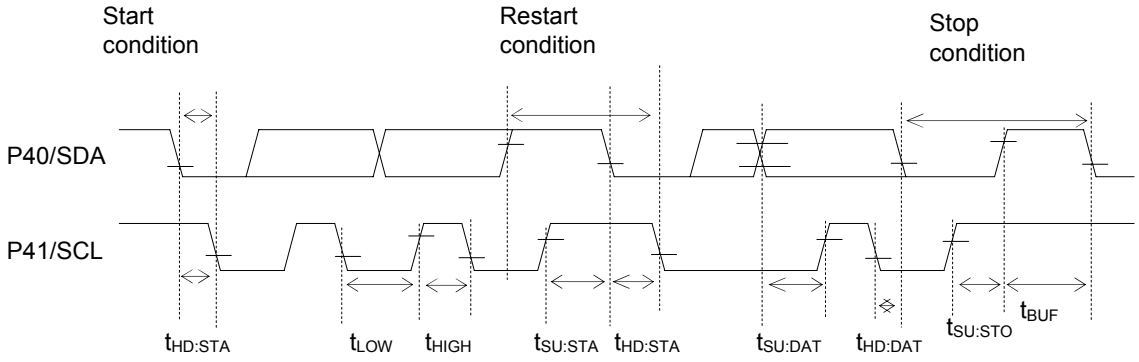
(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

• AC Characteristics (I^2C bus interface : Fast mode 400kHz)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

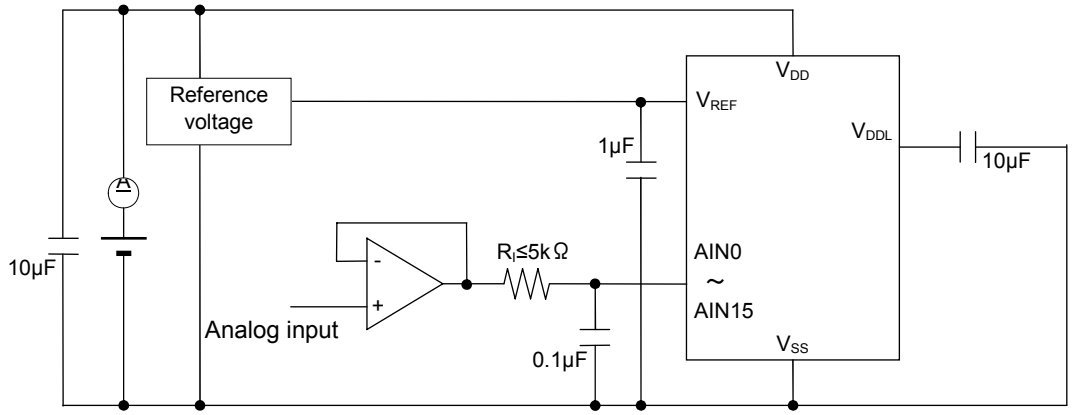


• Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

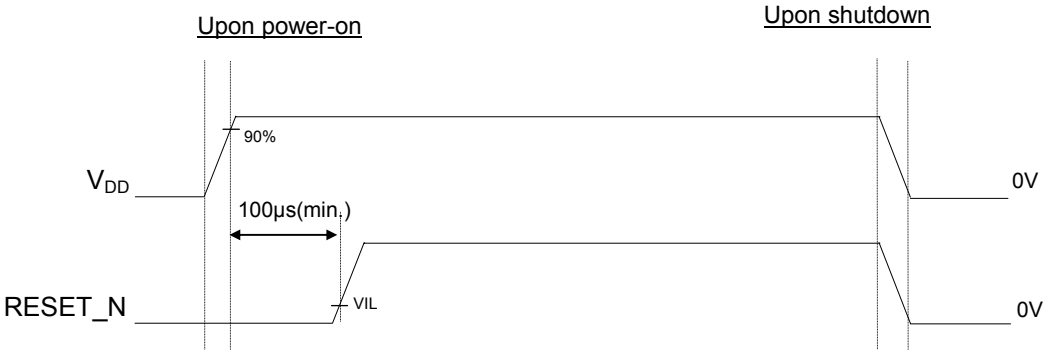
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 5.5V	–4	—	+4	LSB
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	–3	—	+3	
Zero-scale error	V_{OFF}	—	–4	—	+4	
Full-scale error	FSE	—	–4	—	+4	
Input impedance	R_I	—	—	—	5k	Ω
Reference voltage	V_{REF}		4.5	—	V_{DD}	V
Conversion time	t_{CONV}	HSCLK=3.0M to 8.4MHz	—	102	—	φ/CH

φ: Period of high-speed clock (HSCLK)

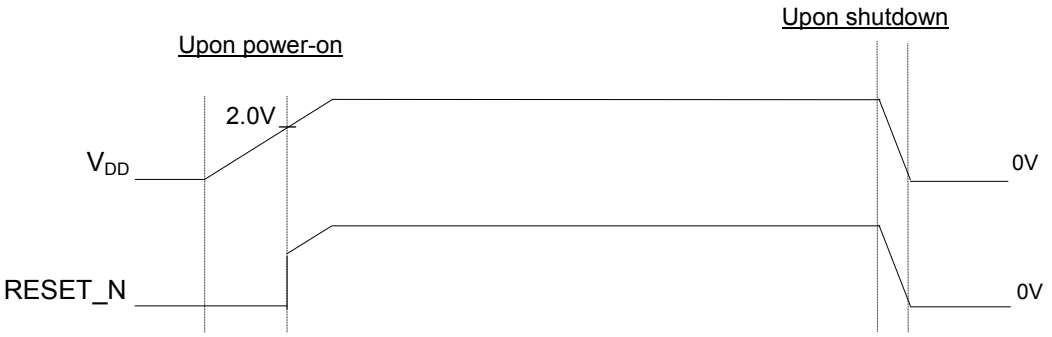


• Power-on/Shutdown Sequence

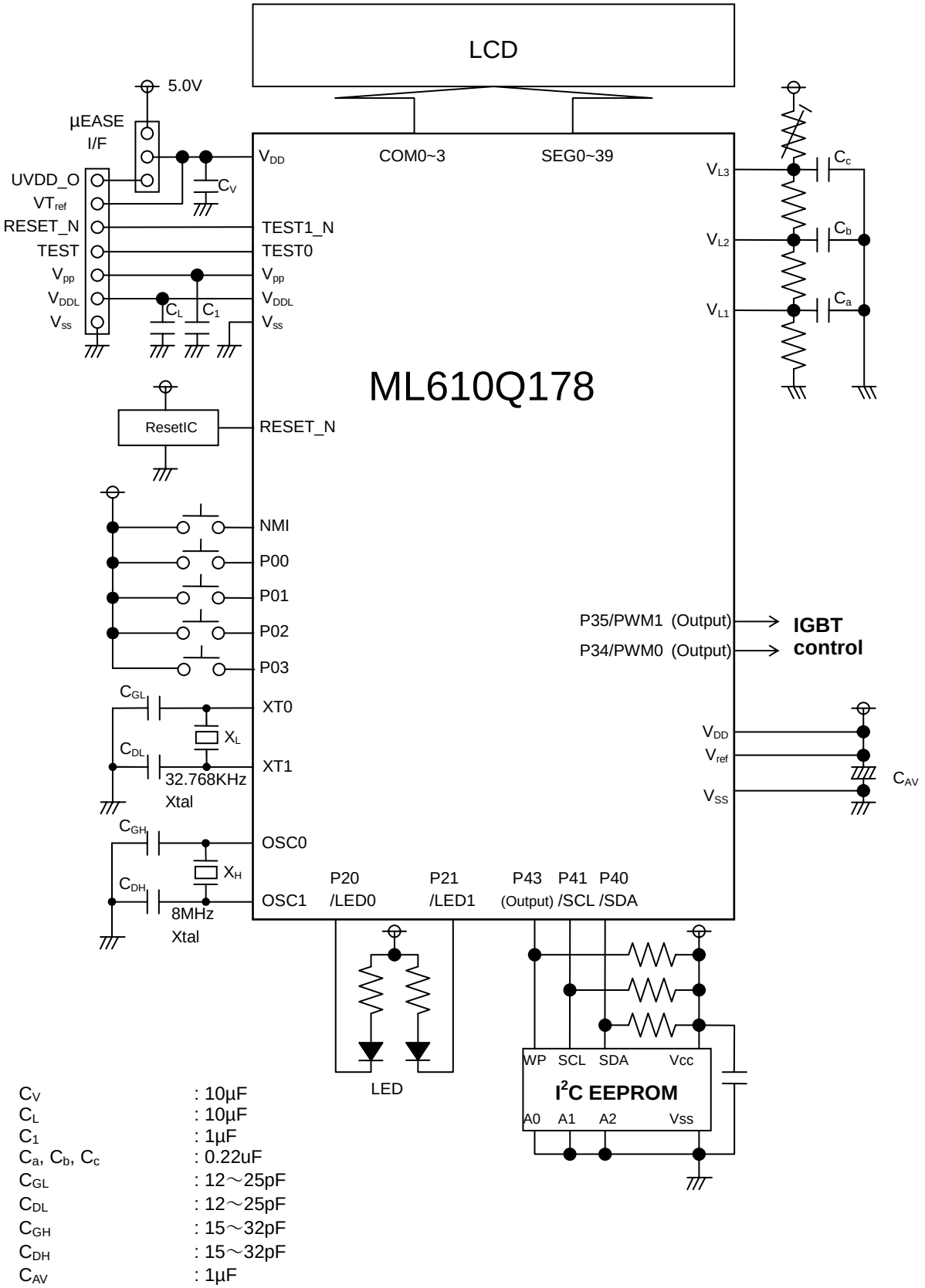
■ When the power rise time is 100 µs or less



■ When the power rise time is more than 100 µs



Appendix D The example of an application circuit



C_V	: 10µF
C_L	: 10µF
C_1	: 1µF
C_a, C_b, C_c	: 0.22uF
C_{GL}	: 12～25pF
C_{DL}	: 12～25pF
C_{GH}	: 15～32pF
C_{DH}	: 15～32pF
C_{AV}	: 1µF

Appendix E Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview

•About unused pins

[ ] Please confirm how to handle the unused pins(Refer to Section 1.3.4 in the user's manual).

Chapter 2 CPU and Memory Space

• Program Code size

[ ] 130,048 Byte (0:0000H～1:FFFFH)

• Data Memory size

[ ] 130,048 Byte (0:0000H～1:FFFFH)

• Data RAM size

[ ] 4,096 Byte (0:E000H～0:EFFFH)

• Unused area

[ ] Please fill test area 0:FC00H to 0:FDFFH with BRK instruction code "0FFH" (Refer to a startup file "ML610Q178A.asm" for programming in the source code).

[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". Please fill the area with the code "0FFH" when you release a code for LAPIS Semiconductor's factory programming.

• Initializing RAM

[ ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Reset Function

• Reset activation pulse width

[ ] Minimum 100us (Refer to Appendix C-2 in the user's manual)

[ ] There is no flag which shows that the reset by RESET_N pin occurred. (Refer to 3.2.2 in the user's manual)

• BRK instruction reset

[ ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore initialize the SFRs by your software. (Refer to 3.3.1 in the user's manual)

Chapter 4 MCU Control Function

•STOP mode

[ ] When the MIE flag is "0", the stop code acceptor (STPACP) cannot be enabled under the condition where both the interrupt enable and request flags become "1" (Refer to Sections 4.2.2 and 4.2.3. in the user's manual).

[ ] Place two NOP instructions next to the instruction that sets the STP bit to "1" (Refer to Section 4.3.3. in the user's manual).

•HALT mode

[ ] Place two NOP instructions next to the instruction that sets the HLT bit to "1" (Refer to Section 4.3.2. in the user's manual).

•BLKCON register

[ ] BLKCON registers enable or disable corresponsive each peripheral (Refer to Section 4.2.4 - 4.2.7. in the user's manual).

[ ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

Chapter 5 Interrupts(INTs)

•Unused interrupt vector table

[ ] Please define all unused interrupt vector tables for fail safe.

•Non-maskable interrupt

[ ] The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE flag (Refer to Sections 5.2.10. and 5.3 in the User's Manual).

Chapter 6 Clock Generation Circuit

•Initial System clock

[ ] At power up or system reset, the 16MHz PLLl oscillation clock oscillates and 2MHz clock which is 1/8 of 16MHz is supplied to CPU as the system clock.

•Switching high-speed clock operation mode to low-speed clock operation mode

[ ] When switching the high-speed clock to the low-speed clock after the recovery from the STOP mode, make sure the low-speed clock is oscillating checking to see the low-speed time base counter's Q128H bit becomes "1".

•Port secondary function setting

[ ] Specify the secondary function for the port 2 when driving a clock to the pin(Refer to Section 6.4 in the user's manual).

Chapter 7 Time Base Counter

•HTBCLK

[ ] When using the HTBCLK for a timer, set an arbitrary dividing ratio in the high-speed side time base counter frequency divide register (HTBDR register) (see Section 7.2.3. in the User's Manual).

•How to read LTBC

[ ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Refer to Section 7.3.1 in the user's manual).

Chapter 8 Timers

•How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 8.2.8 to 8.2.13 in the user's manual).

Chapter 9 Watchdog Timer

•Overflow period

Clear WDT during the selected overflow period:

[ ] 125ms, [ ] 500ms, [ ] 2s, [ ] 8s

•WDP

[ ] Check the WDP content before writing to the WDTCON register, then determine writing whether "5AH" or "0A5H" (Refer to Section 9.2.2. in the user's manual).

Chapter 10 PWM

•Pins used

[ ] P34 pin or P43 pin is used

[ ] P35 pin or P47 pin is used

•How to read the registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 10.2.4 , 10.2.11 in the user's manual).

•Port tertiary function setting

[ ] Specify the tertiary function for the port (Refer to Section 10.4 in the user's manual).

Chapter 11 Synchronous Serial Port

•Pins used

[ ] P40(SIN0), P41(SCK0) and P42(SOUT0) are used, or P44(SIN0), P45(SCK0) and P46(SOUT0) are used.

[ ] P50(SIN1), P51(SCK1) and P52(SOUT1)

•Port secondary and tertiary function setting

[ ] Specify the secondary Function for the port(Refer to Section 11.4 in the user's manual).

Chapter 12 UART

•Pins used

[ ] P02(RXD0) or P42(RXD0) is used.

[ ] P03(RXD1) or P52(RXD1) is used.

[ ] P43(TXD0) or P53(TXD0) is used.

[ ] P53(TXD1) or P43(TXD1) is used.

[ ] Select the P02 or P42 for RXD0 by specifying U0RSEL bit of UA0MOD0 register.

[ ] Select the P03 or P52 for RXD0 by specifying U1RSEL bit of UA1MOD0 register.

•Port secondary function setting

[ ] Specify the secondary Function for the port(Refer to Section 12.4 in the user's manual).

Chapter 13 I^2C Bus Interface

[ ] P40(SDA) pin and P41(SCL) pin used.

[ ] Specify the secondary Function for the port(Refer to Section 13.4 in the user's manual).

Chapter 14 NMI Pin

•Pins used

[ ] Don't leave Hi-impedance NMI pin in floating state.

Chapters 15 to 26 Port

•Pin Handling

[ ] Don't leave Hi-impedance Input ports in floating state.

•Port secondary Function

[ ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port.

Chapters 27 LCD

•bias

[ ] 1/3 bias or [ ] 1/2 bias.

•The select of an I/O Port and a segment driver output

[ ] Set up the choice of an I/O Port or segment driver output by the LCD port segment registers 1 to 4.

Chapter 28 Successive Approximation Type A/D Converter

•Operating Conditions

[ ] Please confirm voltage of operation and a clock frequency.
HSCLK = 3MHz – 8.4MHz, AVDD=4.5V~5.5V

[ ] Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).

[ ] Do not start A/D conversion with all of bits SACHF to SACH0 of the SA-ADC mode register 0 (SADMOD0) and the SA-ADC mode register 1 (SADMOD1) set to "0". （Please refer to clause 28.2.35-28.2.37 in the user's manual.）

Chapter 29 Battery Level Detector

[ ] Please select the threshold voltage when the BLD circuit is OFF.

Chapter 31 On-Chip Debug Function

• Operating Conditions

[ ] Supply a voltage from 2.7V to 5.5V to the VDD pin when programming (erasing and writing) the Flash ROM with LAPIS semiconductor development tool uEASE.

[ ] Please do not apply LSIs being used for debugging to mass production.

[ ] Please validate the ROM code on your production board without LAPIS semiconductor development tool uEASE.

Chapter 32 Code-Option

[ ] Set Code-option data as the test data domain of a program memory.

[ ] Set "0FFH"data to test data domains other than Code-option data.

Appendix A SFR (Specific Function Registers)

•Initial value

[ ] Please confirm there are some SFRs have undefined initial value at reset (Refer to Appendix A in the user's manual).

Appendix C Electrical Characteristics

•External capacitors for Power circuits

[ ] CL=10uF （connected to VDDL pin）, [ ] Cv =10uF (connected to VDD pin）

•Operating voltage

[ ] 2.2V to 5.5V

•Operating temperature

[ ] -40'C to +85'C

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL610Q178-01	Jun. 8, 2012	–	–	Formal edition 1.0