

High and Low Side Driver

Features

- Floating channel designed for bootstrap operation
- Fully operational to 200V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground +/-5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Shut down input turns off both channels
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description

The IR2010 is a high power, high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

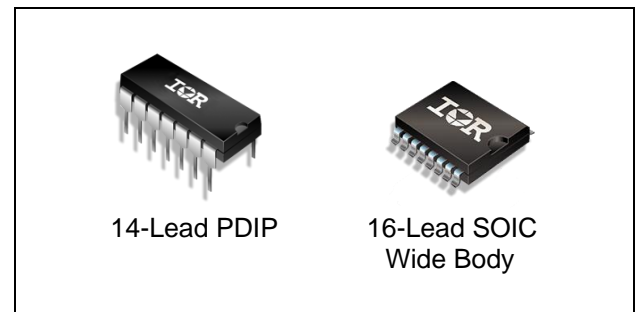
Applications

- Converters
- DC motor drive

Product Summary

V_{OFFSET} (max)	200V
$I_{\text{O+/-}}$ (typ)	3.0A / 3.0A
V_{OUT}	10 – 20V
$t_{\text{on/off}}$ (typ)	95ns & 65ns
Delay Matching (max)	15ns

Package Options



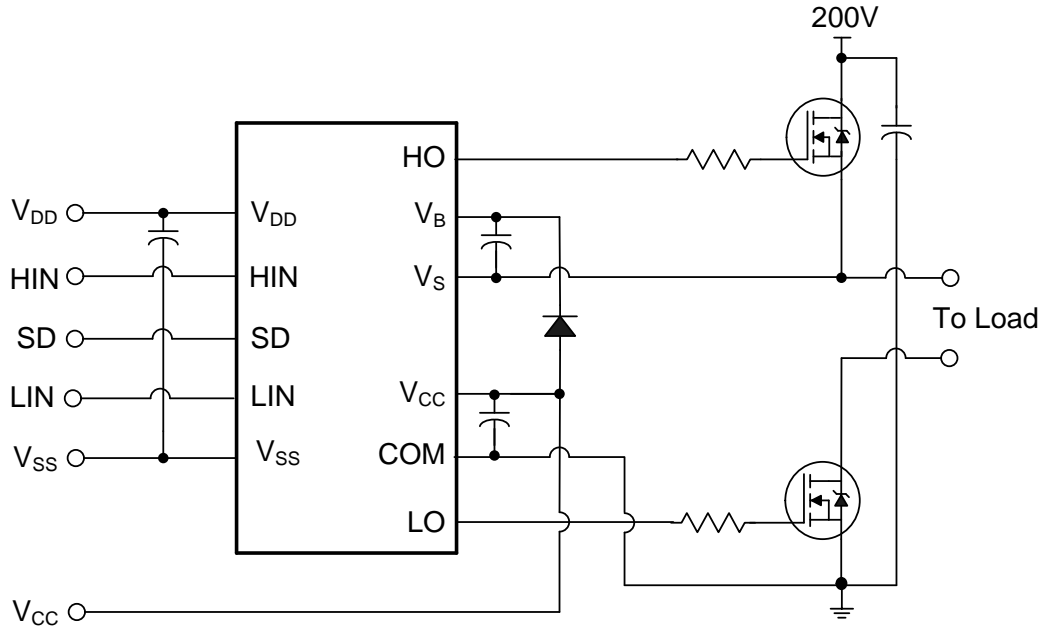
14-Lead PDIP

16-Lead SOIC
Wide Body

Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR2010PBF	PDIP14	Tube	25	IR2010PBF
IR2010SPBF	SO16W	Tube	45	IR2010SPBF
IR2010SPBF	SO16W	Tape and Reel	1000	IR2010STRPBF

Typical Connection Diagram



(Refer to Lead Assignments for correct configuration.) This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V_B	High side floating supply voltage	-0.3	225	V	
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$		
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
V_{CC}	Low side fixed supply voltage	-0.3	25		
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$		
V_{DD}	Logic supply voltage	-0.3	$V_{SS} + 25$		
V_{SS}	Logic supply offset voltage	$V_{CC} - 25$	$V_{CC} + 0.3$		
V_{IN}	Logic input voltage (HIN, LIN & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$		
dV_S/dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns	
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	14-Lead PDIP	—	1.6	W
		16-Lead SOIC	—	1.25	
R_{thJA}	Thermal resistance, junction to ambient	14-Lead PDIP	—	75	$^\circ\text{C/W}$
		16-Lead SOIC	—	100	
T_J	Junction temperature	—	150	$^\circ\text{C}$	
T_S	Storage temperature	-55	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 24 and 25.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	†	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	$V_{SS} + 3$	$V_{SS} + 20$	
V_{SS}	Logic supply offset voltage	-5 ^{††}	5	
V_{IN}	Logic input voltage (HIN, LIN, & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

† Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to $-V_{BS}$.

†† When $V_{DD} < 5\text{V}$, the minimum V_{SS} offset is limited to $-V_{DD}$
(Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000pF and T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	50	95	135	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	8	30	65	105		$V_S = 200V$
t_{sd}	Shutdown propagation delay	9	35	70	105		
t_r	Turn-on rise time	10	—	10	20		
t_f	Turn-off fall time	11	—	15	25		
MT	Delay matching, HS & LS turn-on/off	6	—	—	15		

Static Electrical Characteristics

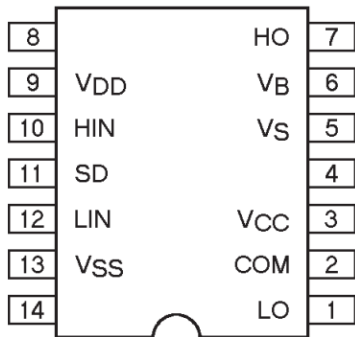
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V and T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	$V_{DD} = 15V$
V_{IL}	Logic "0" input voltage	13	—	—	6.0		$V_{DD} = 3.3V$
V_{IH}	Logic "1" input voltage	12	2	—	—		$I_O = 0A$
V_{IL}	Logic "0" input voltage	13	—	—	1		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.0	μA	$V_B = V_S = 200V$
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		$V_{IN} = 0V$ or V_{DD}
I_{LK}	Offset supply leakage current	16	—	—	50		$V_{IN} = V_{DD}$
I_{QBS}	Quiescent V_{BS} supply current	17	—	70	210		$V_{IN} = 0V$
I_{QCC}	Quiescent V_{CC} supply current	18	—	100	230		
I_{QDD}	Quiescent V_{DD} supply current	19	—	1	5		
I_{IN+}	Logic "1" input bias current	20	—	20	40	V	
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.5	8.6	9.7	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O+}	Output high short circuit pulsed current	26	2.5	3.0	—	A	
I_{O-}	Output low short circuit pulsed current	27	2.5	3.0	—		

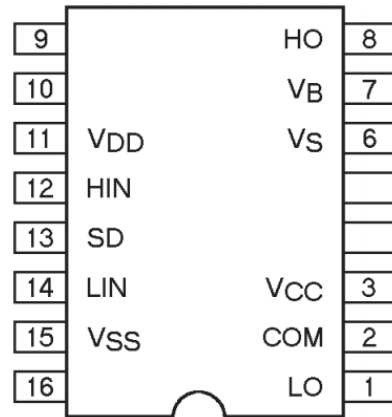
Lead Definitions

Symbol	Description
V _{DD}	Logic Supply
HIN	Logic input for high side gate driver outputs (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver outputs (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14-Lead PDIP



16-Lead SOIC (Wide Body)

Application Information and Additional Details

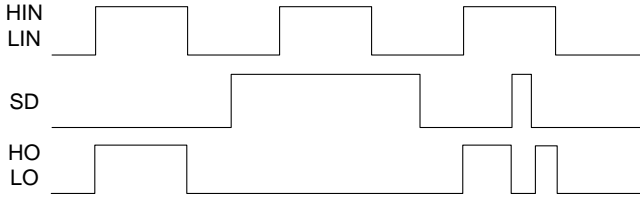


Figure 1. Input/Output Timing Diagram

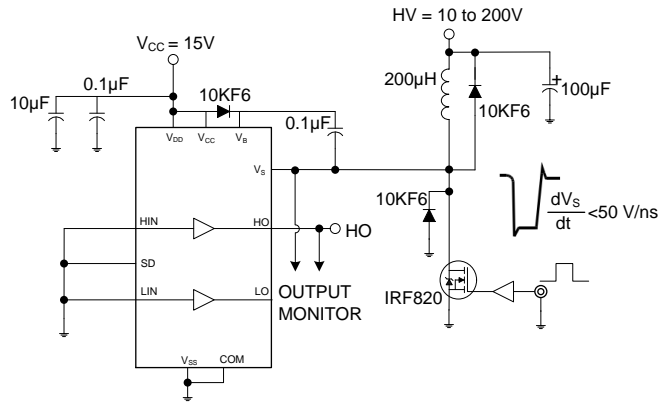


Figure 2. Floating Supply Voltage Transient Test Circuit

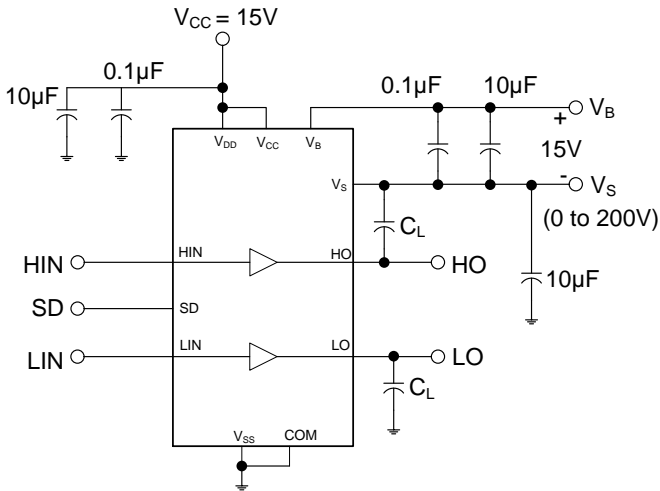


Figure 3. Switching Time Test Circuit

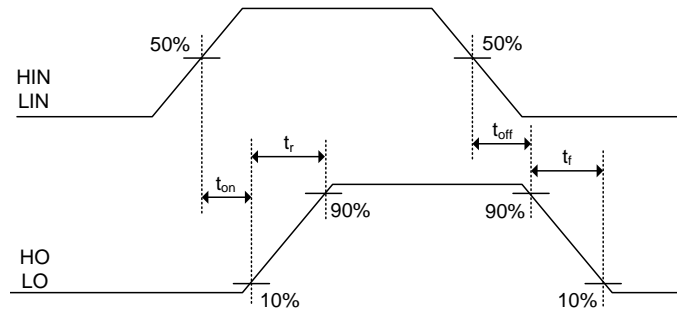


Figure 4. Switching Time Waveform Definition

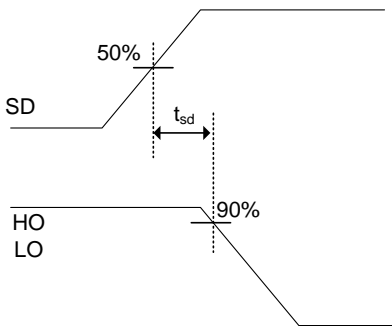


Figure 5. Shutdown Waveform Definitions

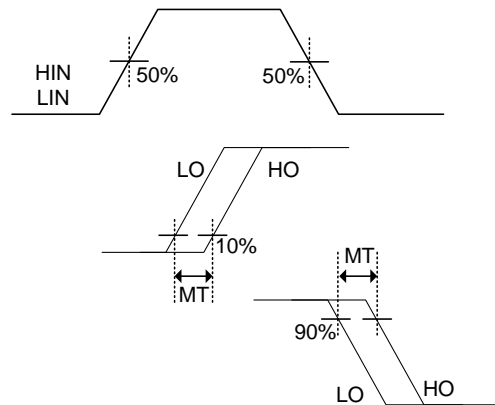


Figure 6. Delay Matching Waveform Definitions

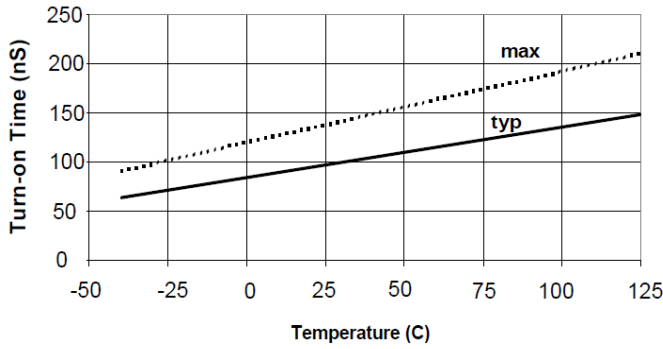


Figure 7A. Turn-on Time vs. Temperature

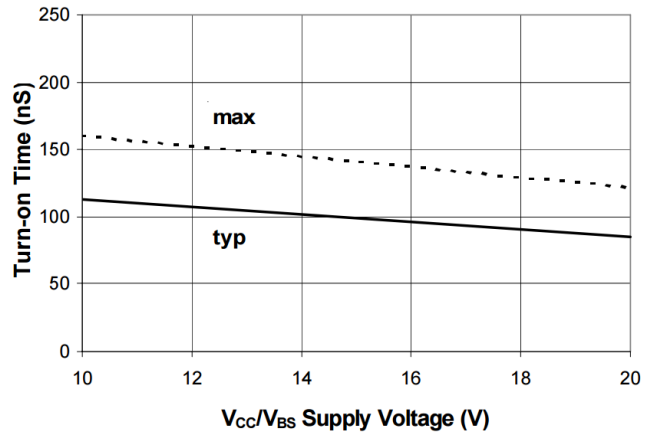


Figure 7B. Turn-on Time vs. V_{CC}/V_{BS} Voltage

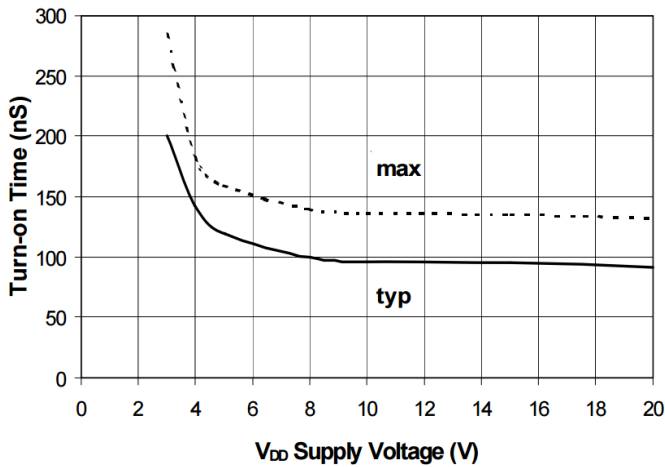


Figure 7C. Turn-on Time vs. V_{DD} Voltage

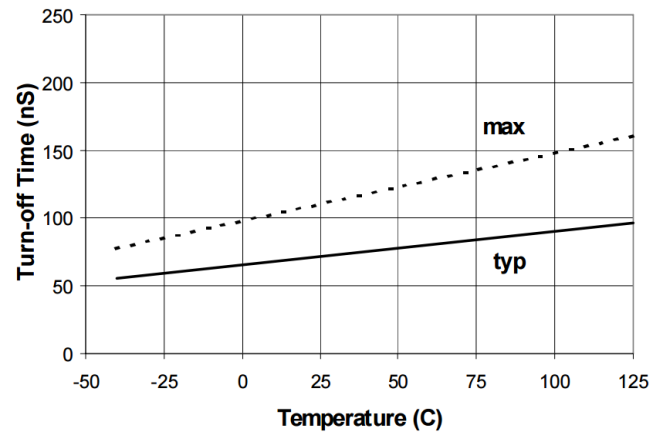


Figure 8A. Turn-off Time vs. Temperature

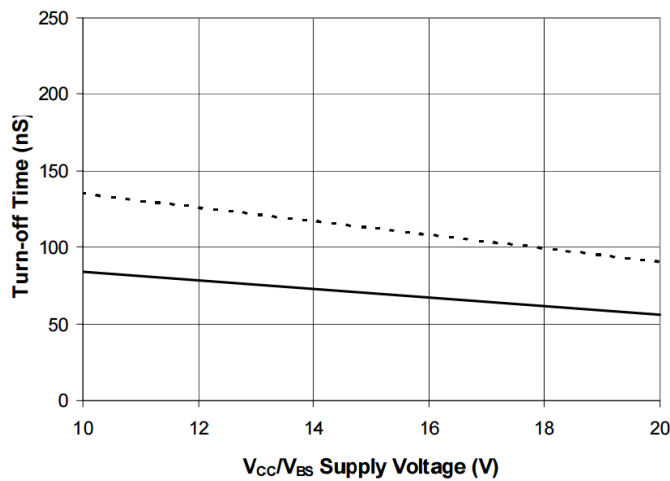


Figure 8B. Turn-off Time vs. V_{CC}/V_{BS} Voltage

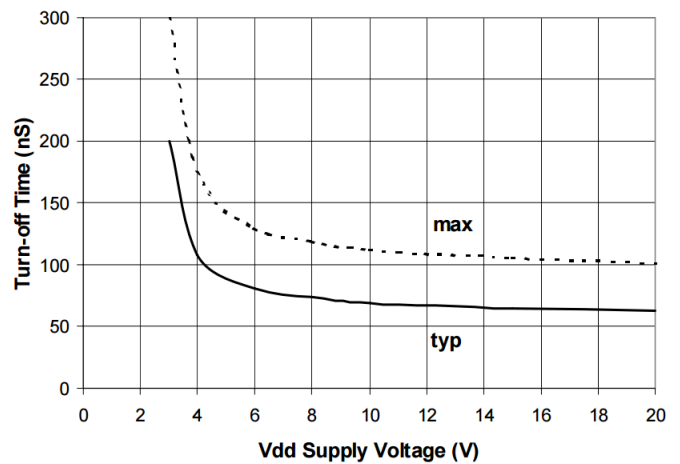


Figure 8C. Turn-off Time vs. V_{DD} Voltage

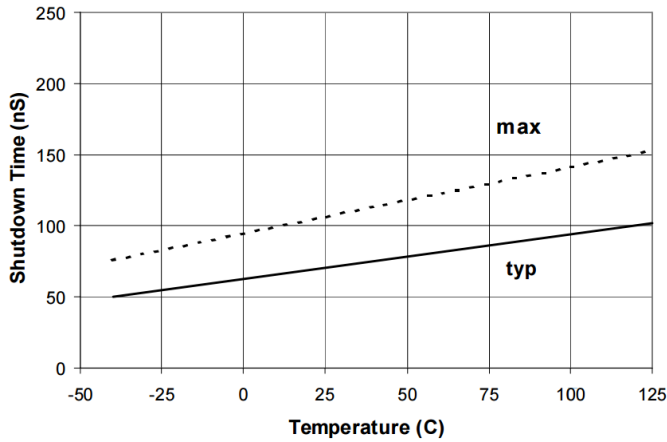


Figure 9A. Shutdown Time vs. Temperature

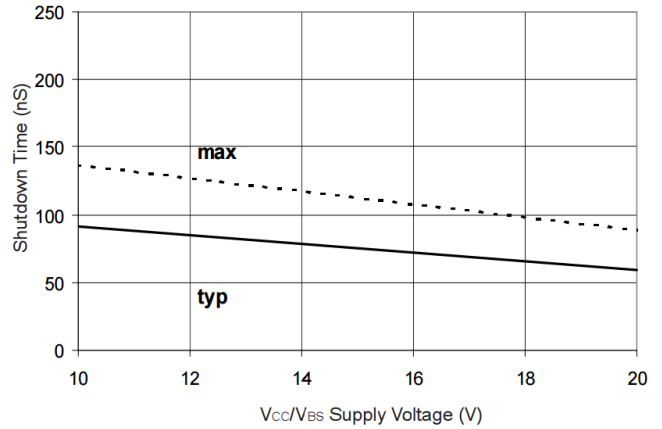


Figure 9B. Shutdown Time vs. V_{CC}/V_{BS} Voltage

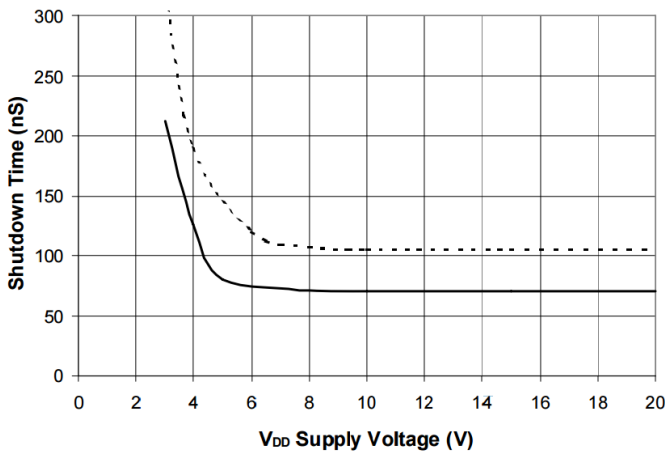


Figure 9C. Shutdown Time vs. V_{DD} Voltage

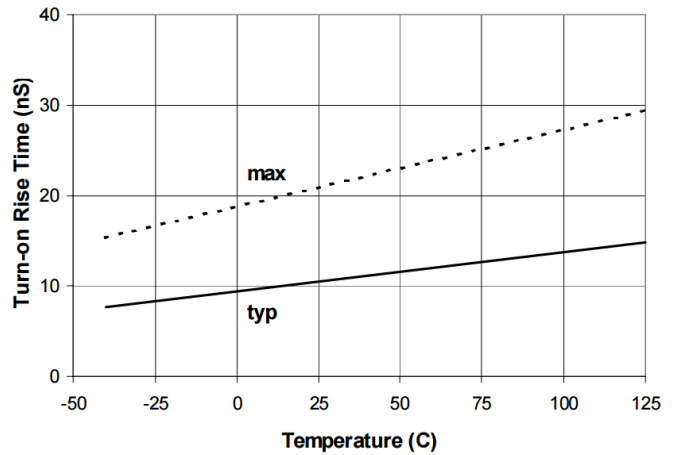


Figure 10A. Turn-on Rise Time vs. Temperature

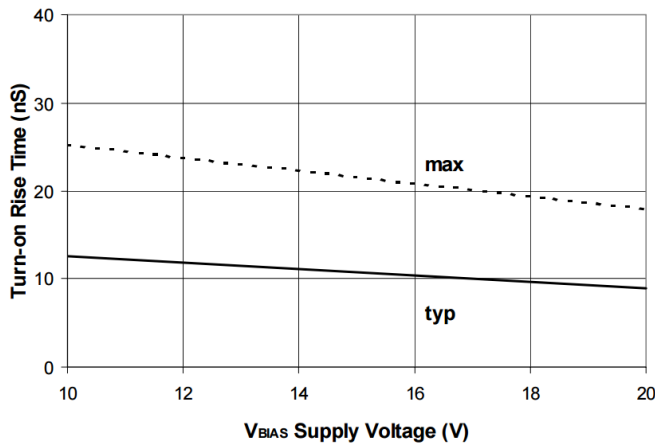


Figure 10B. Turn-on Rise Time vs. V_{BIAS} ($V_{CC}=V_{BS}=V_{DD}$) Voltage

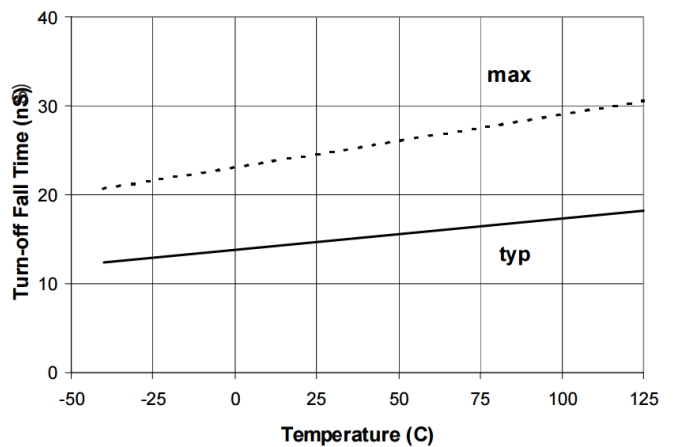


Figure 11A. Turn-off Fall Time vs. Temperature

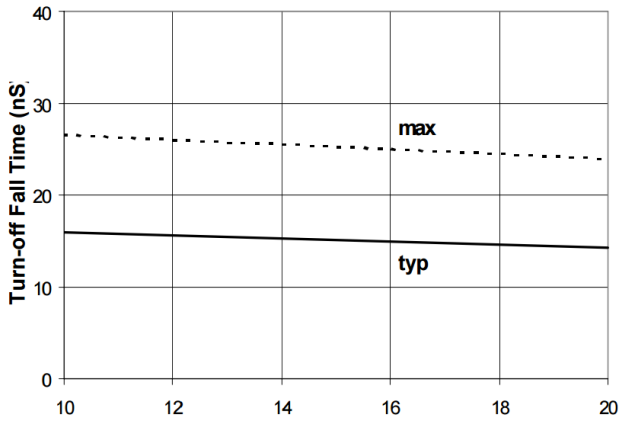


Figure 11B. Turn-Off Fall Time vs. V_{BIAS} (V_{CC}=V_{BS}=V_{DD}) Voltage

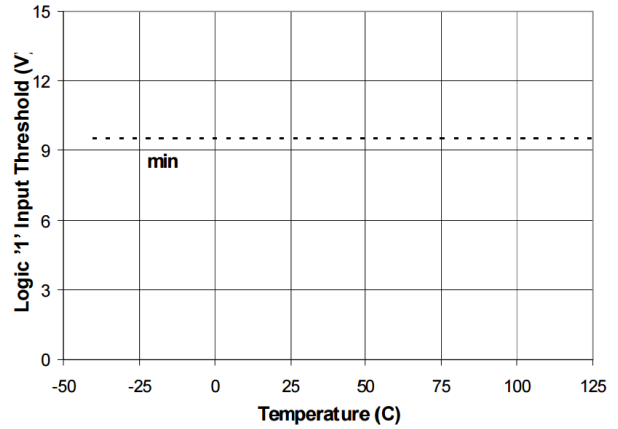


Figure 12A. Logic "1" Input Threshold vs. Temperature

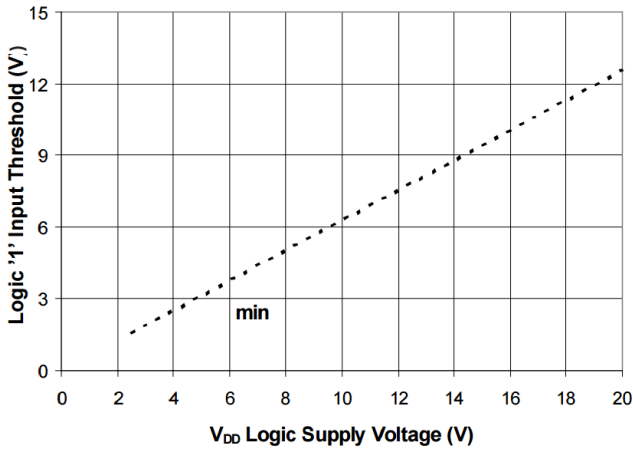


Figure 12B. Logic "1" Input Threshold vs. V_{DD} Voltage

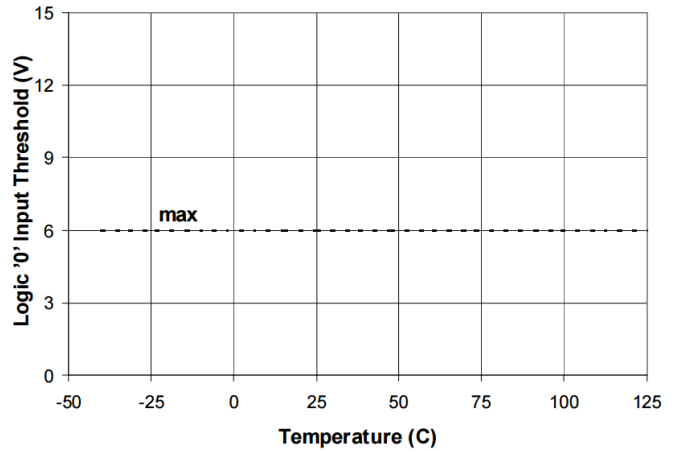


Figure 13A. Logic "0" Input Threshold vs. Temperature

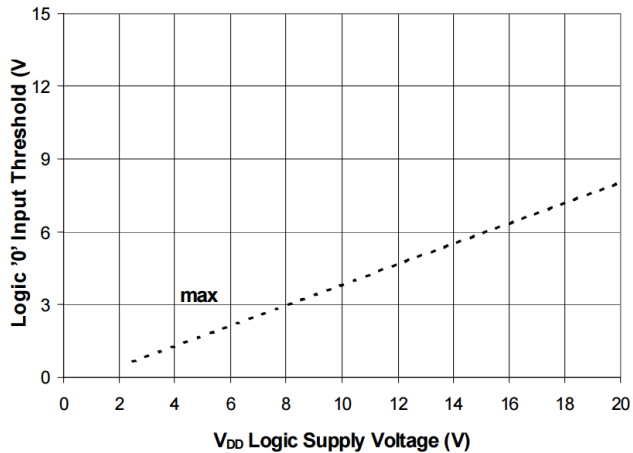


Figure 13B. Logic "0" Input Threshold vs. V_{DD} Voltage

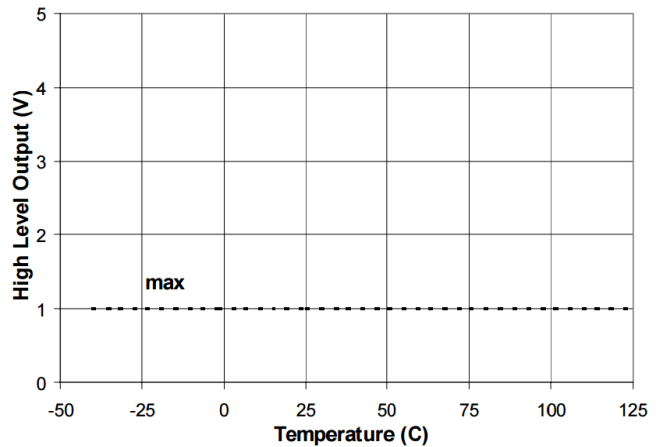


Figure 14A. High Level Output vs. Temperature

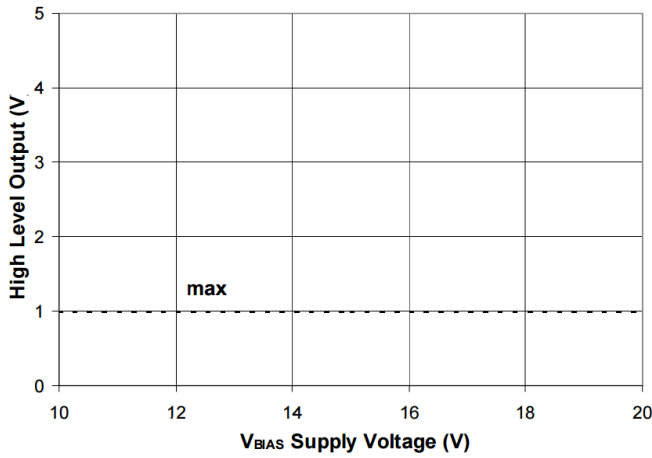


Figure 14B. High Level Output vs. V_{BIAS} Voltage

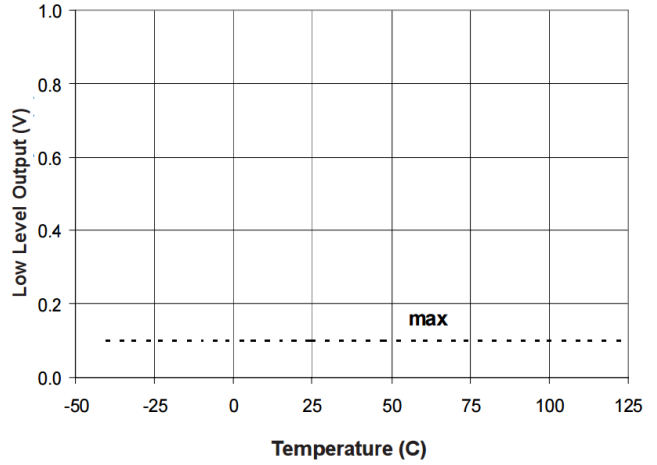


Figure 15A. Low Level Output vs. Temperature

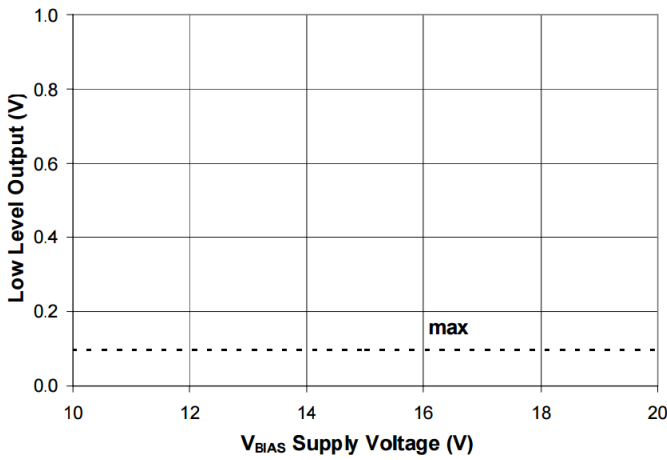


Figure 15B. Low Level Output vs. V_{BIAS} Voltage

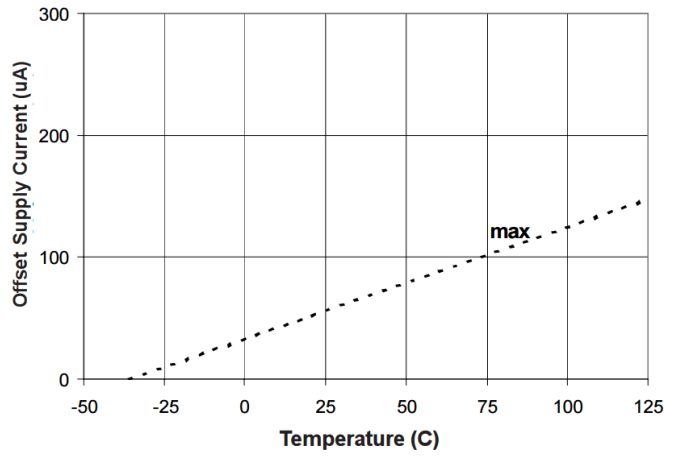


Figure 16A. Offset Supply Current vs. Temperature

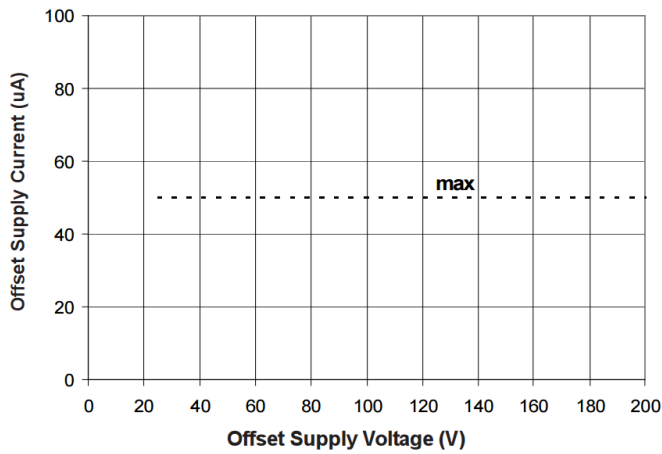


Figure 16B. Offset Supply Current vs. Offset Voltage

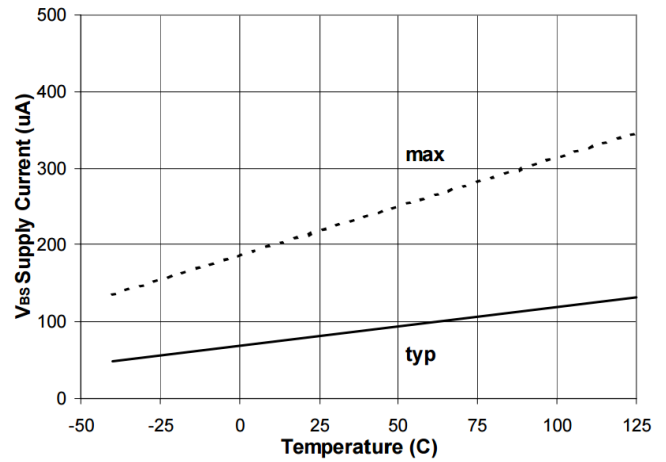


Figure 17A. V_{BS} Supply Current vs. Temperature

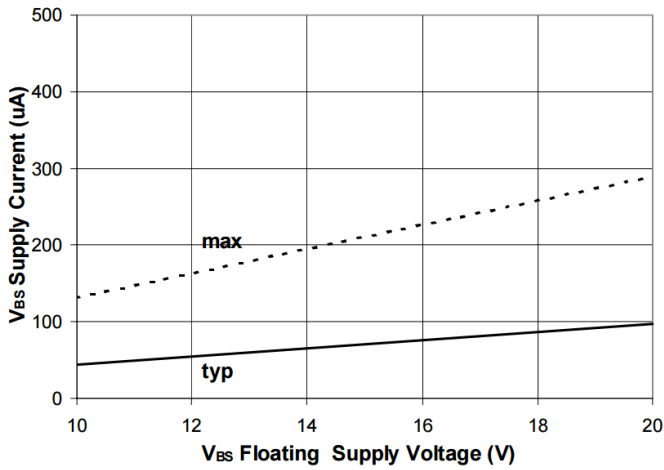


Figure 17B. V_{BS} Supply Current vs. V_{BS} Voltage

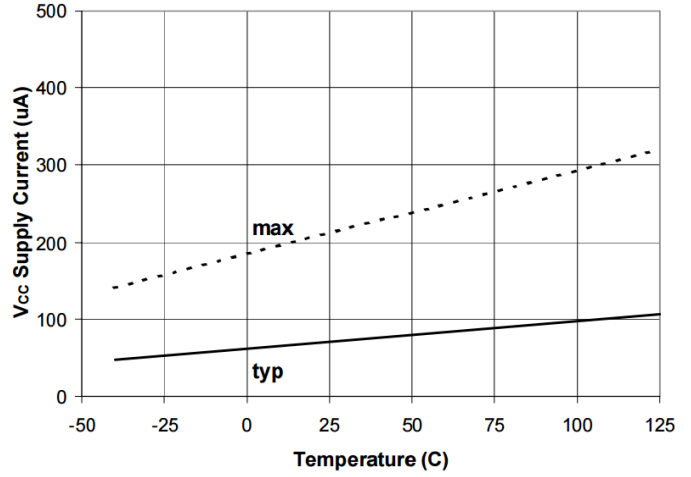


Figure 18A. V_{CC} Supply Current vs. Temperature

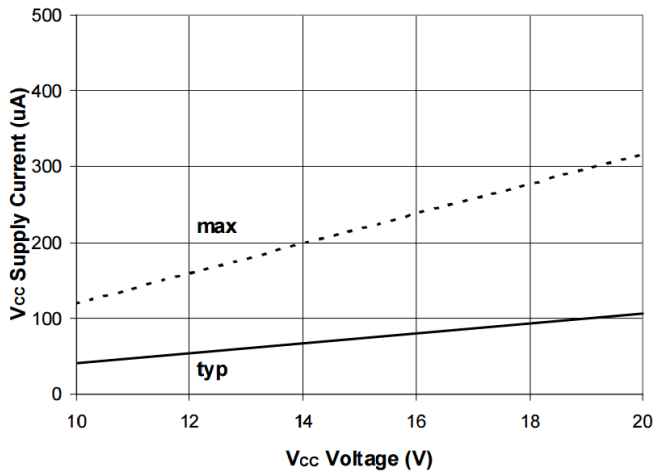


Figure 18B. V_{CC} Supply Current vs. V_{CC} Voltage

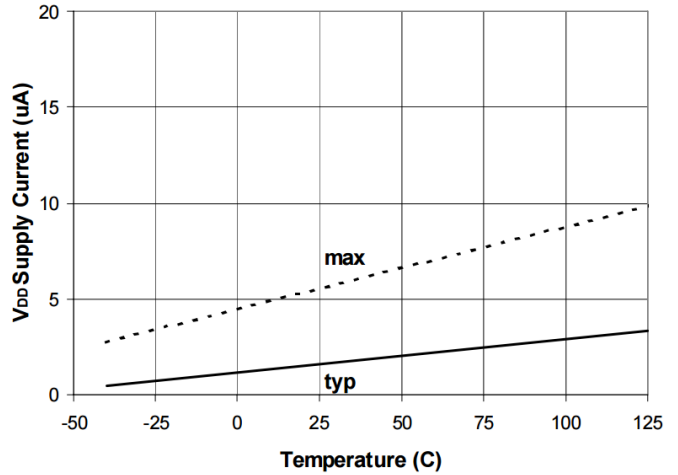


Figure 19A. V_{DD} Supply Current vs. Temperature

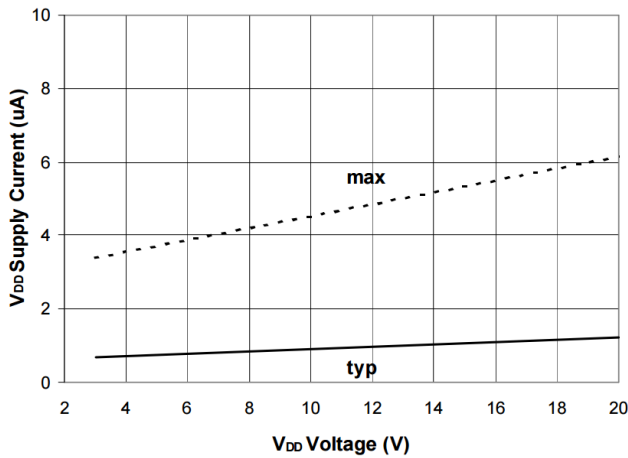


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

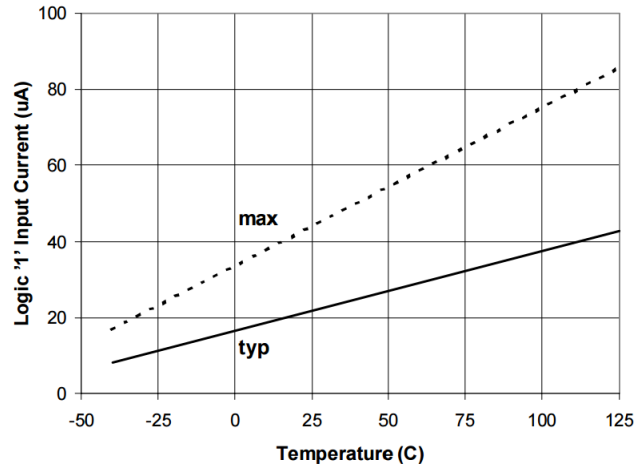


Figure 20A. Logic "1" Input Current vs. Temperature

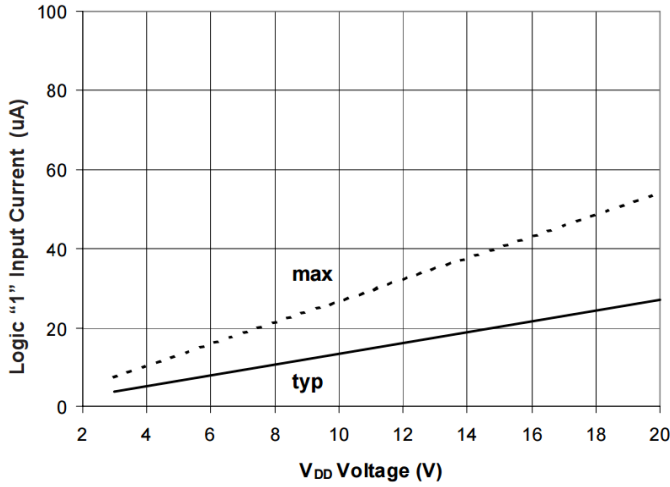


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

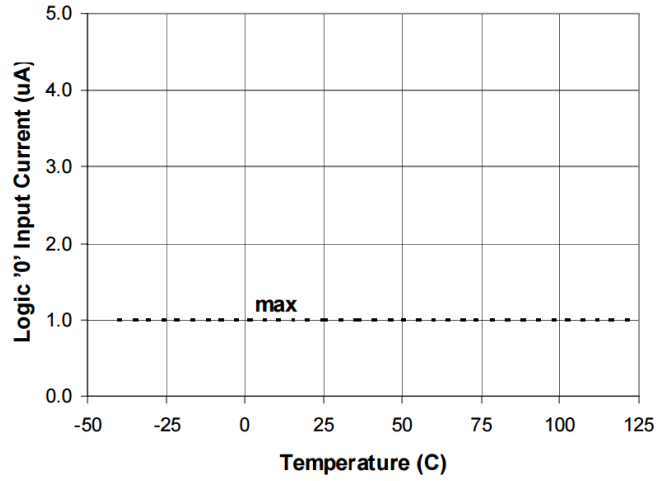


Figure 21A. Logic "0" Input Current vs. Temperature

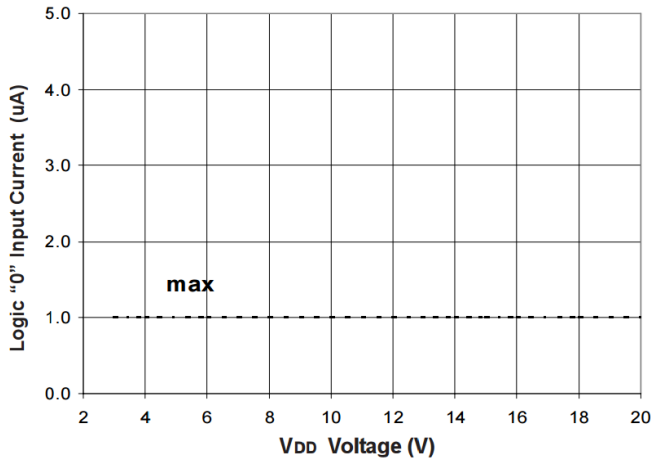


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

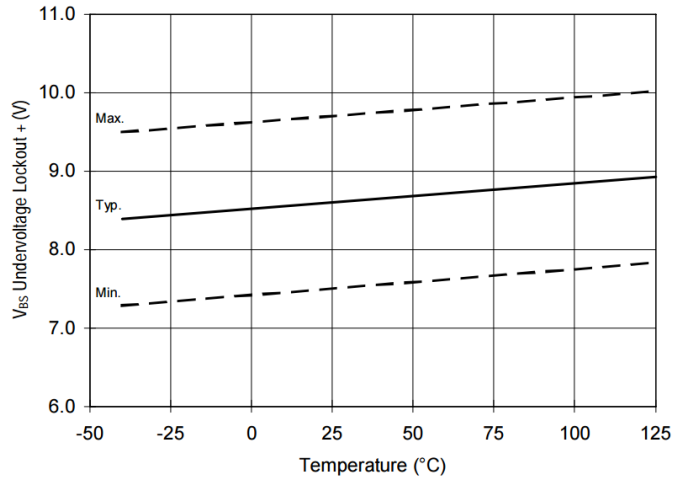


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

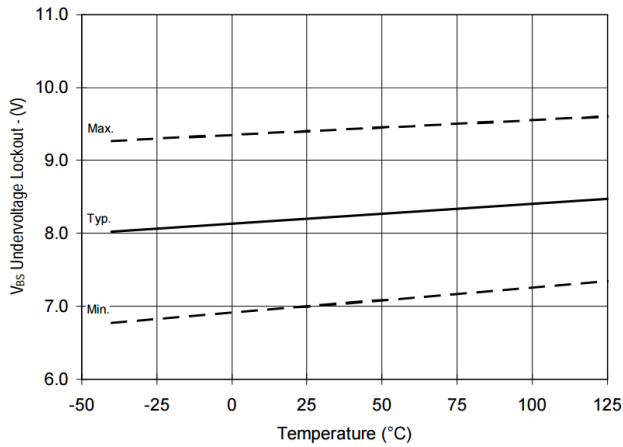


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

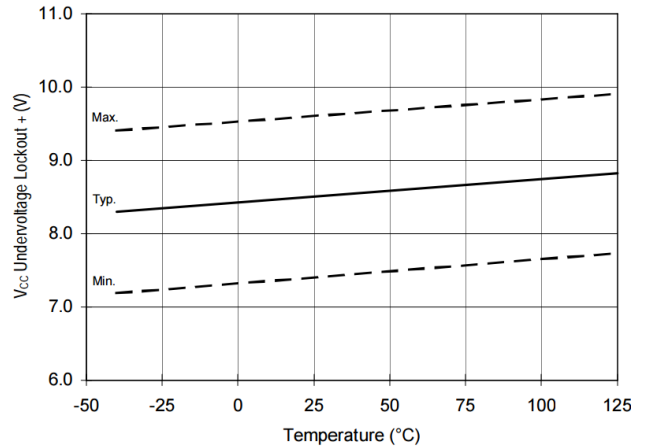


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

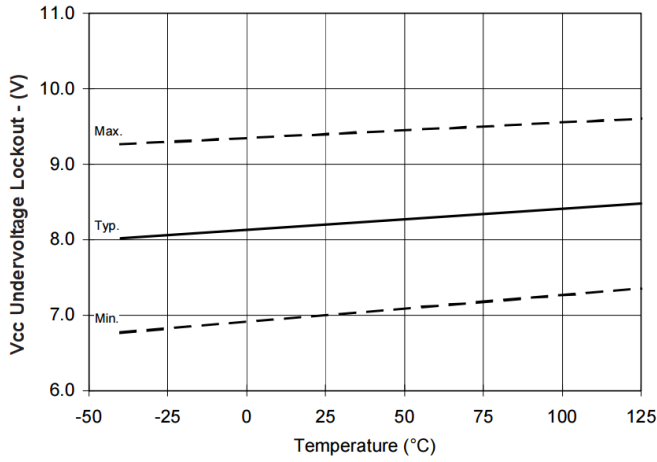


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

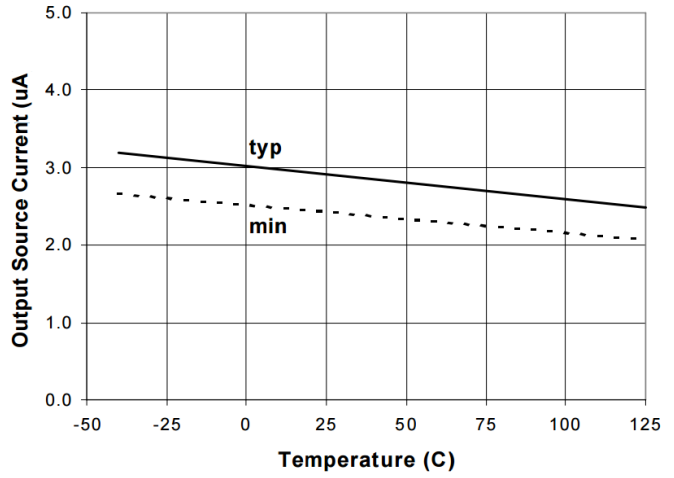


Figure 26A. Output Source Current vs. Temperature

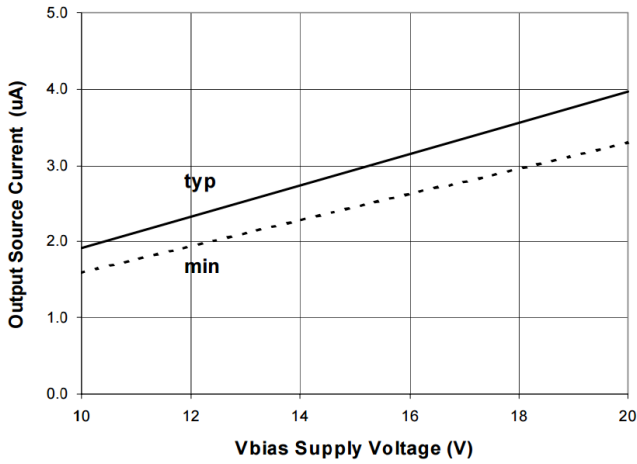


Figure 26B. Output Source Current vs. V_{BIAS} Voltage

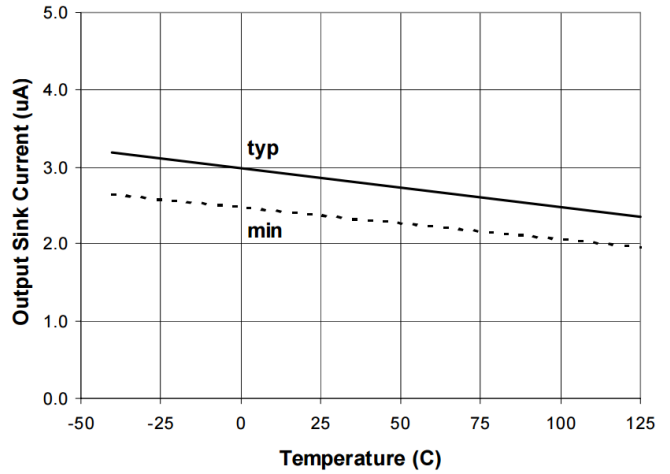


Figure 27A. Output Sink Current vs. Temperature

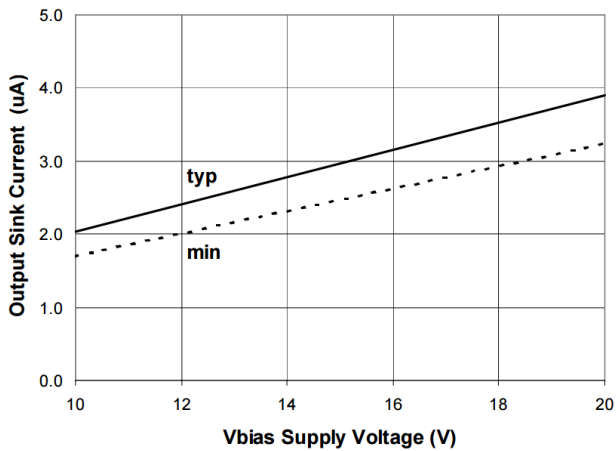


Figure 27B. Output Sink Current vs. V_{BIAS} Voltage

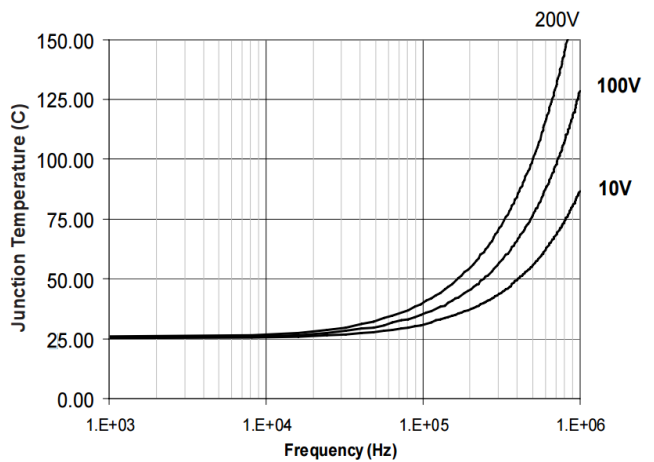


Figure 28. IR2010 T_j vs. Frequency
R_{GATE} = 10Ω, V_{CC} = 15V with IRFPE50

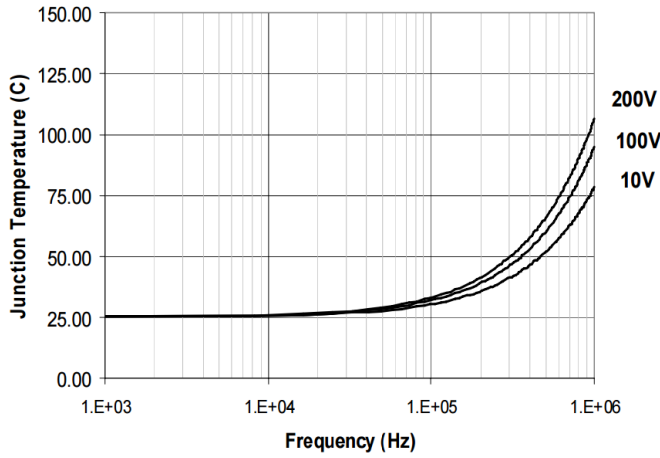


Figure 29. IR2010 Tj vs. Frequency
 $R_{GATE} = 16\Omega$, $V_{CC} = 15V$ with IRFBC40

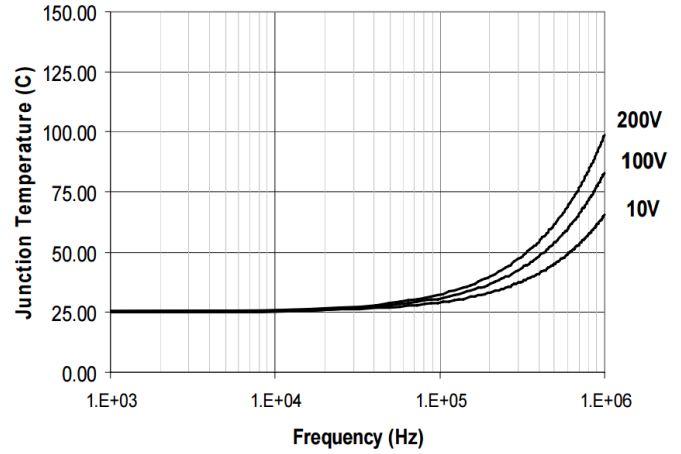


Figure 30. IR2010 Tj vs. Frequency
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$ with IRFBC30

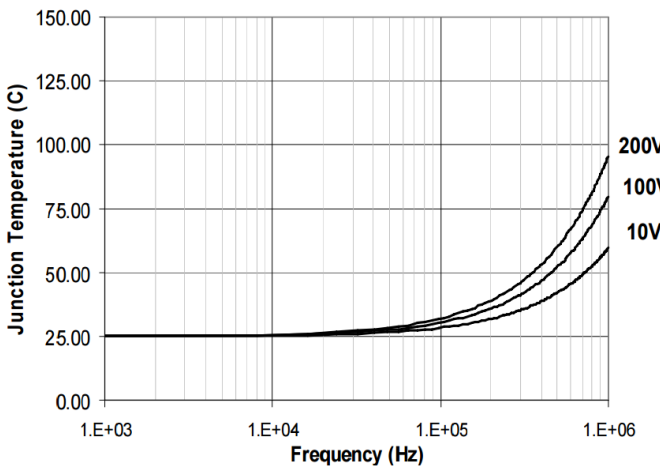


Figure 31. IR2010 Tj vs. Frequency
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$ with IRFBC20

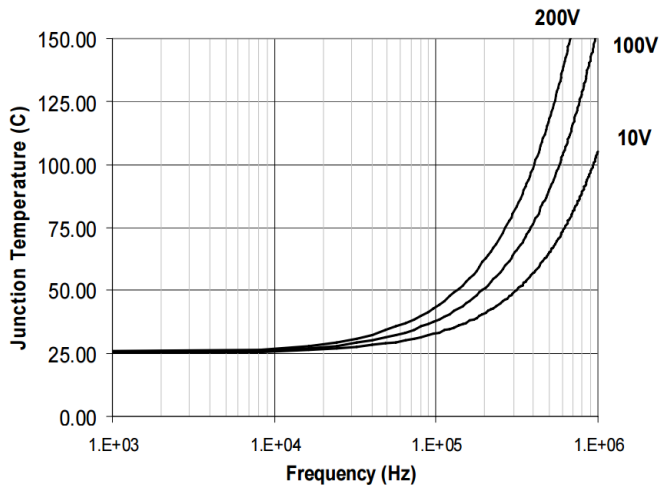


Figure 32. IR2010 Tj vs. Frequency
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$ with IRFBE50

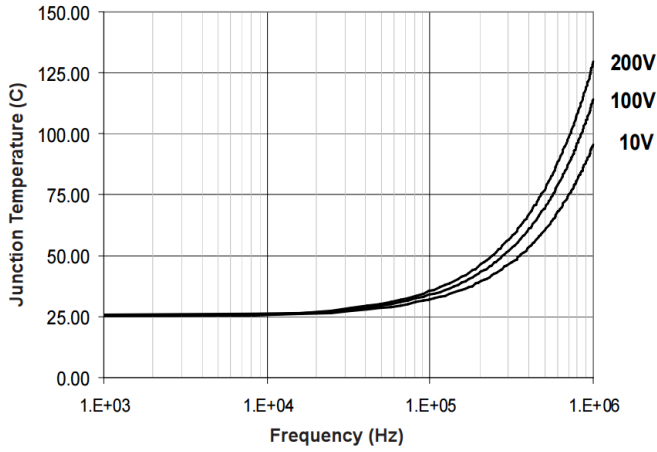


Figure 33. IR2010S Tj vs. Frequency
 $R_{GATE} = 16\Omega$, $V_{CC} = 15V$ with IRFBC40

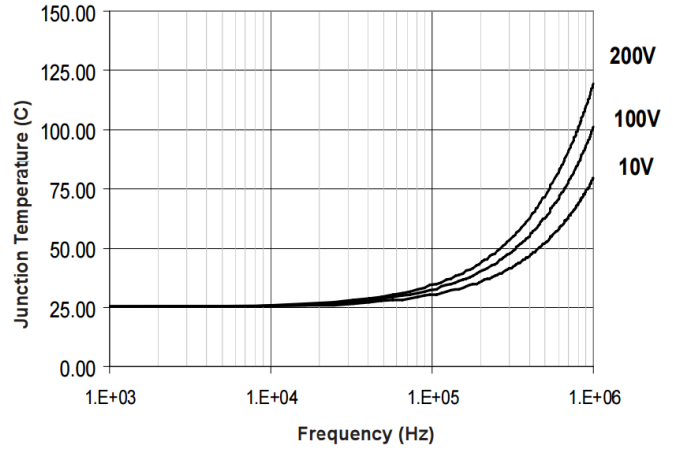


Figure 34. IR2010S Tj vs. Frequency
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$ with IRFBC30

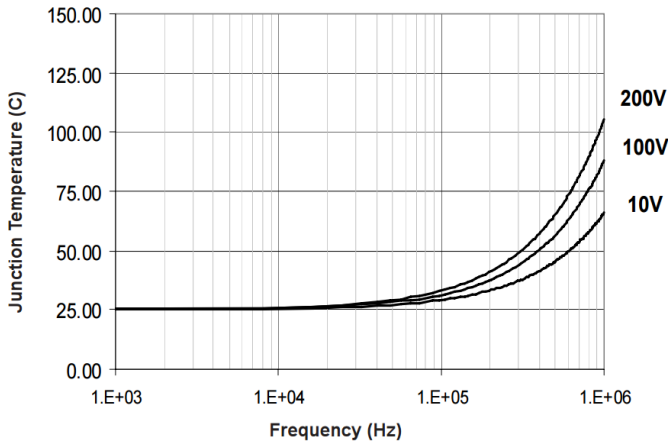
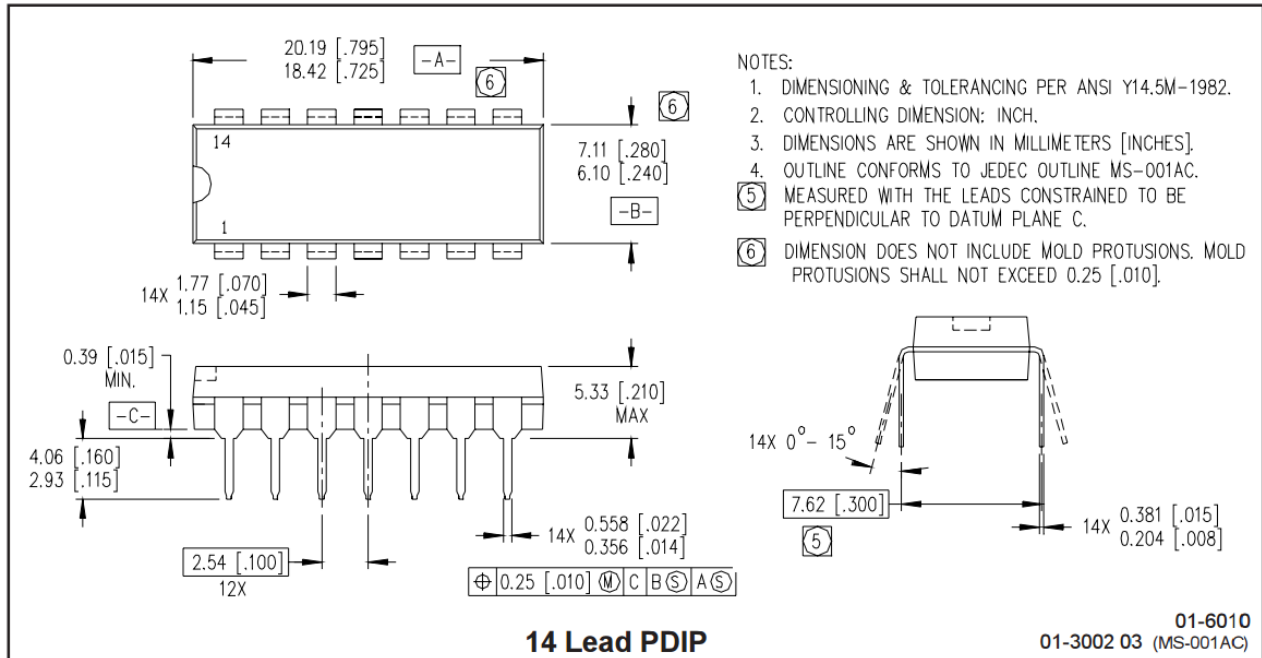
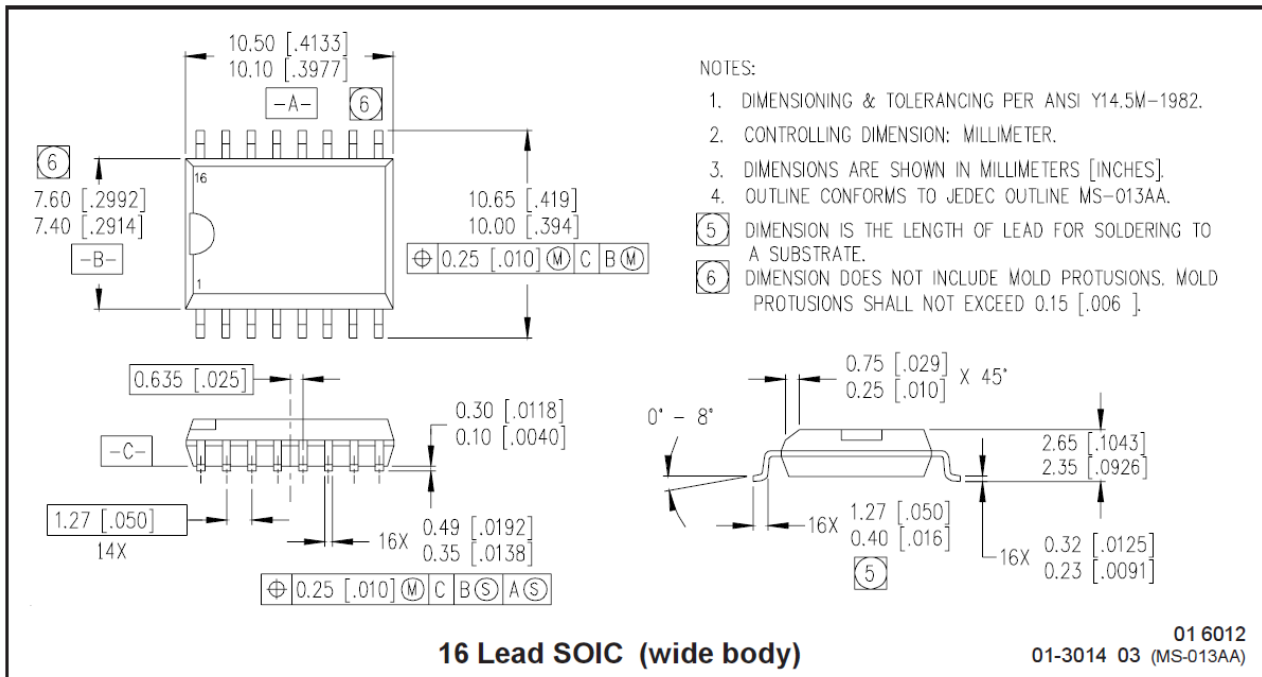


Figure 35. IR2010S Tj vs. Frequency
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$ with IRFBC20

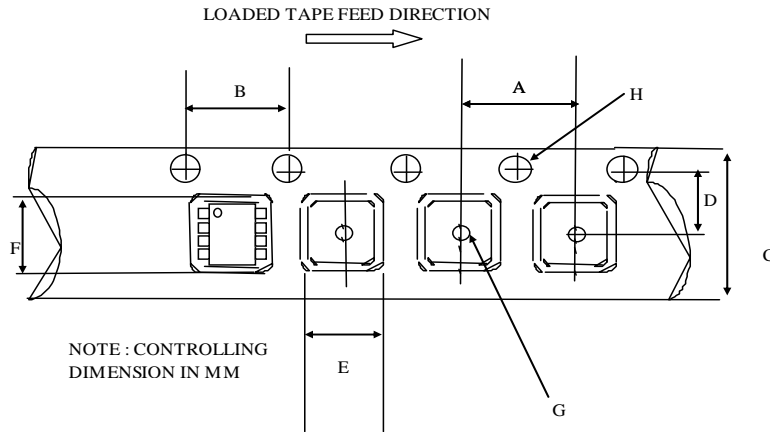
Package Details


- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
 5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
 6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



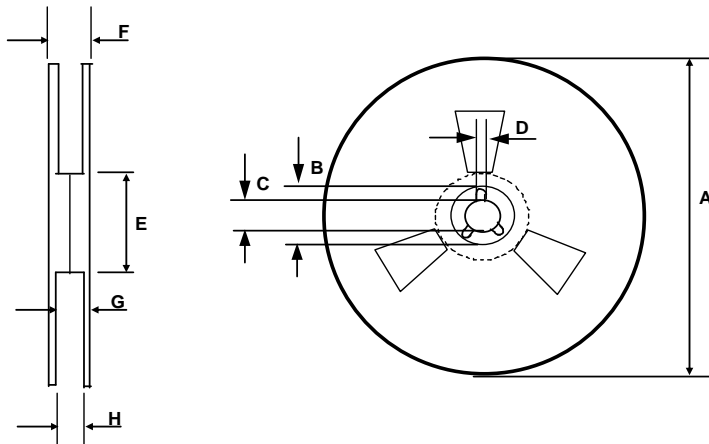
- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
 5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
 6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

Tape and Reel Details



CARRIER TAPE DIMENSION FOR 16SOICW

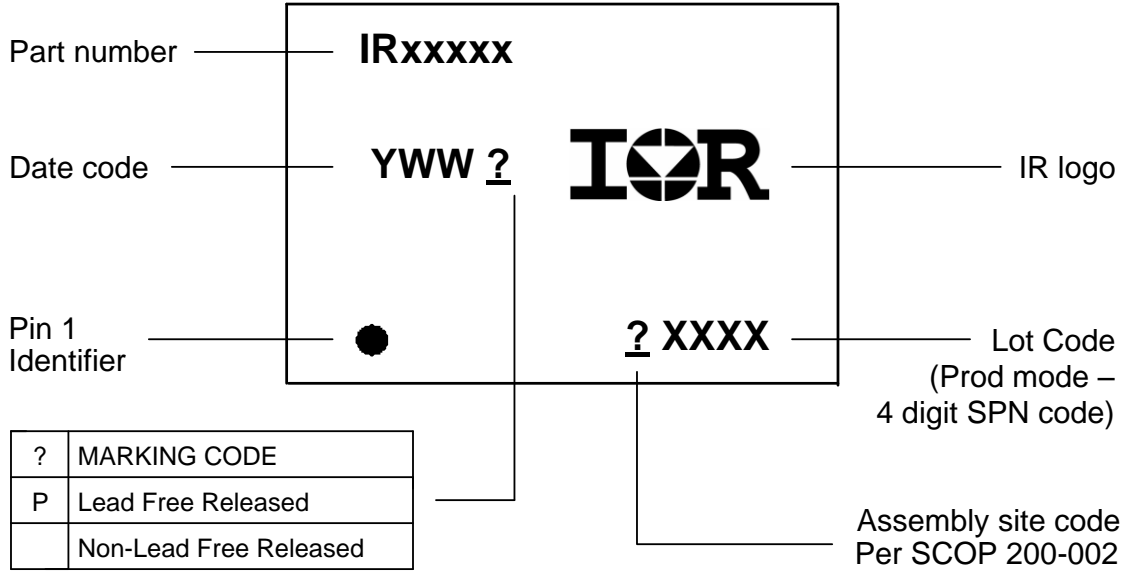
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



Qualification Information[†]

Qualification Level		Industrial ^{††} (per JEDEC JESD 47)
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level	16-Lead SOIC WB	MSL3 ^{†††} (per IPC/JEDEC J-STD-020)
RoHS Compliant		Yes

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

The information provided in this document is believed to be accurate and reliable. However, International Rectifier assumes no responsibility for the consequences of the use of this information. International Rectifier assumes no responsibility for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of International Rectifier. The specifications mentioned in this document are subject to change without notice. This document supersedes and replaces all information previously supplied.

For technical support, please contact IR's Technical Assistance Center
<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:
 233 Kansas St., El Segundo, California 90245
 Tel: (310) 252-7105