ASSP
Dual Serial Input
PLL Frequency Synthesizer

MB15U36

➢ DESCRIPTION

The Fujitsu MB15U36 is a serial input Phase Locked Loop (PLL) frequency synthesizer with 2.0GHz and 1.2GHz prescalers. A 64/65 or a 128/129 for the 2.0GHz prescaler, and a 64/65 or a 128/129 for the 1.2GHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 9.0mA typ. at a supply voltage of 5.0V. MB15U36 utilizes a refined charge pump design (Fujitsu's Super Charger) that provides fast tuning along with low noise performance.

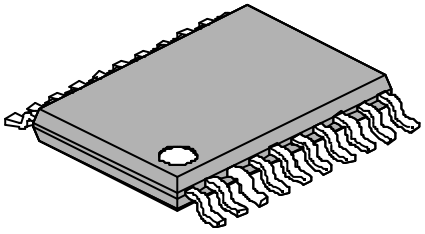
MB15U36 is ideally suitable for digital mobile communications, such as CATV, PHS(Personal Handy Phone System), and PCS(Personal Communication Service).

➢ FEATURE

-High frequency operation : RF synthesizer: 2.0GHz max.
IF synthesizer: 1.2GHz max.
-Power supply voltage : Vcc=3.0 V to 5.5V
-Very low power supply current : Icc=9.0mA typ. (Vcc=5.0V)
-Power saving function : Ips1=Ips2=10uA max.
-Serial input 15 bit programmable reference divider : R=3 to 32,767
-Serial input 18 bit programmable divider consisting of
Binary 7 bit swallow counter : 0 to 127
Binary 11 bit programmable counter : 3 to 2,047
-On-chip high performance charge pump circuit and phase comparator achieved high speed settling time and low phase noise.
-Wide operating temperature : Ta = -40 to +85 °C
-Plastic 20 pin TSSOP package

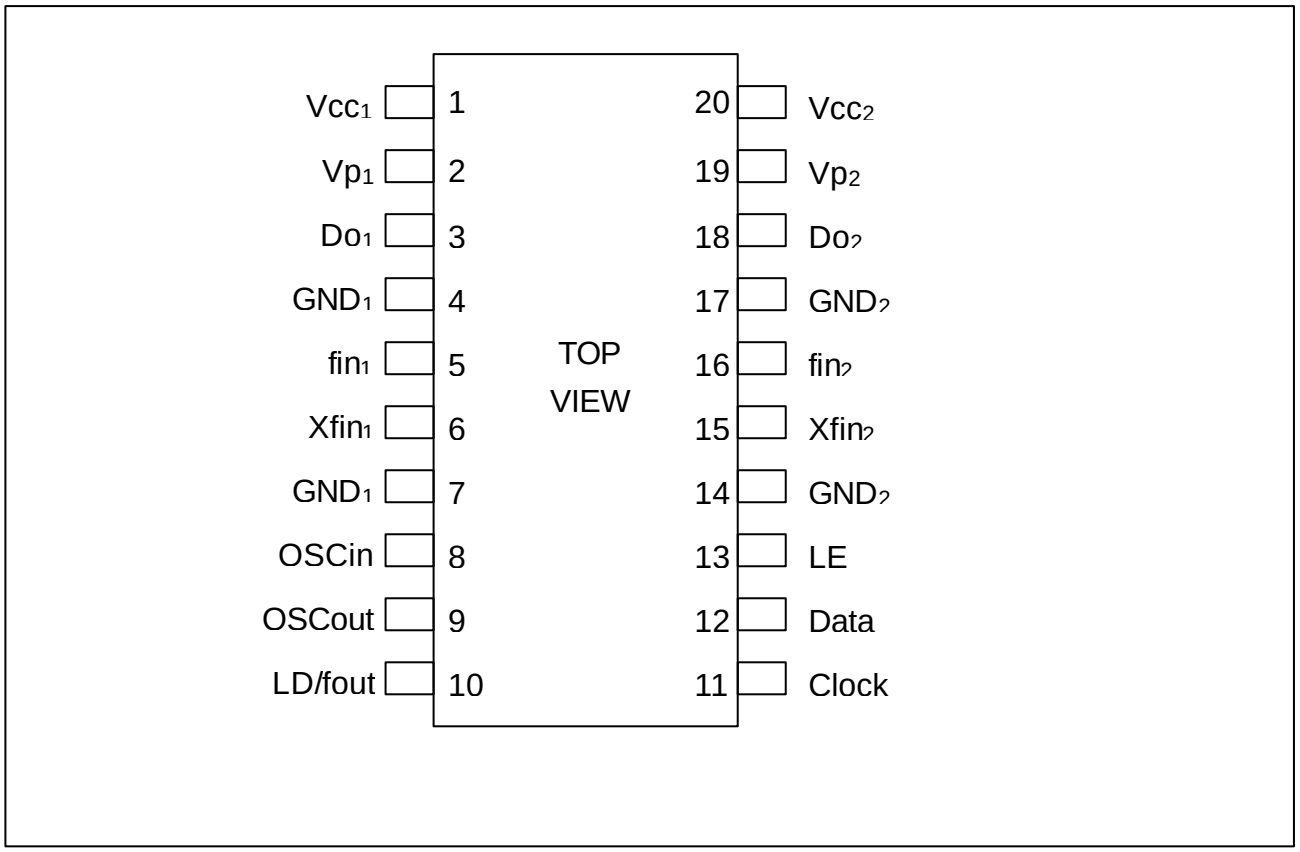
➢ PACKAGE

20-pinPlastic SSOP



FPT-20P-M03

➢ PIN ASSIGNMENT



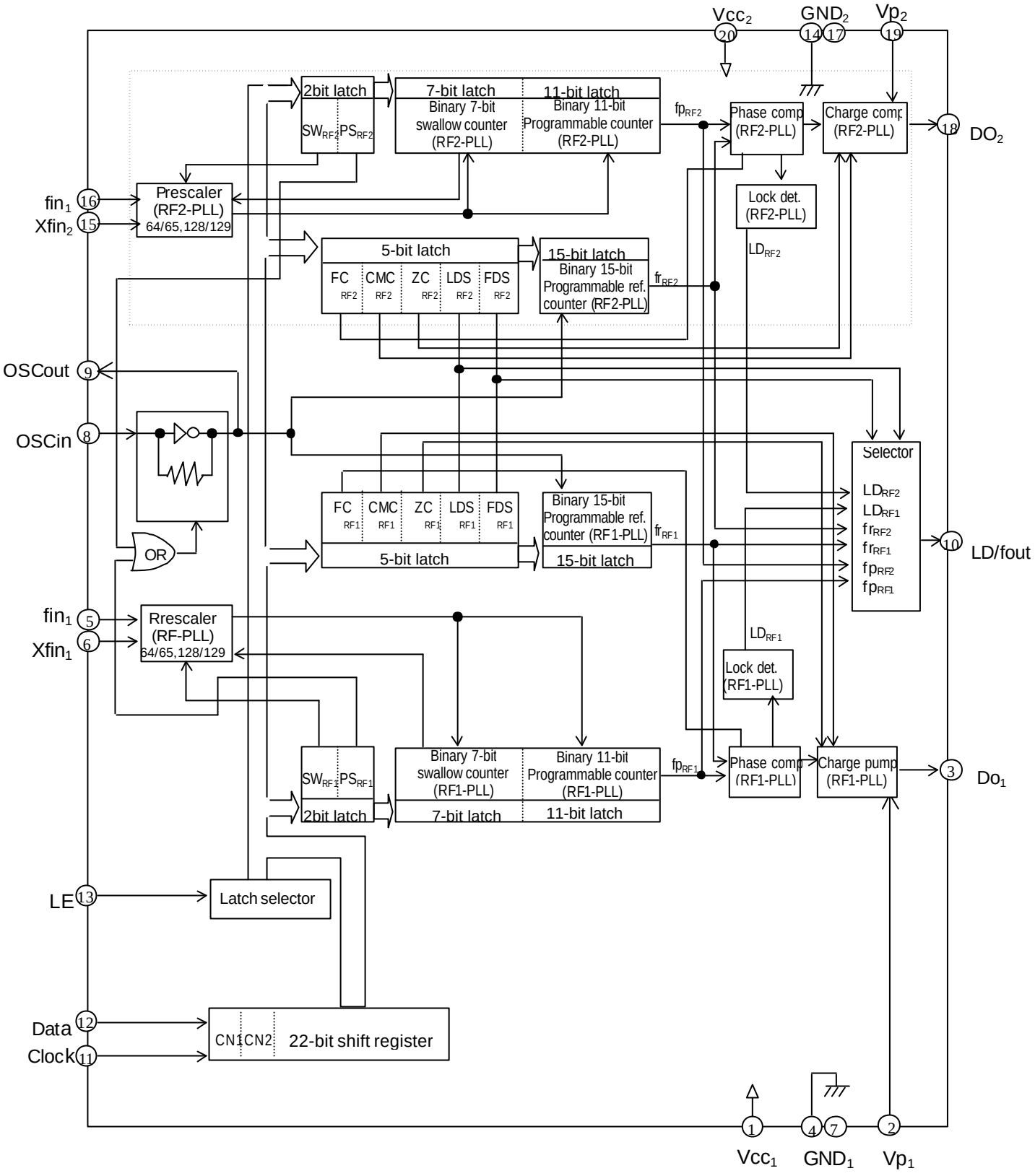
➢ PIN DESCRIPTIONS

Pin No	Pin name	I/O	Descriptions
1	Vcc_1	-	Power supply voltage input pin for the RF1-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF1-PLL is cancelled.
2	Vp_1	-	Power supply for RF1 charge pump.(Independent of 19 pin)
3	Do_1	O	Charge pump output for the RF1-PLL section. Phase detector characteristics can be reversed using the FC bit.
4	GND_1	-	Ground for the RF1-PLL section.
5	fin_1	I	Prescaler input pin for the RF1-PLL section. Connection to an external VCO should be via AC coupling.
6	$Xfin_1$	I	Prescaler complimentary input for the RF1-PLL. Section. This pin should be grounded via a capacitor.
7	GND_1	-	Ground for the RF1-PLL section.
8	OSCin	I	The programmable reference divider input. External TCXO reference oscillator input or connection to crystal. TCXO should be connected with via AC coupling.
9	OSCout	-	Oscillator output or connection to crystal.
10	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout). The output signal is selected by the LDS and FDS bits in the serial data.
11	Clock	I	Clock input for the 22 bit shift register. One bit data is shifted into the shift register on a rising edge of the clock.
12	Data	I	Serial data input. Data is transferred to the corresponding latch (RF1-ref counter, RF1-prog counter, RF2-ref counter, RF2-prog counter according to the control bits setting in the serial programming data.
13	LE	I	Load enable signal input. When LE is “H”, data in the shift register is transferred to the corresponding latch according to the control bits in the serial programming data.
14	GND_2	-	Ground for the RF2-PLL section.
15	$Xfin_2$	I	Prescaler complimentary input for the RF2-PLL section. This pin should be grounded via a capacitor.
16	fin_2	I	Prescaler input pin for the RF2-PLL section. Connection to an external VCO should be via AC coupling.
17	GND_2	-	Ground for the RF2-PLL section.
18	Do_2	O	Charge pump output for the RF2-PLL section. Phase detector characteristics can be reserved using FC bit.
19	Vp_2	-	Power supply voltage for the RF2 charge pump.(Independent of 2 pin)
20	Vcc_2	-	Power supply voltage input pin for the RF2-PLL section. When power is OFF, latched data of IF-PLL is cancelled.

MB15U36

➢ BLOCK DIAGRAM

PKG:TSSOP-20(FPT-20-M03)



➢ ABSOLUTE MAXIMUM

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	Vcc	-0.5 to 6.5	V	
	Vp	-0.5 to 6.5	V	
Input voltage	Vi	-0.5 to 6.5	V	
Output voltage	Vo	-0.5 to 6.5	V	
Storage temperature	T_{STG}	-55 to +125	°C	

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

➢ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	Vcc	4.5	5.0	5.5	V	Vcc_1=Vcc_2
		3.0	5.5	5.5	V	Vcc_1=Vcc_2 *1
	Vp	Vcc	-	5.5	V	
Input voltage	Vi	GND	-	Vcc	V	
Operating temperature	Ta	-40	-	+85	°C	

*1:Prescaler divide ratio is only 64/65 (SW="L") at RF1

Handling Precautions

-This device should be transported and stored in anti-static containers.

-This is a static-sensitive device ; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.

-Always turn the power supply off before inserting or removing the device from its socket.

-Protect leads with a conductive sheet when handling or transporting PC boards with devices

➢ ELECTRICAL CHARACTERISITCS

Parameter		Symbol	Condition		Value			Unit
Power supply current		I_{CC1}*1	fin1=2000MHz fosc=12MHz	Vcc=5.0V	–	6.0	–	mA
				Vcc=3.0V	–	3.5	–	mA
		I_{CC2}*2	fin2=1200MHz fosc=12MHz	Vcc=5.0V	–	3.0	–	mA
				Vcc=3.0V	–	2.5	–	mA
Power saving current		I_{PS1}	V_{CC1} current at PS bit RF1/RF2="H"		–	0.1*3	10	uA
		I_{PS2}	V_{CC2} current at PS bit RF2="H"		–	0.1*3	10	uA
Operating frequency		f_{in1}*4	RF1-PLL		100	–	2000	MHz
		f_{in2}*4	RF2-PLL		50	–	1200	MHz
		fosc	Min. 500mVpp		3	–	40	MHz
Input sensitivity		P_{fin1}	RF1-PLL, 50Ω termination		-10	–	+2	dBm
			RF1-PLL, Vcc=3.5V 300MHz≤fin≤1000MHz 50Ω termination		-18	–	+2	dBm
		P_{fin2}	RF2-PLL, 50Ω termination		-10	–	+2	dBm
		Vosc			500	–	Vcc	mVp-p
Input voltage	Data, Clock LE	V_{IH}			Vcc×0.8	–	–	V
		V_{IL}			–	–	Vcc×0.2	V
Input current	Data, Clock LE	I_{IH}*5	V_{IH}=Vcc		-1.0	–	+1.0	uA
		I_{IL}*5	V_{IH}=0Vcc		-1.0	–	+1.0	uA
	OSCin	I_{IH}	V_{IH}=Vcc		0	–	+100	uA
		I_{IL}*5	V_{IH}=0Vcc		-100	–	0	uA
Output voltage	LD/fout	V_{OH}	I_{OH}=-1mA		Vcc-0.4	–	–	V
		V_{OL}	I_{OL}=1mA		–	–	0.4	V
	Do1 Do2	V_{DOH}	I_{DOH}=-0.5mA		Vp-0.4	–	–	nA
		V_{DOL}	I_{DOL}=0.5mA		–	–	0.4	mA
High impedance cutoff current	Do1 Do2	I_{OFF}	Vcc=Vp=5.0V 0.5V≤V_{DO}≤Vp-0.5V		–	–	3.0	nA
Output current	LD/fout	I_{OH}*5	Vcc=5.0V		–	–	-1.0	mA
		I_{OL}	Vcc=5.0V		+1.0	–	–	mA

➢ ELECTRICAL CHARACTERISITCS (Continued)

Parameter		Symbol	Condition	Value			Unit
				MIN	TYP	MAX	
Output current	D_{O1} D_{O2}	I_{DOH}*5	Vcc=Vp=5.0V, V_{DOH}=Vp/2 CMCbit="L", Ta=25°C	–	-1.25	–	mA
			Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="L", Ta=25°C	–	-1.00	–	mA
		I_{DOL}	Vcc=Vp=5.0V, V_{DOL}=Vp/2 CMCbit="L", Ta=25°C	–	1.25	–	mA
			Vcc=Vp=3.0V, V_{DOL}=Vp/2 CMCbit="L", Ta=25°C	–	1.00	–	mA
		I_{DOH}*5	Vcc=Vp=5.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	-5.00	–	mA
			Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	-4.00	–	mA
		I_{DOL}	Vcc=Vp=5.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	5.00	–	mA
			Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	4.00	–	mA
Cp current change ratio	I_{DOL}/I_{DOH}	I_{DOMT}*6	V_{DO}=Vp/2, Ta=25°C	–	3	–	%
	I_{DO} vs V_{DO}	I_{DOVD}*7	0.5V≤V_{DO}≤Vp-0.5V Ta=25°C	–	15	–	%
	I_{DO} vs Ta	I_{DOTA}*8	V_{DO}=Vp/2 -40°C ≤Ta≤+85°C	–	10	–	%

*1: Conditions: V_{CC1}=5.0V, Ta=25°C in locking state

*2: Conditions: V_{CC2}=5.0V, Ta=25°C in locking state

*3: Conditions: Vcc=5.0V, Ta=25°C, fosc=12.8MHz(-2dBm)

*4: AC coupling. The minimum frequency is specified with a connecting coupling capacitor of 1000pF. Please note the harmonics when using at the low frequency(<1/2 max.frequency)

*5: The symbol "-" means direction of current flow.

*6: Conditions: Vcc=Vp=5.0V, Ta=25°C

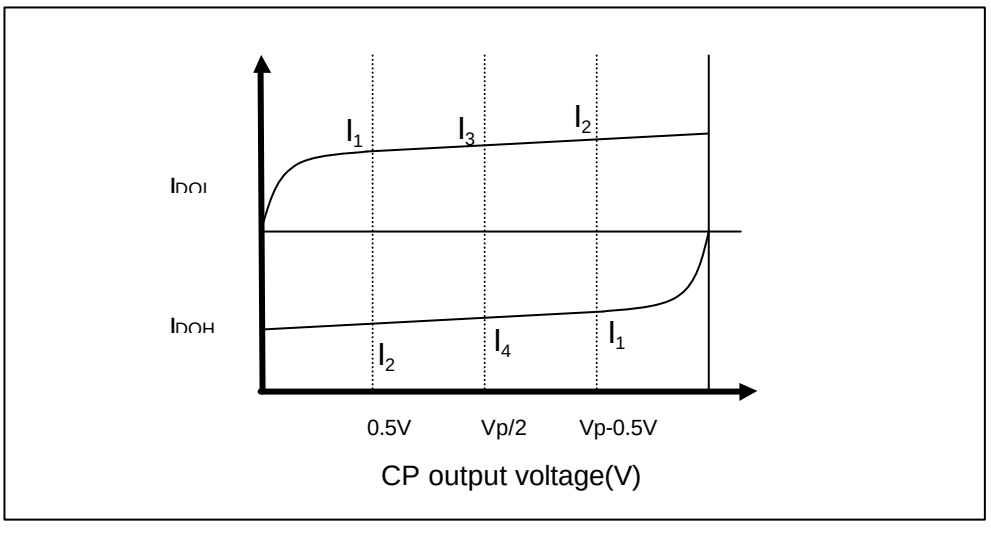
$(|| I_3| - |I_4||)/ [(| I_3| + |I_4|)/2] \times 100\%$

*7: Conditions: Vcc=Vp=5.0V, Ta=25°C

$[(|| I_2| - |I_1||) /2] /[(| I_1| + |I_2|)/2] \times 100\%$ (Applied to each I_{DOL}, I_{DOH})

*8: Conditions: Vcc=Vp=5.0V

$[(|| I_{DO(85°c)}| - |I_{DO(-40°c)}||) /2] /[(| I_{DO(85°c)}| + |I_{DO(-40°c)}|)/2] \times 100\%$(Applied to each I_{DOL}, I_{DOH})



➢ FUNCTIONAL DESCRIPTION

The divide ratio can be calculated using the following equation:
fvco = [(P × N) + A] × fosc / R (A<N)
fvco : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (64 or 128 for RF1-PLL or RF2-PLL)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter (0≤A≤127)
fosc: Output frequency of the reference frequency oscillator
R : Preset divide ratio of binary 15-bit programmable reference counter (3 to 32,767)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of RF1/RF2-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually. Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch them depending upon the control bit data setting.

Table1. control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the RF2-PLL
L	H	The programmable reference counter for the RF1-PLL
H	L	The programmable counter and the swallow counter for the RF2-PLL
H	H	The programmable counter and the swallow counter for the RF1-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	FC	CMC	ZC	LDS	FDS

CN1,2 :Control bit
R1 to R15 :Divide ratio setting bits for the programmable reference counter(3 to 32,767)
FC :Phase control bit for the phase detector
CMC :Charge pump output current control bit
ZC :Forced high-impedance control bit for the charge pump
LDS/FDS :LD/fout signal select bit
Note: Start data input with MSB first

Programmable Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	SW	PS

CN1 :Control bit
N1 to N11 :Divide ratio setting bits for the programmable counter(3 to 2,047)
A1 to A7 :Divide ratio setting bits for the swallow counter(0 to 127)
SW :Divide ratio setting bit for the prescaler
(64/65 or 128/129 for the RF1/RF2-PLL)
PS :Power saving mode control bit
Note: Start data input with MSB first

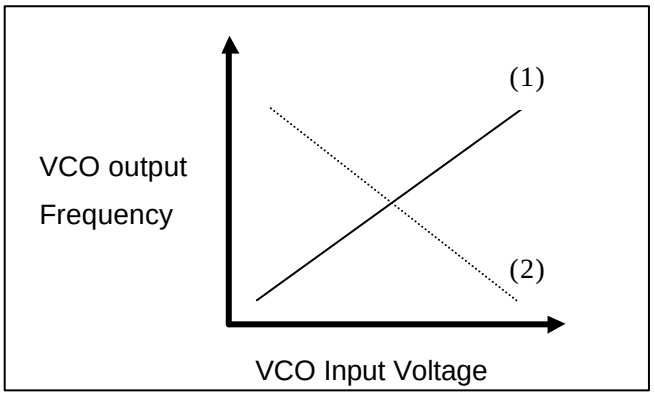
Table.2 Binary 15 bit programmable reference counter data setting

Divide ratio (R)	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less then 3 is prohibited.

Tabale.3 Phase comparator phase switching data setting

	FC="H"	FC="L"
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO polarity	(1)	(2)



NOTE: Z= High impedance

When the LPF and VCO characteristics are similar to (1), set FC bit high

When the VCO characteristics are similar to (2), set FC bit low.

Table.4 Charge pump output current selection

CMC	Charge pump output current
0	1×IDO
1	4×IDO

Table.5 Forced high impedance control for the charge pump

ZC	Charge pump output
0	Normal output
1	High impedance

Table.6 LD/fout output select data setting

LDS_{RF}	LDS_{IF}	RDS_{RF}	RDS_{IF}	LD/fout output signal
0	0	0	0	Disabled
0	1	0	0	LD signal (RF2 lock detect)
1	0	0	0	LD signal (RF1 lock detect)
1	1	0	0	LD signal (RF1/RF2 lock detecy)
×	0	0	1	fout (output fr_{RF2})
×	0	1	0	fout (output fr_{RF1})
×	1	0	1	fout (output fp_{RF2})
×	1	1	0	fout (output fp_{RF1})
0	0	1	1	Fast lock
0	1	1	1	RF2 counter reset
1	0	1	1	RF1 counter reset
1	1	1	1	RF1/RF2 Counter reset

Note : ×=don't care

The Fast lock mode utilizes the LD/fout output pin. While Fast lock mode, whenever RF Charge pump output current select bit(CMC_{RF} bit) is selected "H", LD/fout output pin (open drain output) is "L". When CMCRF bit is selected"L", LD/fout output pin(open drain output) is "Z".(See Fast lock circuit example)

Table.7 Binary 11 bit Programmable counter data setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table.8 Binary 7 bit swallow counter data setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range=0 to 127

Table.9 Prescaler data setting

		SW="L"	SW="H"
Prescaler divide ratio	RF2-PLL	64/65	128/129
	RF1-PLL	64/65	128/129

Table.10 Power saving mode setting(1)

PS_{RF2}	$\overline{PS}_{RF2}$	RF2-PLL counters	RF1-PLL counters	OSC input buffer
H	H	OFF	OFF	OFF
L	H	ON	OFF	ON
H	L	OFF	ON	ON
L	L	ON	ON	ON

Setting a $PS_{RF1/RF2}$ bit to high, RF1-PLL/RF2-PLL enters into power saving mode resultant current consumption can be limited to 10uA max.. Setting PS bit to low, power saving mode is released so that the device works normally. Allow 1us after frequency stabilization on power-up for exiting the power saving mode.(PS: "H" to "L)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10uA per one PLL section.
At that time, the DO become the same state as when a loop is locking. That is, the DO becomes high impedance. A VCO control voltage is naturally kept at the locking voltage which defined by a time constant of LPF. As a result, VCO's frequency is kept at the locking frequency.

Serial data input timing

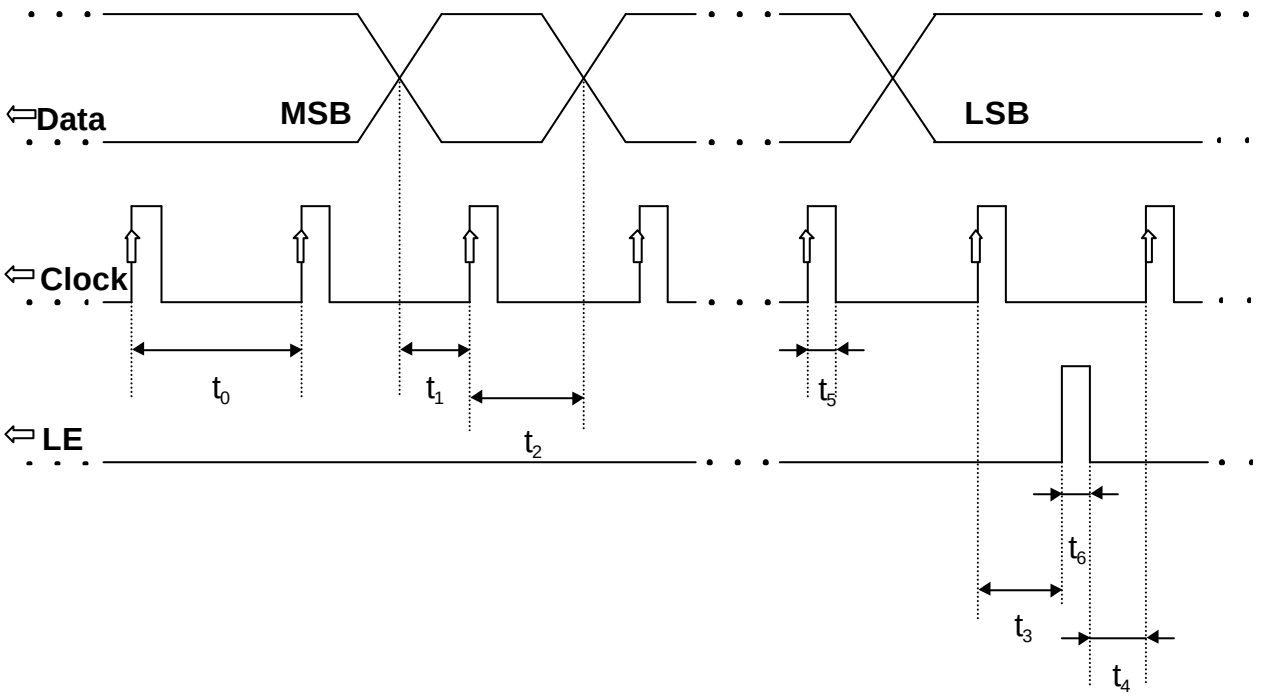
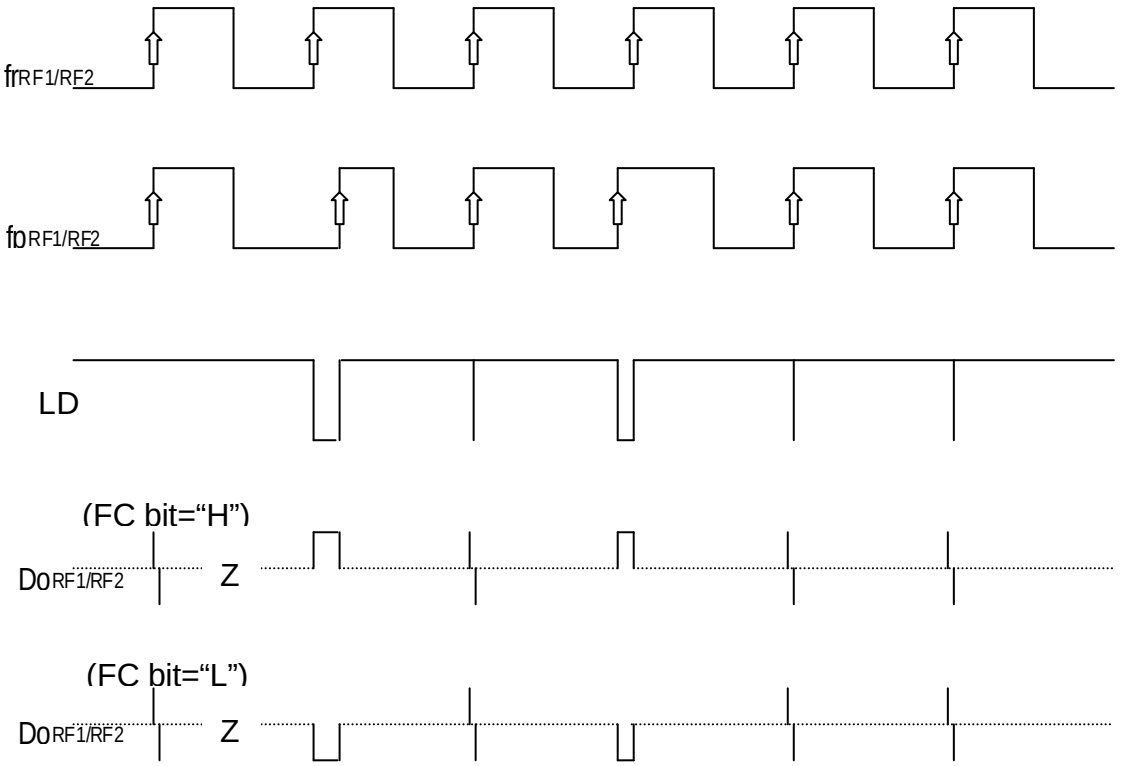


Table11.Timing parameters

Parameter	MIN.	TYP.	MAX.	Unit	Note
t0	100	–	–	ns	CK Rate
t1	20	–	–	ns	tsu CK → Data
t2	20	–	–	ns	th CK → Data
t3	30	–	–	ns	tsu LE
t4	20	–	–	ns	tsu inactive
t5	30	–	–	ns	tw CK
t6	100	–	–	ns	tw LE

On rising edge of the clock, one bit of the data is transferred into the shift register.

➢ Phase detector output waveform

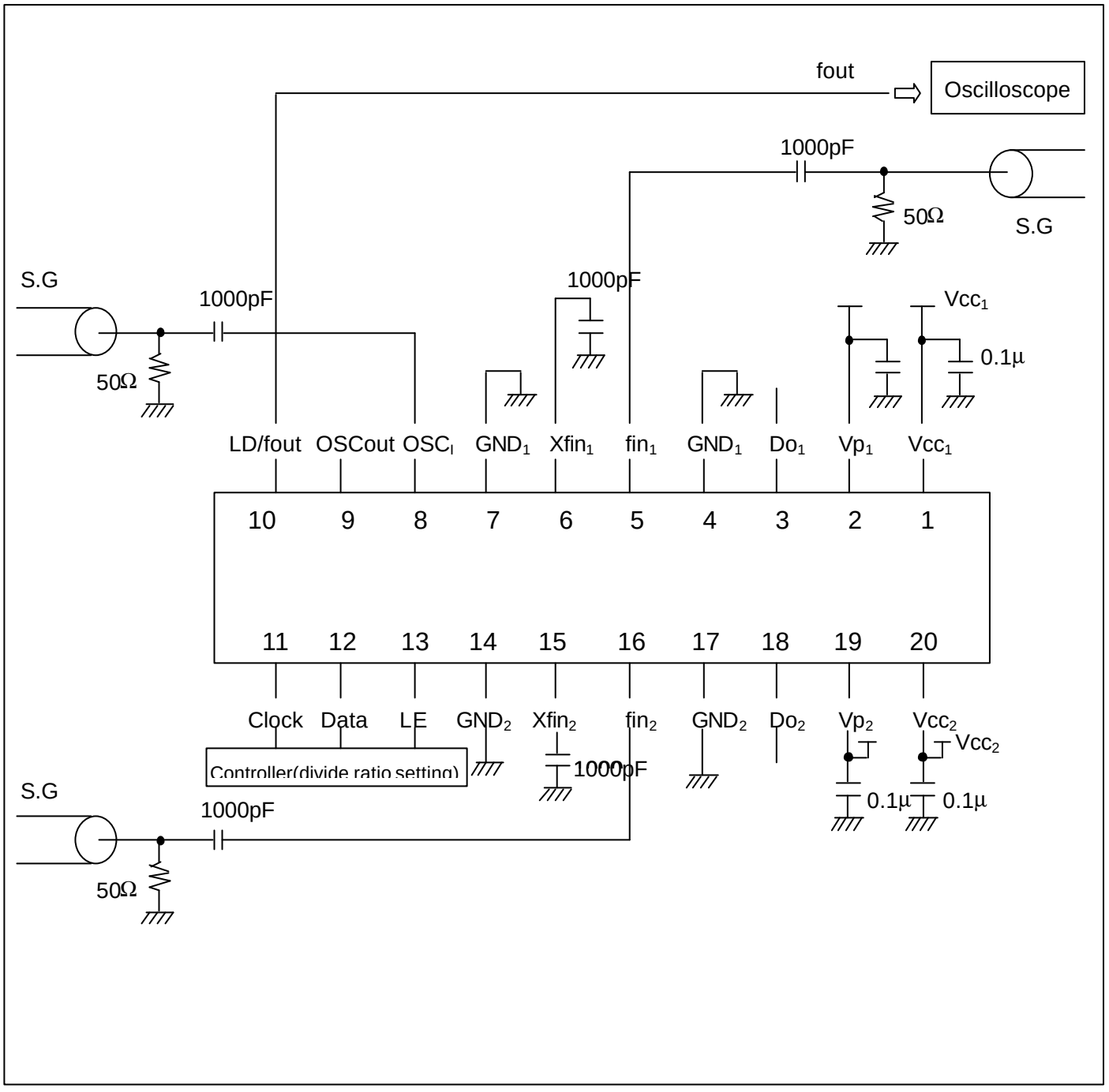


Note: Phase error detection range = -2π to +2π

Pulse on $Do_{RF1/RF2}$ signals are output to prevent dead zone.

MB15U36

➢ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)

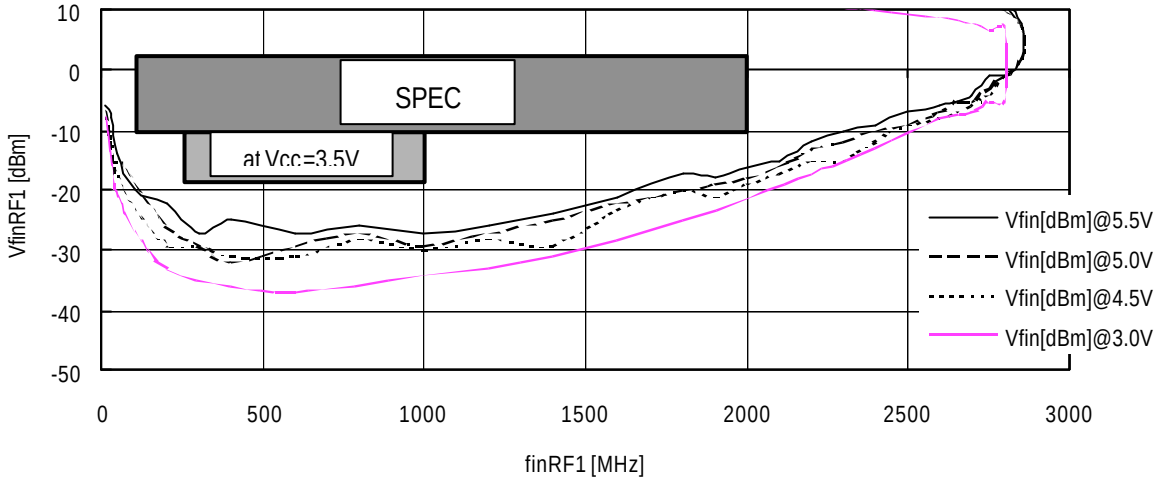


MB15U36

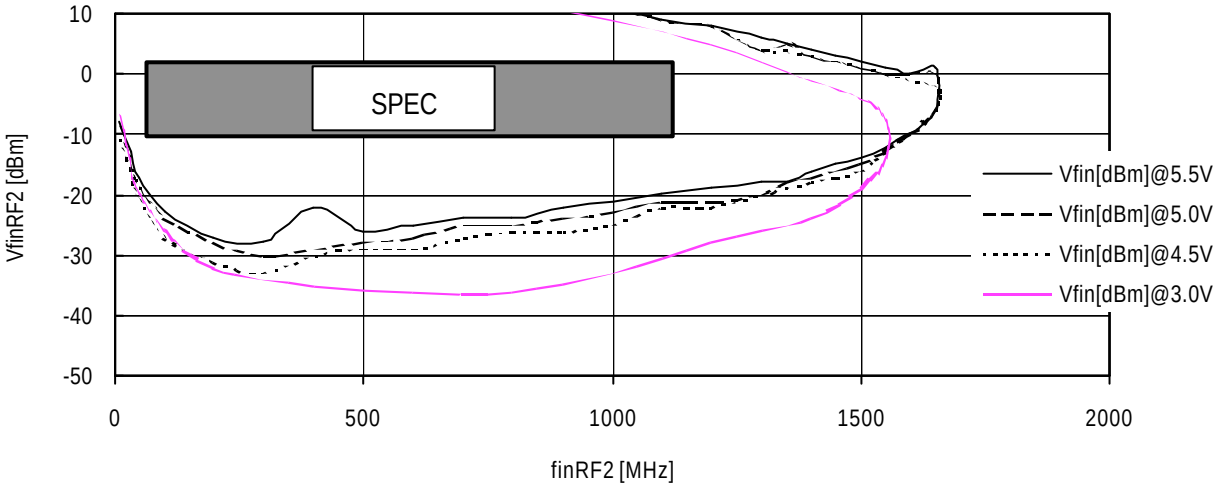
➢ TYPICAL CHARACTERISTICS

1.fin input sensitivity

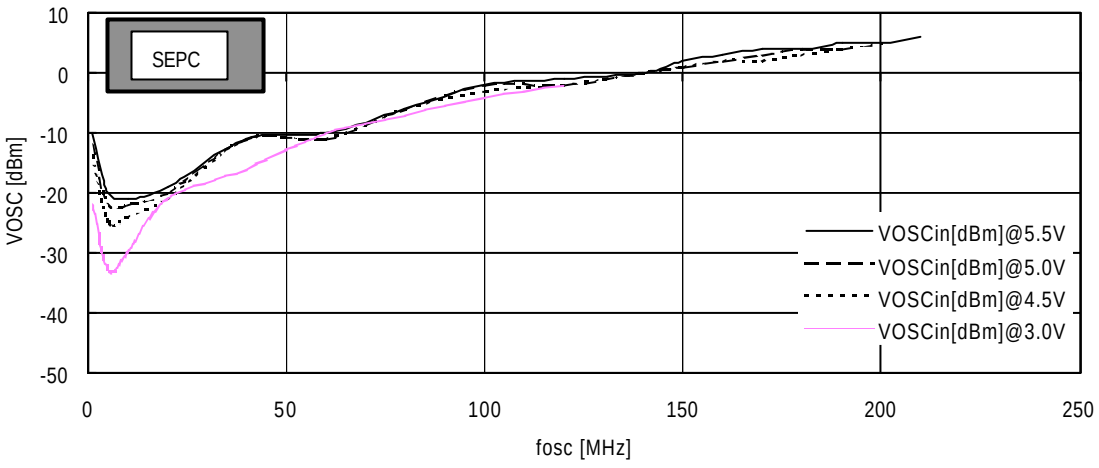
Input sensitivity of fin (RF1) versus Input frequency



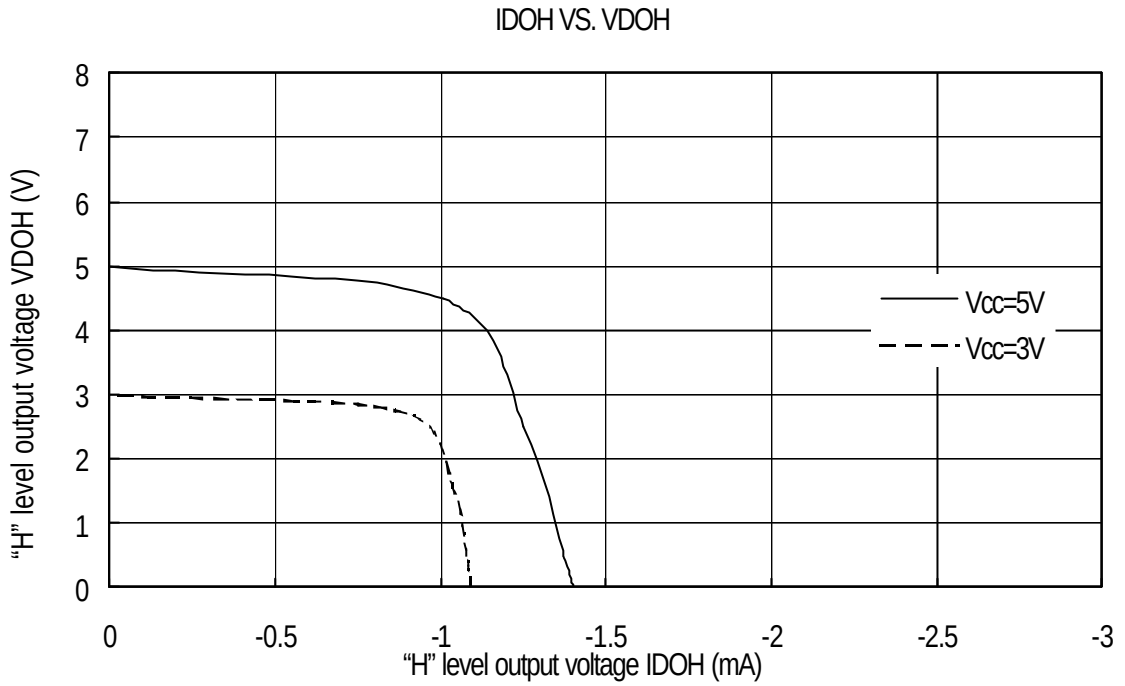
Input sensitivity of fin (RF2) versus Input frequency

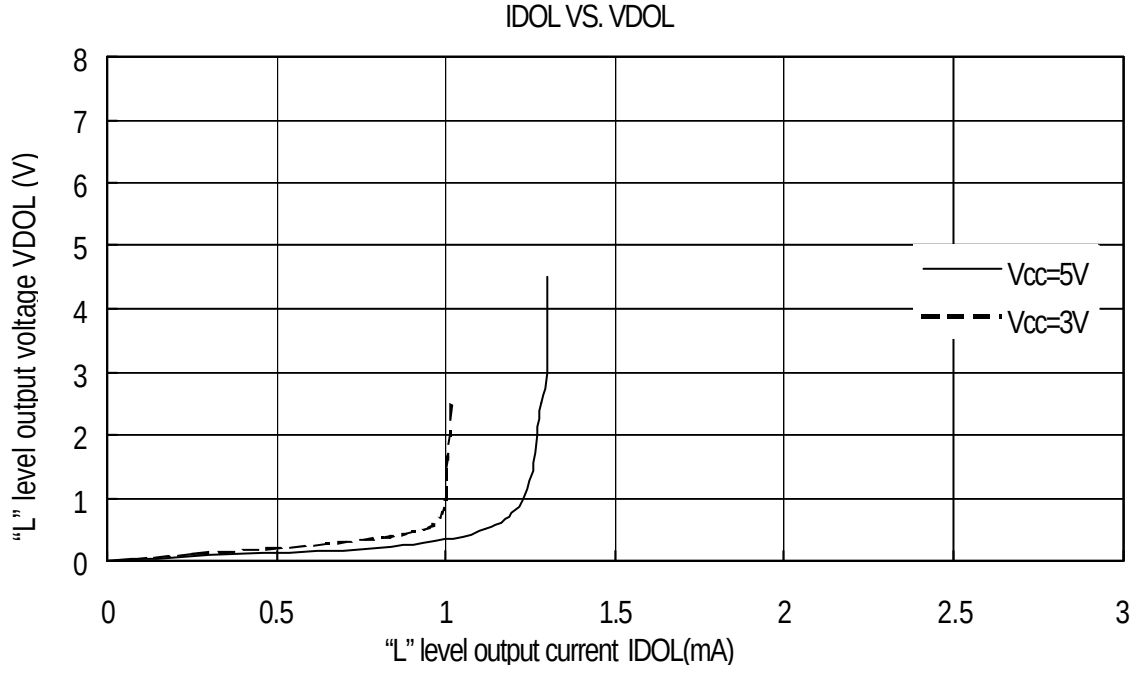


2.OSCin Input seinsitivity

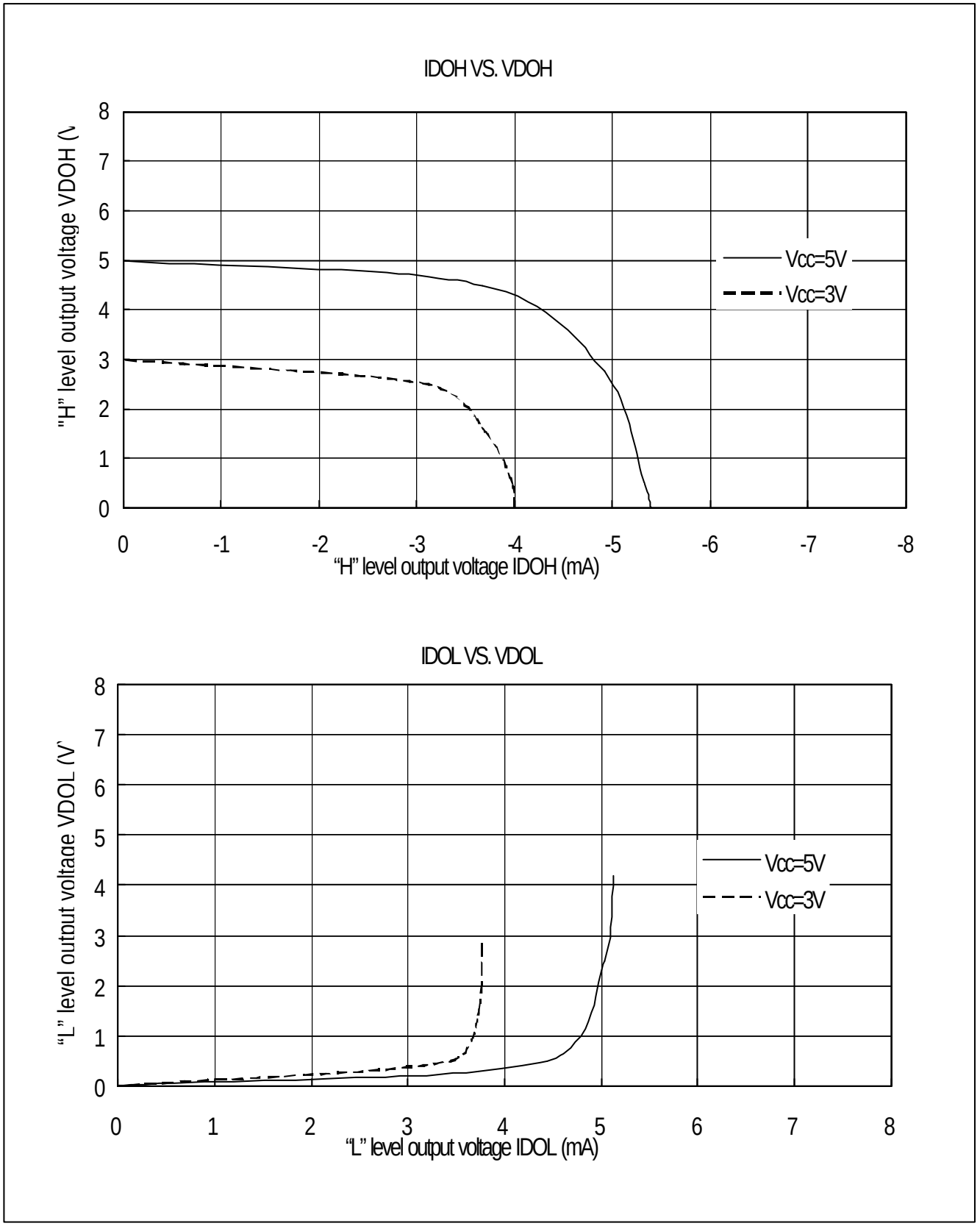


3.Do output current (1´Do mode)



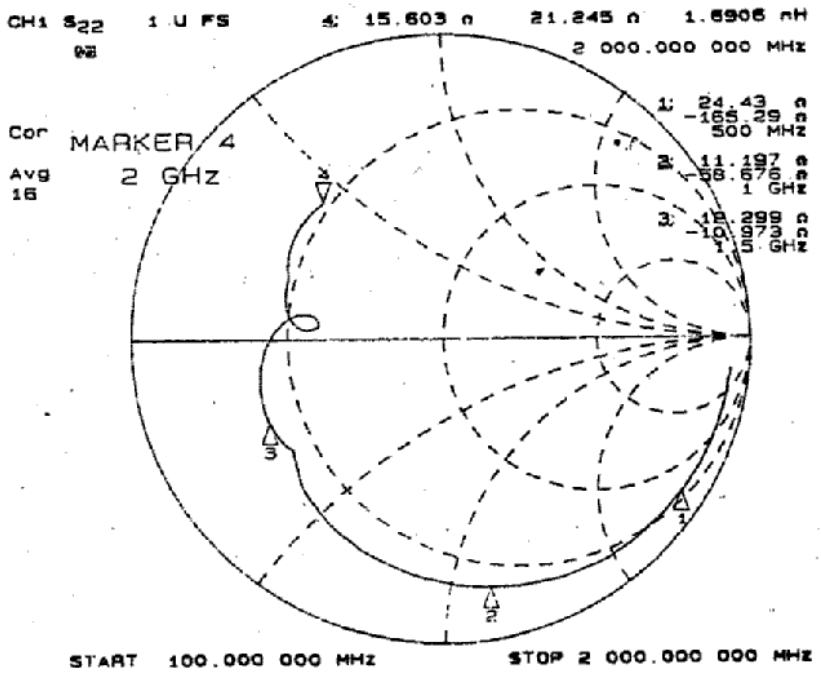


4.Do output current (4´ Do mode)

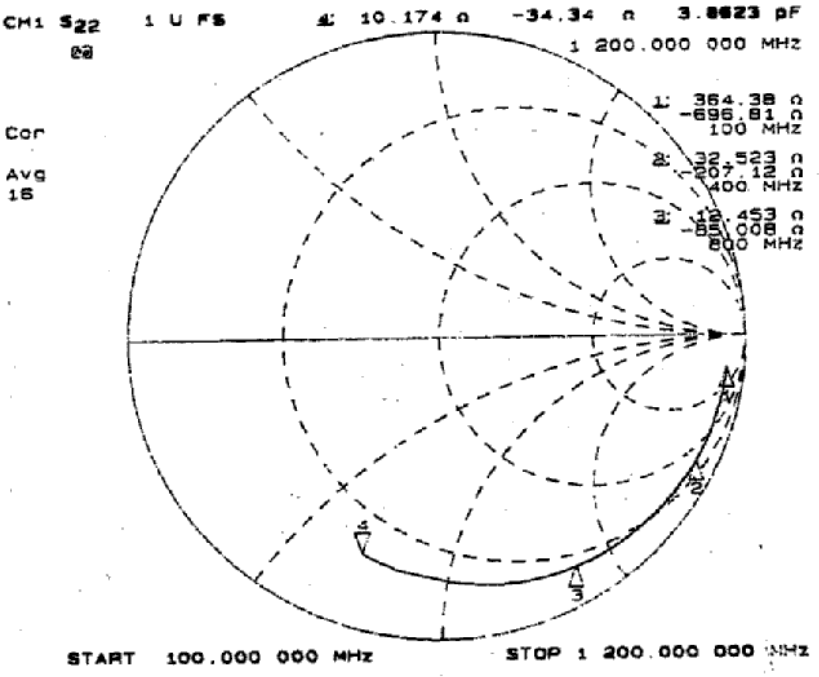


5.Input impedance

Input impedance of fin (RF1)

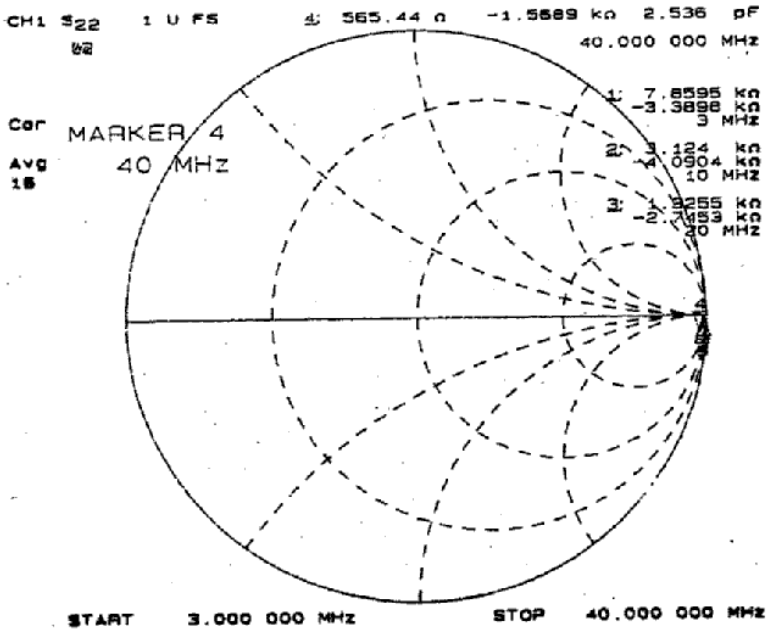


Input impedance of fin (RF2)

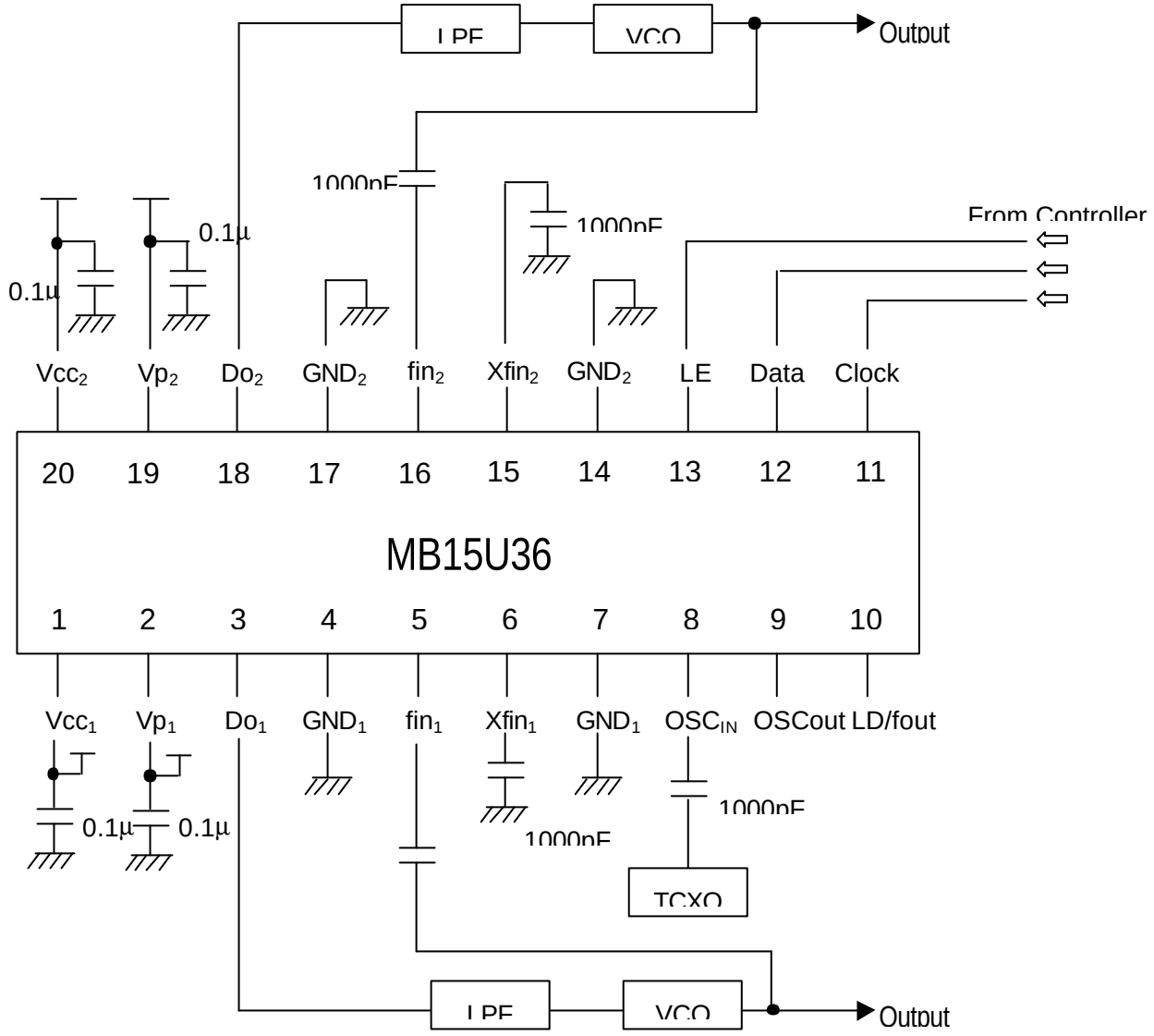


5.Input impedance

Input impedance of fin (OSCin)

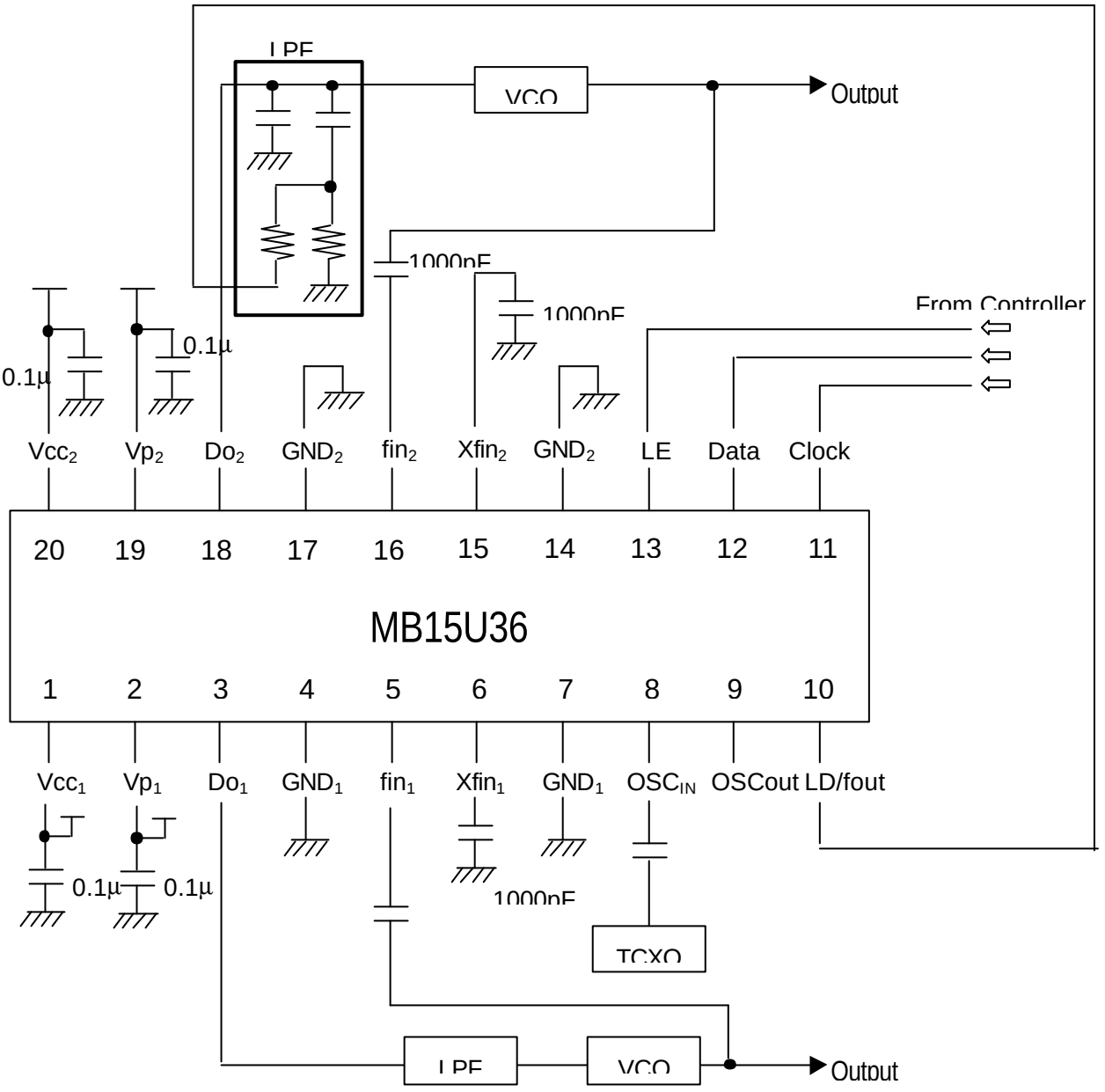


➢ APPLICATION EXAMPLE



Clock, Data, LE : Insert a pull-down or pull-up resister as needed to prevent oscillation when the terminals are left open.

➢ APPLICATION EXAMPLE : Fast lock mode



Clock, Data, LE : Insert a pull-down or pull-up resister as needed to prevent oscillation when the terminals are left open.

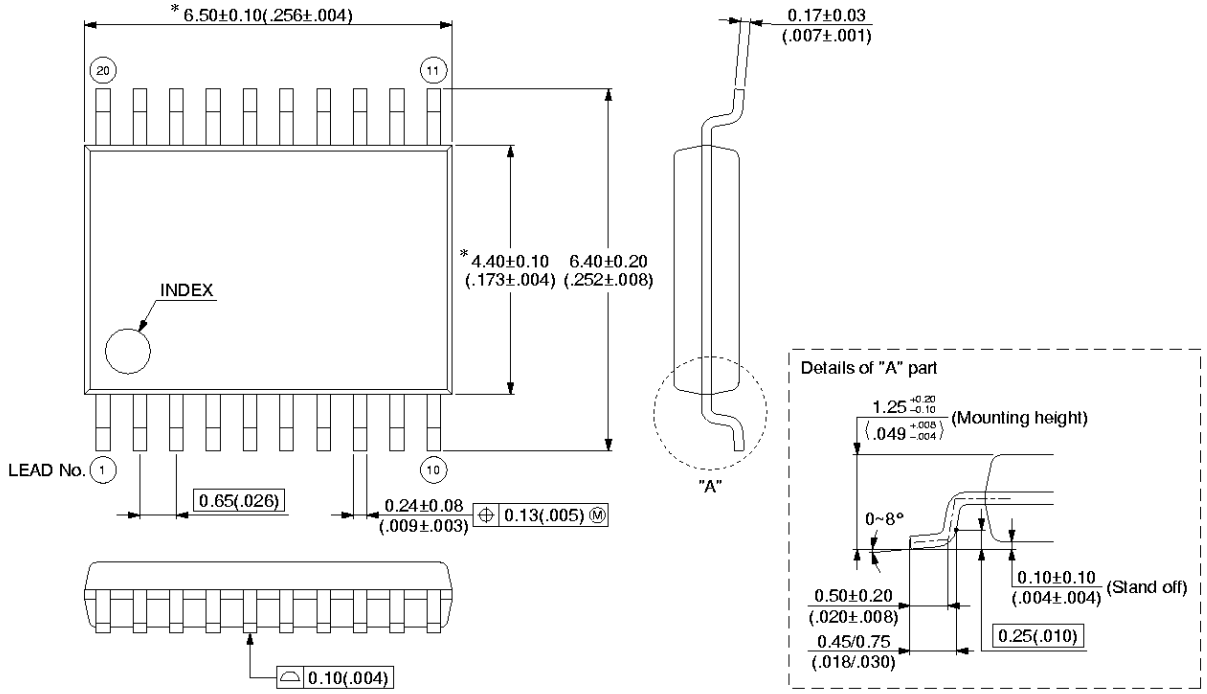
The Fastlock mode is controlled by the LDS/FDS bits and the CMC$_{RF1}$ bit. When the CMC$_{RF1}$ bit is set to "H" (the RF1 charge pump current is increased 4x normal mode), the LD/fout pin (open drain output) is "L", enabling the parallel resistor in the loop filter. This effectively increases the LPF bandwidth, allowing the loop to lock faster. After the loop has locked onto a new frequency, the CMC$_{RF1}$ bit is set to "L", forcing the LD/fout output pin into a high impedance state and returning the LPF bandwidth back to its original value.

MB15U36

➢ PACKAGE DIMENSION

20pins, Plastic SSOP

(FPT-20P-M03)



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➢ ORDERING INFORMATION

Part number	Package	Remarks
MB15U36PFV	20pin Plastic SSOP (FPT-20P-M03)	-