

# DATA SHEET

## **PCK111**

Low voltage 1:10 differential  
ECL/PECL/HSTL clock driver

Product data  
Supersedes data of 2003 Dec 03

2004 Apr 23

# Low voltage 1:10 differential ECL/PECL/HSTL clock driver

## PCK111

### FEATURES

- 85 ps part-to-part skew typical
- 20 ps output-to-output skew typical
- Differential design
- $V_{BB}$  output
- Low voltage  $V_{EE}$  range of  $-2.25\text{ V}$  to  $-3.8\text{ V}$  for ECL
- Low voltage  $V_{CC}$  range of  $+2.375\text{ V}$  to  $+3.8\text{ V}$  for PECL
- $75\text{ k}\Omega$  input pull-down resistors
- ECL/PECL outputs
- Form, fit, and function compatible with MC100EP111

### DESCRIPTION

The PCK111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The PECL input signals can be either differential or single-ended if the  $V_{BB}$  output is used. The selected signal is fanned out to 10 identical differential outputs.

The PCK111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent  $t_{PD}$  distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into  $50\ \Omega$ , even if only one side is being used. In most applications, all ten differential pairs will be used, and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used, which, while not being catastrophic to most designs, will mean a loss of skew margin.

The PCK111 can be used for high performance clock distribution in  $+3.3\text{ V}$  or  $+2.5\text{ V}$  systems. Designers can take advantage of the PCK111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

The PCK111 may be driven single-endedly utilizing the  $V_{BB}$  bias output with the  $\overline{CLK0}$  input. If a single-ended signal is to be used, the  $V_{BB}$  pin should be connected to the  $\overline{CLK0}$  input and bypassed to ground via a  $0.01\ \mu\text{F}$  capacitor. The  $V_{BB}$  output can only source/sink  $0.2\text{ mA}$ , therefore, it should be used as a switching reference for the PCK111 only. Part-to-part skew specifications are not guaranteed when driving the PCK111 single-endedly.

### PINNING

#### Pin configurations

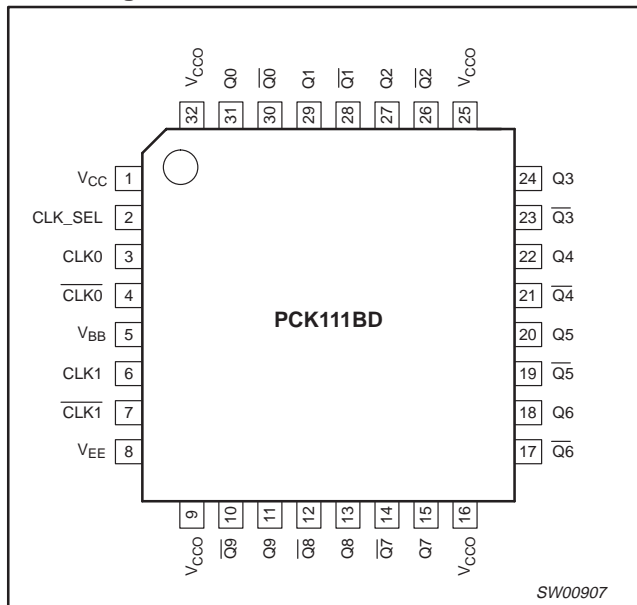


Figure 1. LQFP32 pin configuration

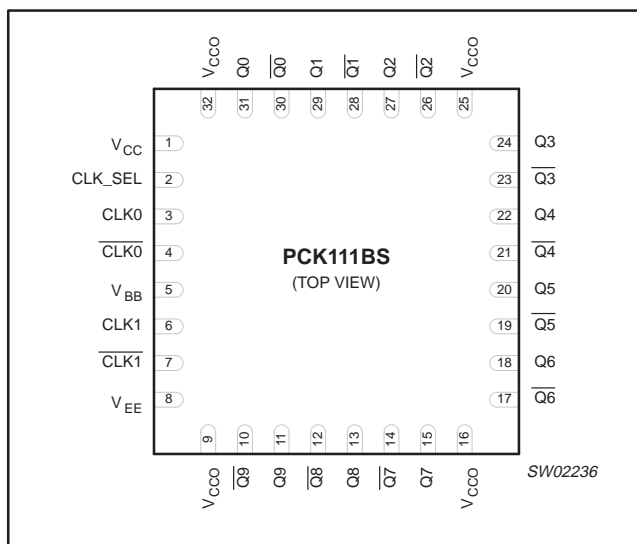


Figure 2. HVQFN32 pin configuration

### ORDERING INFORMATION

Type number	Package		Version	Temperature range
	Name	Description		
PCK111BD	LQFP32	plastic low profile quad flat package; 32 leads; body $7 \times 7 \times 1.4\text{ mm}$	SOT358-1	$-40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$
PCK111BS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85\text{ mm}$	SOT617-1	$-40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$

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PCK111

## Pin description

SYMBOL	PIN	DESCRIPTION
V <sub>CC</sub>	1	Supply voltage
CLK_SEL	2	Active CMOS clock select input
CLK0, $\overline{\text{CLK0}}$	3, 4	Differential ECL/PECL/HSTL input pair
V <sub>BB</sub>	5	Reference voltage output
CLK1, $\overline{\text{CLK1}}$	6, 7	Differential ECL/PECL/HSTL input pair
V <sub>EE</sub>	8	Ground
V <sub>CCO</sub>	9, 16, 25, 32	Output drive power supply voltage
Q0–Q9	31, 29, 27, 24, 22, 20, 18, 15, 13, 11	Differential PECL outputs
$\overline{\text{Q0}}-\overline{\text{Q9}}$	30, 28, 26, 23, 21, 19, 17, 14, 12, 10	Differential PECL outputs

## LOGIC SYMBOL

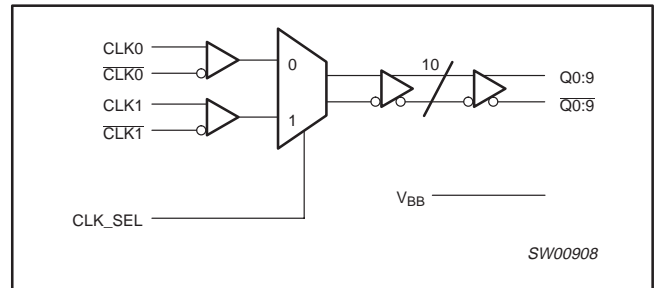


Figure 3. Logic symbol

## FUNCTION TABLE

CLK_SEL	Active input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	LIMITS	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +4.6	V
ESDHBM	Electrostatic discharge (Human Body Model; 1.5 kΩ, 100 pF)	>1.75	kV
ESDMM	Electrostatic discharge (Machine Model; 0 kΩ, 200 pF)	>200	V
ESDCDM	Electrostatic discharge (Charge Device Model)	>1000	V

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.25	3.8	V
V <sub>IR</sub>	Receiver input voltage		V <sub>EE</sub>	V <sub>CC</sub>	V
V <sub>DIFF</sub>	Input differential voltage <sup>1</sup>	V <sub>(CLKinN)</sub> -V <sub>(CLKin)</sub>	—	1.00	V
T <sub>amb</sub>	Operating ambient temperature range in free air		-40	+85	°C

### NOTE:

- To idle an unused differential clock input, connect one input terminal (e.g. CLK1) to V<sub>BB</sub> and leave its complimentary input terminal (e.g.  $\overline{\text{CLK1}}$ ) open-circuit, in which case  $\overline{\text{CLK1}}$  will default LOW by its internal pull-down resistor. Inputs should not be shorted to ground or V<sub>CC</sub>.

# Low voltage 1:10 differential ECL/PECL/HSTL clock driver

PCK111

## DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.25\text{ to }-3.80\text{ V}$ 

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	85 °C MIN	85 °C MAX	UNIT
$I_{EE}$	Internal supply current	Absolute value of current	45	85	60	95	65	105	mA
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC} = -2.0\text{ V}$	270	360	290	380	300	380	mA
$I_{IN}$	Input current	Includes pullup/pulldown resistors	—	150	—	150	—	150	$\mu\text{A}$
$V_{BB}$	Internal bias voltage		-1.38	-1.23	-1.38	-1.23	-1.38	-1.23	V
$V_{IH}$	Input HIGH voltage	Single ended	-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V
		CLK_SEL	$0.2V_{EE}$	$V_{CC}$	$0.2V_{EE}$	$V_{CC}$	$0.2V_{EE}$	$V_{CC}$	V
$V_{IL}$	Input LOW voltage	Single ended	-1.810	-1.475	-1.810	-1.475	-1.810	-1.475	V
		CLK_SEL	$V_{EE}$	$0.8V_{EE}$	$V_{EE}$	$0.8V_{EE}$	$V_{EE}$	$0.8V_{EE}$	V
$V_{PP}$	Input amplitude	Difference of input = $V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
$V_{CMR}$	Common mode voltage	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	$V_{EE} + 1.0$	-0.3	$V_{EE} + 1.0$	-0.3	$V_{EE} + 1.0$	-0.3	V
$V_{OH}$	Output HIGH voltage	$I_{OH} = -30\text{ mA}$	-1.3	-0.95	—	—	-1.2	0.90	V
$V_{OL}$	Output LOW voltage	$I_{OL} = -5\text{ mA}$	-1.85	-1.4	—	—	-1.90	-1.5	V
$V_{OUTpp}$	Differential output swing		350	—	—	—	500	—	MV

### NOTE:

- $V_{PP}$  minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum  $V_{PP}$  of 100 mV.

## DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = V_{CCO} = 2.25\text{ to }3.80\text{ V}$ ,  $V_{EE} = 0\text{ V}$ 

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	85 °C MIN	85 °C MAX	UNIT
$I_{EE}$	Internal supply current	Absolute value of current	45	85	60	95	65	105	mA
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC} = -2.0\text{ V}$	270	360	290	380	300	380	mA
$I_{IN}$	Input current	Includes pullup/pulldown resistors	—	150	—	150	—	150	$\mu\text{A}$
$V_{BB}$	Internal bias voltage		$V_{CC}$ -1.38	$V_{CC}$ -1.23	$V_{CC}$ -1.38	$V_{CC}$ -1.23	$V_{CC}$ -1.38	$V_{CC}$ -1.23	V
$V_{IH}$	Input HIGH voltage	Single ended	$V_{CC}$ -1.165	$V_{CC}$ -0.880	$V_{CC}$ -1.165	$V_{CC}$ -0.880	$V_{CC}$ -1.165	$V_{CC}$ -0.880	V
		CLK_SEL	$0.8V_{CC}$	$V_{CC}$	$0.8V_{CC}$	$V_{CC}$	$0.8V_{CC}$	$V_{CC}$	V
$V_{IL}$	Input LOW voltage	Single ended	$V_{CC}$ -1.810	$V_{CC}$ -1.475	$V_{CC}$ -1.810	$V_{CC}$ -1.475	$V_{CC}$ -1.810	$V_{CC}$ -1.475	V
		CLK_SEL	$V_{EE}$	$0.2V_{CC}$	$V_{EE}$	$0.2V_{CC}$	$V_{EE}$	$0.2V_{CC}$	V
$V_{PP}$	Input amplitude	Difference of input = $V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
$V_{CMR}$	Common mode voltage	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	1.0	$V_{CC}-0.3$	1.0	$V_{CC}-0.3$	1.0	$V_{CC}-0.3$	V
$V_{IHCMR}$	Input HIGH voltage (HSTL)		1.2	$V_{CC}$	1.2	$V_{CC}$	1.2	$V_{CC}$	V
$V_x$	Input crossover voltage (HSTL)	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	0.68	0.9	0.68	0.9	0.68	0.9	V
$V_{OH}$	Output HIGH voltage	$I_{OH} = -30\text{ mA}$	$V_{CC}$ -1.30	$V_{CC}$ -0.95	—	—	$V_{CC}$ -1.20	$V_{CC}$ -0.90	V
$V_{OL}$	Output LOW voltage	$I_{OL} = -5\text{ mA}$	$V_{CC}$ -1.85	$V_{CC}$ -1.40	—	—	$V_{CC}$ -1.90	$V_{CC}$ -1.50	V
$V_{OUTpp}$	Differential output swing		350	—	—	—	500	—	MV

### NOTE:

- $V_{PP}$  minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum  $V_{PP}$  of 100 mV.

# Low voltage 1:10 differential ECL/PECL/HSTL clock driver

PCK111

## AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 2.25\text{ V to }3.80\text{ V}$ ,  $V_{EE} = 0\text{ V}$ , or  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.25\text{ V to }-3.80\text{ V}$ 

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	85 °C MIN	85 °C MAX	UNIT
$t_{PD}$	Differential propagation delay	Nominal (single input condition) $V_{PP} = 0.650\text{ V}$ , $V_{CMR} = V_{CC} - 0.800\text{ V}$ (Note 1)	350	500	380	530	450	590	ps
$t_{skew}$	Part-to-part skew	Note 1	—	110	—	110	—	110	ps
$t_{skew}$	Output-to-output same part skew	Note 1	—	50	—	50	—	50	ps
$t_{jitter}$	Cycle-to-cycle jitter		—	1	—	1	—	1	ps
$f_{MAX}$	Maximum output frequency	Functional to 1.5 GHz; Timing specifications apply to 1.0 GHz	—	1500	—	1500	—	1500	MHz
$t_r/t_f$	Output rise/fall time at 20% to 80%	All outputs terminated 50 $\Omega$ to $V_{CC} - 2.0\text{ V}$	100	300	100	300	100	300	ps

### NOTE:

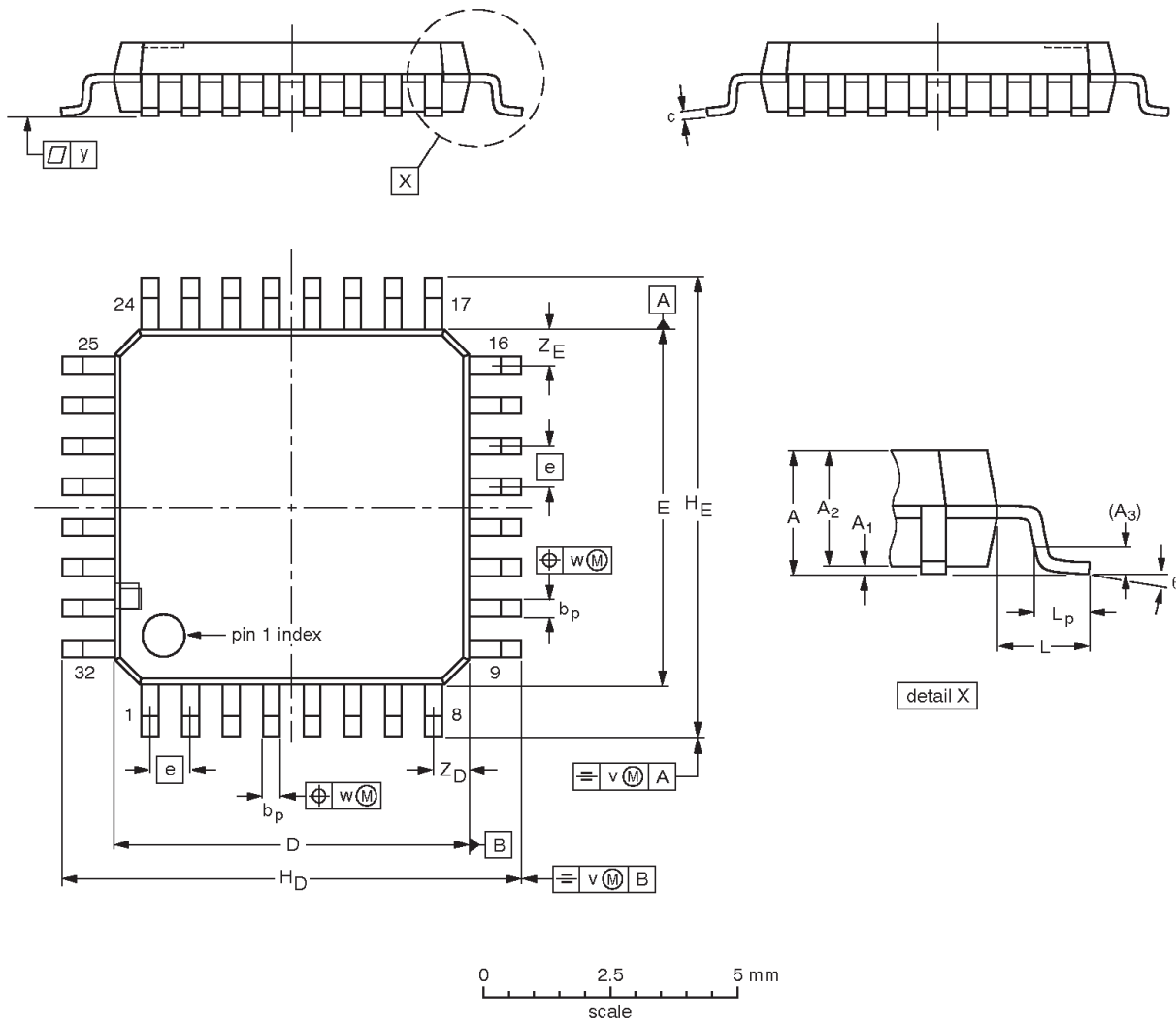
- For operation with 2.5 V supply, the output termination is 50  $\Omega$  to  $V_{EE}$ .  
For operation with 3.3 V supply, the output termination is 50  $\Omega$  to  $V_{CC} - 2\text{ V}$ .

# Low voltage 1:10 differential ECL/PECL/HSTL clock driver

PCK111

**LQFP32:** plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm

**SOT358-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

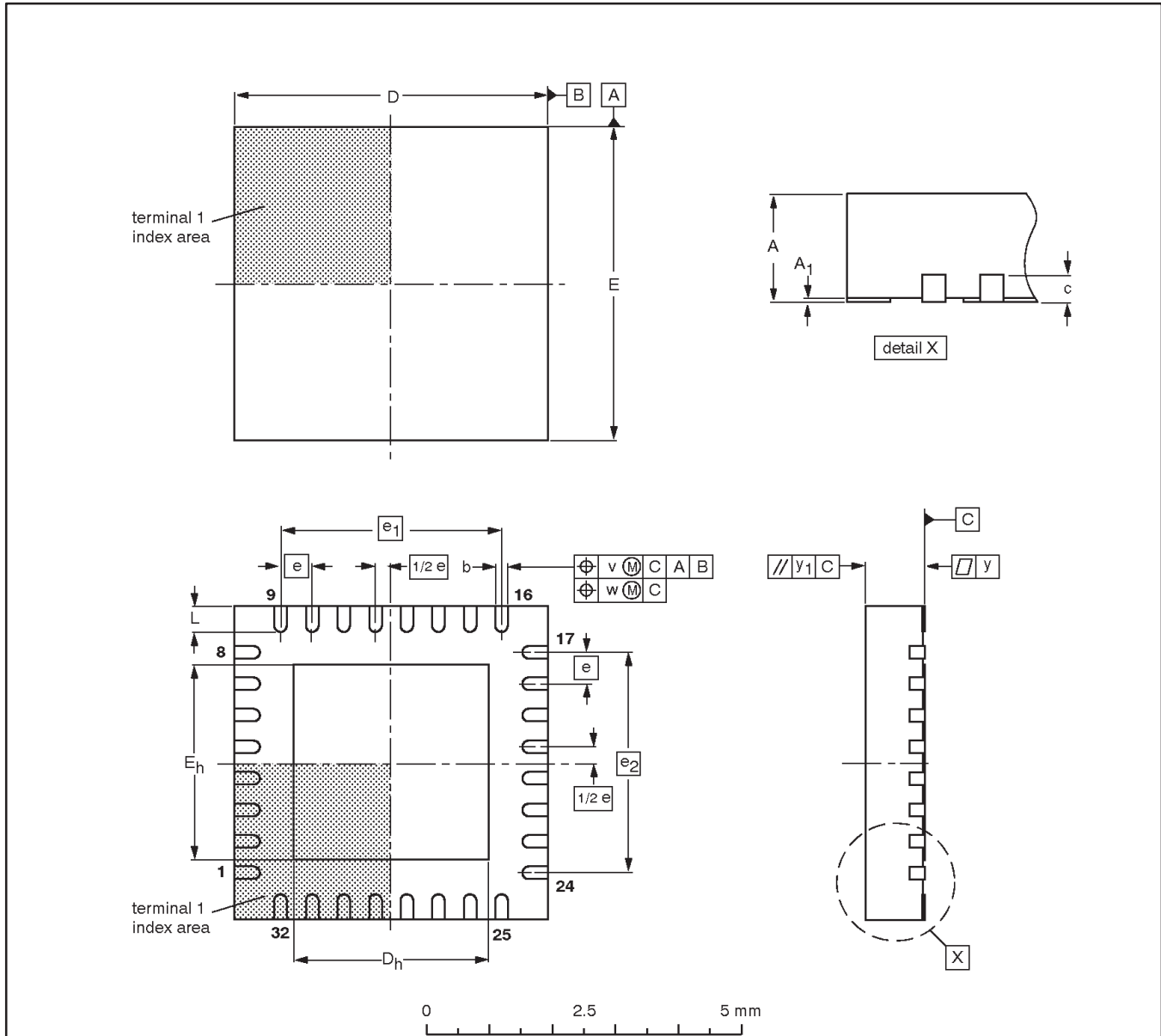
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				00-01-19 03-02-25

Low voltage 1:10 differential  
ECL/PECL/HSTL clock driver

PCK111

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals;  
body 5 x 5 x 0.85 mm

SOT617-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	---	MO-220	---			01-08-08 02-10-18

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**Low voltage 1:10 differential  
ECL/PECL/HSTL clock driver**

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**PCK111****REVISION HISTORY**

Rev	Date	Description
_5	20040423	<b>Product data (9397 750 13082). Supersedes data of 2003 Dec 03 (9397 750 12451).</b> Modifications: <ul style="list-style-type: none"><li>• Add Part type PCK111BS, HVQFN32 package option (SOT617-1).</li></ul>
_4	20031203	Product data (9397 750 12451); ECN 853-2281 01-A14515 dated 14 November 2003. Supersedes data of 13 December 2002 (9397 750 10865).
_3	20021213	Product data (9397 750 10865); ECN 853-2281 29225 of 22 November 2002.
_2	20020215	Product data (9397 750 09465); ECN 853-2281 27735 of 15 February 2002.



# Low voltage 1:10 differential ECL/PECL/HSTL clock driver

PCK111

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
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Date of release: 04-04

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Document order number:

9397 750 13082

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